



## 18 Output, 3.3V SDRAM Buffer for Desktop PCs with 4 DIMMs

### Features

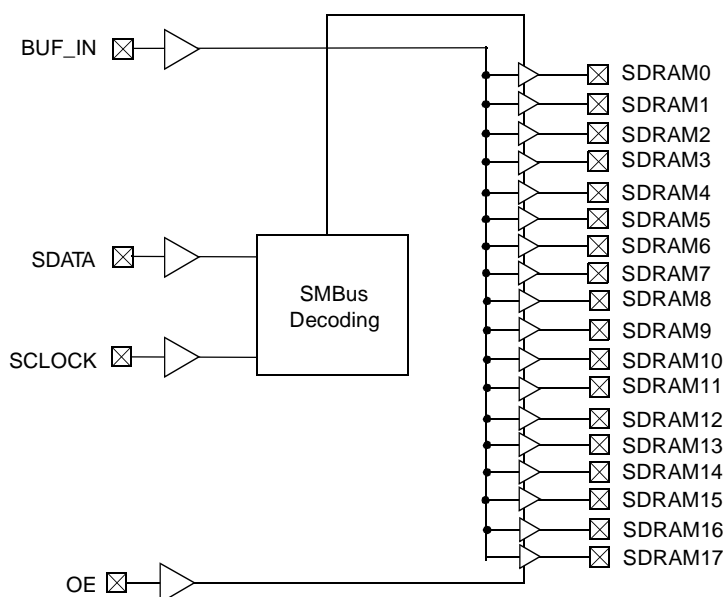
- One input to 18 output buffer/driver
- Supports up to four SDRAM DIMMs
- Two additional outputs for feedback
- SMBus interface for individual output control
- Low skew outputs (< 200 ps)
- Up to 100 MHz operation
- Dedicated OE pin for testing
- Space-saving 48-pin SSOP package
- 3.3V operation

### Functional Description

The CY2318BNZ is a 3.3V buffer designed to distribute high-speed clocks in PC applications. The part has 18 outputs, 16 of which can be used to drive up to four SDRAM DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium II® processors. The CY2318BNZ can be used in conjunction with the CY2280, CY2281, CY2282 or similar clock synthesizer for a complete Pentium II motherboard solution.

The CY2318BNZ also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull up). A separate Output Enable pin facilitates testing on ATE.

### Block Diagram



### Pin Configuration

#### SSOP Top View

NC	1	48	NC
NC	2	47	NC
V <sub>DD</sub>	3	46	V <sub>DD</sub>
SDRAM0	4	45	SDRAM15
SDRAM1	5	44	SDRAM14
V <sub>SS</sub>	6	43	V <sub>SS</sub>
V <sub>DD</sub>	7	42	V <sub>DD</sub>
SDRAM2	8	41	SDRAM13
SDRAM3	9	40	SDRAM12
V <sub>SS</sub>	10	39	V <sub>SS</sub>
BUF_IN	11	38	OE
V <sub>DD</sub>	12	37	V <sub>DD</sub>
SDRAM4	13	36	SDRAM11
SDRAM5	14	35	SDRAM10
V <sub>SS</sub>	15	34	V <sub>SS</sub>
V <sub>DD</sub>	16	33	V <sub>DD</sub>
SDRAM6	17	32	SDRAM9
SDRAM7	18	31	SDRAM8
V <sub>SS</sub>	19	30	V <sub>SS</sub>
V <sub>DD</sub>	20	29	V <sub>DD</sub>
SDRAM16	21	28	SDRAM17
V <sub>SS</sub>	22	27	V <sub>SS</sub>
V <sub>DDIIC</sub>	23	26	V <sub>SSIIC</sub>
SDATA	24	25	SCLOCK

Pentium II is a registered trademark of Intel Corporation.

## Pin Summary

Name	Pins	Description
V <sub>DD</sub>	3, 7, 12, 16, 20, 29, 33, 37, 42, 46	3.3V Digital voltage supply
V <sub>SS</sub>	6, 10, 15, 19, 22, 27, 30, 34, 39, 43	Ground
V <sub>DDIIC</sub>	23	SMBus Voltage supply
V <sub>SSIIC</sub>	26	Ground for SMBus
BUF_IN	11	Input clock (5V Tolerant)
OE	38	Output Enable (active HIGH), Three-state outputs when low <sup>[1]</sup>
SDATA	24	SMBus data input <sup>[1]</sup>
SCLK	25	SMBus clock input <sup>[1]</sup>
SDRAM [0–3]	4, 5, 8, 9	SDRAM byte 0 clock outputs
SDRAM [4–7]	13, 14, 17, 18	SDRAM byte 1 clock outputs
SDRAM [8–11]	31, 32, 35, 36	SDRAM byte 2 clock outputs
SDRAM [12–15]	40, 41, 44, 45	SDRAM byte 3 clock outputs
SDRAM [16–17]	21, 28	SDRAM clock outputs usable for feedback
N/C	1, 2, 47, 48	Reserved for future modifications, do not connect in system

**Note:**

1. Internal pull-up resistor to V<sub>DD</sub> (value > 100 kohms).

## Device Functionality

OE	SDRAM [0–17]
0	Hi-Z
1	1 x BUF_IN

## Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0".
- SMBus Address for the CY2318BNZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

### Byte 0: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	18	SDRAM7 (Active/Inactive)
Bit 6	17	SDRAM6 (Active/Inactive)
Bit 5	14	SDRAM5 (Active/Inactive)
Bit 4	13	SDRAM4 (Active/Inactive)
Bit 3	9	SDRAM3 (Active/Inactive)
Bit 2	8	SDRAM2 (Active/Inactive)
Bit 1	5	SDRAM1 (Active/Inactive)
Bit 0	4	SDRAM0 (Active/Inactive)

### Byte 1: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	45	SDRAM15 (Active/Inactive)
Bit 6	44	SDRAM14 (Active/Inactive)
Bit 5	41	SDRAM13 (Active/Inactive)
Bit 4	40	SDRAM12 (Active/Inactive)
Bit 3	36	SDRAM11 (Active/Inactive)
Bit 2	35	SDRAM10 (Active/Inactive)
Bit 1	32	SDRAM9 (Active/Inactive)
Bit 0	31	SDRAM8 (Active/Inactive)

### Byte 2: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	28	SDRAM17 (Active/Inactive)
Bit 6	21	SDRAM16 (Active/Inactive)
Bit 5	--	Reserved, drive to 0
Bit 4	--	Reserved, drive to 0
Bit 3	--	Reserved, drive to 0
Bit 2	--	Reserved, drive to 0
Bit 1	--	Reserved, drive to 0
Bit 0	--	Reserved, drive to 0

## Maximum Ratings

Supply Voltage to Ground Potential ..... -0.5 to +7.0V  
 DC Input Voltage (except BUF\_IN) ..... -0.5V to  $V_{DD}+0.5$   
 DC Input Voltage (BUF\_IN) ..... -0.5V to 7.0V  
 Storage Temperature ..... -65°C to +150°C

Static Discharge Voltage  
 (per MIL-STD-883, Method 3015) ..... >2000V  
 Ambient Temperature under BIAS ..... -55°C to +125°C

## Operating Conditions

Parameter	Description	Min.	Max.	Unit
$V_{DD}, V_{DDIIC}$	Supply Voltage	3.135	3.465	V
$T_A$	Operating Temperature (Ambient Temperature)	-40	85	°C
$C_L$	Load Capacitance	20	30	pF
$C_{IN}$	Input Capacitance		7	pF

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any Pin with Respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Operating Temperature	0 to +70	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C

## DC Electrical Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{DDQ3} = 3.3\text{V} \pm 5\%$

Parameter	Description	Test Condition/ Comments	Min	Typ	Max	Unit
$I_{DD}$	3.3V Supply Current	BUF_IN = 64 MHz	140	165	200	mA
$I_{DD}$ Tristate	3.3V Supply Current in Three-state	BUF_IN = 100 MHz		5		mA
<b>Logic Inputs (BUF_IN, OE, SCLOCK, SDATA)</b>						
$V_{IL}$	Input Low Voltage		GND-0.3		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DDQ3} + 0.5$	V
$I_{ILEAK}$	Input Leakage Current, BUF_IN		-5		+5	μA
$I_{ILEAK}$	Input Leakage Current <sup>[2]</sup>		-20		+5	μA
<b>Logic Outputs (SDRAM0:17)<sup>[3]</sup></b>						
$V_{OL}$	Output Low Voltage	$I_{OL} = 1 \text{ mA}$			50	mV
$V_{OH}$	Output High Voltage	$I_{OH} = -1 \text{ mA}$	3.1			V
$I_{OL}$	Output Low Current	$V_{OL} = 1.5\text{V}$	70	110	185	mA
$I_{OH}$	Output High Current	$V_{OH} = 1.5\text{V}$	65	100	160	mA
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance (Except BUF_IN)				5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

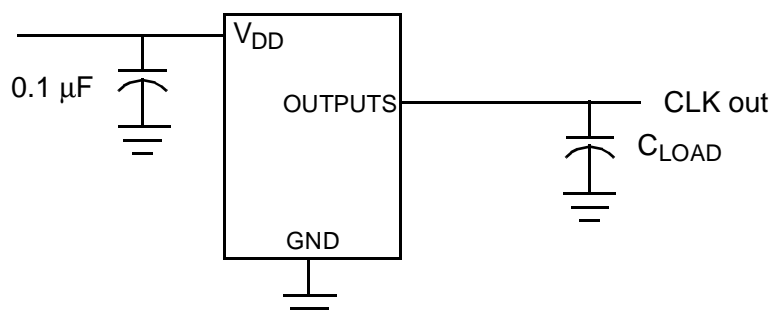
### Notes:

- OE, SCLOCK, and SDATA logic pins have a 250-kΩ internal pull-up resistor (not CMOS level).
- Outputs loaded by 6" 60Ω transmission lines with 20-pF capacitors.

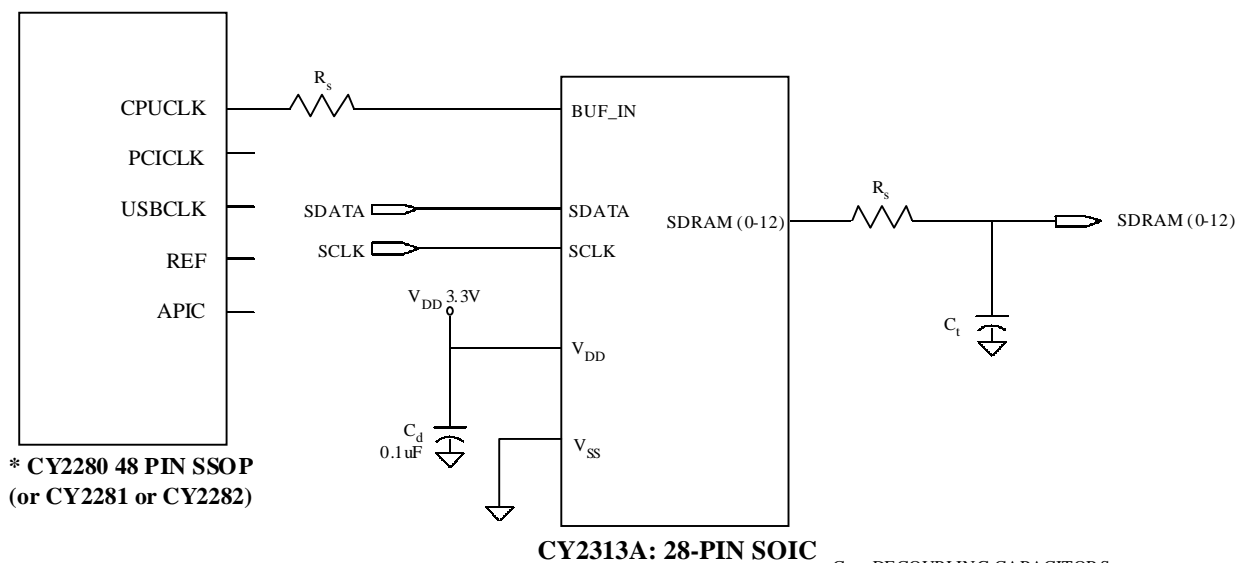
**AC Electrical Characteristics:**  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$  (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
$f_{IN}$	Input Frequency		0		133	MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
$t_{SR}$	Output Skew, Rising Edges				200	ps
$t_{SF}$	Output Skew, Falling Edges				200	ps
$t_{EN}$	Output Enable Time		1.0		8.0	ns
$t_{DIS}$	Output Disable Time		1.0		8.0	ns
$t_{PR}$	Rising Edge Propagation Delay		3.0	3.85	5.0	ns
$t_{PF}$	Falling Edge Propagation Delay		3.0	3.85	5.0	ns
$t_D$	Duty Cycle	Measured at 1.5V	50		60	%
$Z_o$	AC Output Impedance			15		$\Omega$

### Test Circuit



## Application Circuit



\* THIS FREQUENCY SYNTHESIZER IS USED TO GENERATE CPU, PCI, USB, REF, AND APIC CLOCKS.

$C_d$  = DECOUPLING CAPACITORS  
 $C_t$  = OPTIONAL EMI-REDUCING CAPACITORS  
 $R_s$  = SERIES TERMINATING RESISTORS

## Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2318BNZPVI-11	O48	48-Pin SSOP	Industrial (-40 to 85)

Document #: 38-01091-\*\*

## Package Diagram

### 48-Lead Shrink Small Outline Package O48

