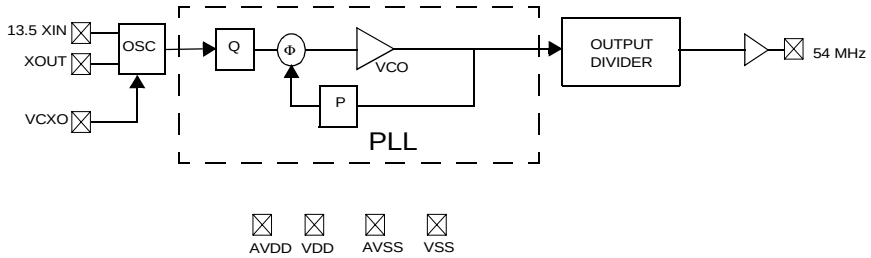
CY2411

54-MHz MPEG Clock Generator with VCXO

Features	Benefits
• **Integrated phase-locked loop**	Highest Performance PLL tailored for multimedia applications
• **Low-jitter, high-accuracy outputs**	Meets critical timing requirements in complex system designs
• **VCXO with analog adjust**	Large ± 150 ppm range, better linearity
• **3.3V Operation**	

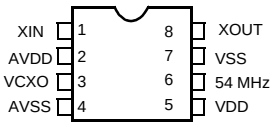
Part Number	Outputs	Input Frequency Range	Output Frequencies
CY2411	1	13.5-MHz Pullable Crystal per Cypress Specification	1 copy of 54 MHz (3.3V)

Logic Block Diagram



Pin Configuration

CY2411
8-pin SOIC



Pin Summary

Name	Pin Number CY2411	Description
A_{VDD}	2	Analog Voltage Supply
V_{DD}	5	Output Voltage Supply
AV_{SS}	4	Analog Ground
V_{SS}	7	Output Ground
X_{IN}	1	Reference Crystal Input
V_{CXO}	3	Analog Control for V_{CXO}
X_{OUT}[1]	8	Reference Crystal Output
54 MHz	6	54 MHz clock output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[2]	–65	100	° C
T_J	Junction Temperature		100	° C
	Digital Inputs	V_{SS}–0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS}–0.3	V_{DD} + 0.3	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
T_A	Ambient Temperature	0		70	° C
C_{LOAD}	Max Load Capacitance			20	pF
P_{max}	Max Output Power Dissipation, 8-pin package			150	° C/W
f_{REF}	Reference Frequency	10	13.5	30	MHz

DC Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	V_{OH} = V_{DD}–0.5, V_{DD}=3.3 V	12	24		mA
I_{OL}	Output Low Current	V_{OL} = 0.5, V_{DD}=3.3 V	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		µA
$f_{\Delta xo}$	V_{CXO} pullability range		–150		+150	ppm
V_{VCXO}	V_{CXO} input range		0		AV_{DD}	V
f_{VBW}	V_{CXO} input bandwidth			DC to 200		kHz
I_{DD}	Supply Current	Sum of Core and Output Current		15	20	mA

Notes:

1. Float XOUT if XIN is externally driven.
2. Rated for 10 years.

AC Electrical Characteristics (V_{DD} = 3.3V)

Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of V_{DD}	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% to 20% of V_{DD}	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter			200	ps
t_{10}	PLL Lock Time				3	ms

Note:
3. Not 100% tested.

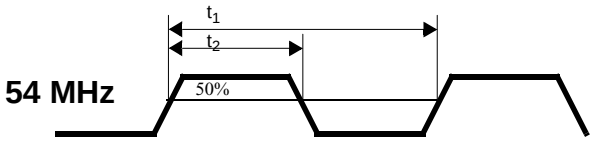


Figure 1. Duty Cycle Definition; DC = t_2/t_1

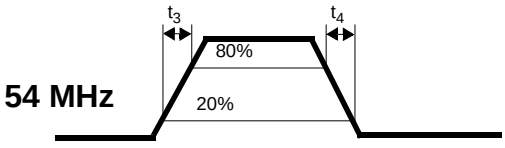
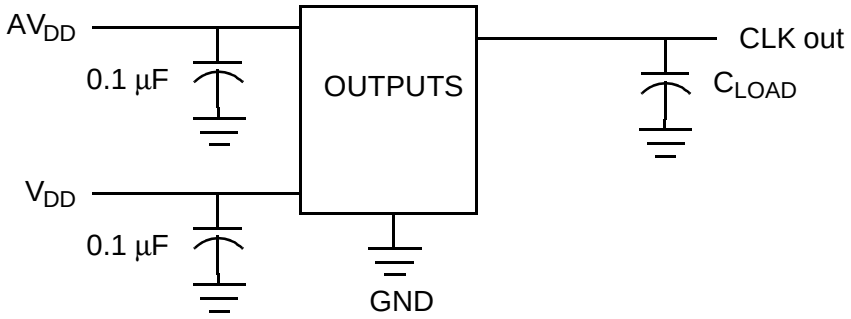


Figure 2. Rise and Fall Time Definitions

Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2411SC	S8	8-Pin SOIC	Commercial	3.3V

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Pin Diagrams

8-Lead (150-Mil) SOIC S8