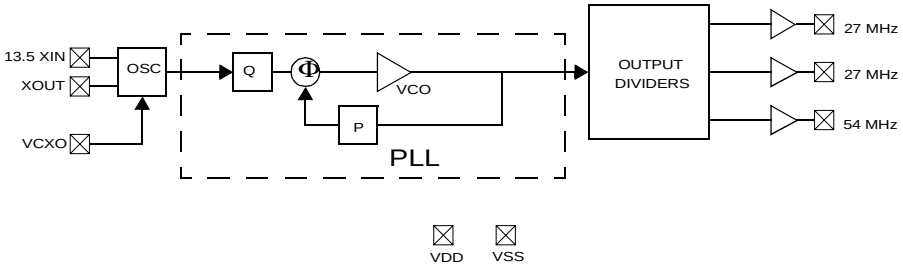
CY2412

MPEG Clock Generator with VCXO

Features	Benefits
• **Integrated phase-locked loop**	Highest Performance PLL tailored for multimedia applications
• **Low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **VCXO with analog adjust**	Large ±150 ppm range, better linearity
• **3.3V Operation**	Enables application compatibility

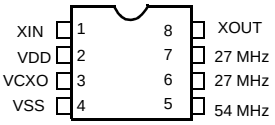
Part Number	Outputs	Input Frequency Range	Output Frequencies
CY2412	3	13.5 MHz pullable crystal input per Cypress Specification	Two copies of 27 MHz, one copy of 54 MHz (3.3V)

Logic Block Diagram



Pin Configuration

CY2412
8-pin SOIC



Pin Summary

Name	Pin Number	Description
XIN	1	Reference Crystal Input
V_{DD}	2	Voltage Supply
VCXO	3	Input Analog Control for VCXO
V_{SS}	4	Ground
54 MHz	5	54 MHz clock output
27 MHz	6	27 MHz clock outputs
27 MHz	7	27 MHz clock outputs
XOUT[1]	8	Reference Crystal Output

Pullable Crystal Specifications

Parameter	Name	Min.	Typ.	Max.	Unit
CR_{load}	Crystal Load Capacitance		14		pF
C0/C1			240		
ESR	Equivalent Series Resistance		35		Ω
T_o	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT_s	Stability over temperature and aging			± 50	ppm

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
VDD	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[2]	–65	100	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	VDD + 0.3	V
	Digital Outputs referred to VDD	V_{SS} – 0.3	VDD + 0.3	V
	Electro-Static Discharge	2		kV
	Soldering Temperature		235°	°C

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			20	pF
P_{max}	Max. Output Power Dissipation, 8-pin package			150	°C/W
f_{REF}	Reference Frequency		13.5		MHz

Notes:
1. Float XOUT if XIN is externally driven.
2. Rated for 10 years.

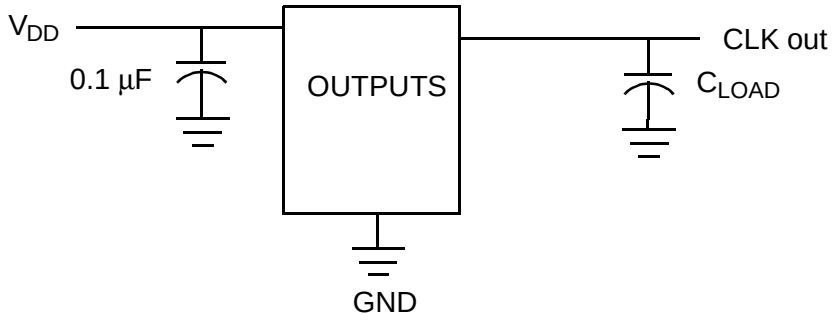
C Electrical Characteristics

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		µA
$f_{\Delta XO}$	VCXO pullability range		–150		+150	ppm
V_{VCXO}	VCXO input range		0		V_{DD}	V
f_{VBW}	VCXO input bandwidth			DC to 200		kHz
I_{DD}	Supply Current	Sum of Core and Output Current			35	mA

AC Electrical Characteristics

Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of V_{DD}	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of V_{DD}	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter		100	200	ps
t_{10}	PLL Lock Time				3	ms

Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2412SC	S8	8-Pin SOIC	Commercial	3.3V

Document #: 38-00898-*A

Note:
3. Not 100% tested.

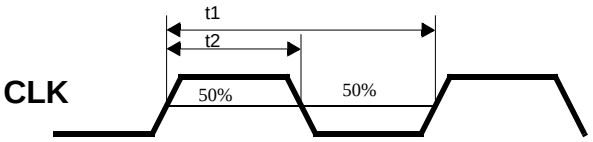


Figure 1. Duty Cycle Definition; DC = t2/t1

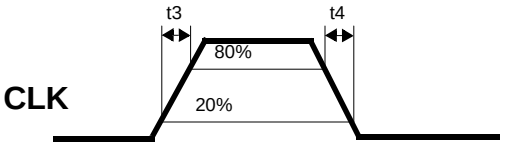


Figure 2. Rise and Fall Time Definitions

Package Diagram

8-Lead (150-Mil) SOIC S8