ADVANCE INFORMATION

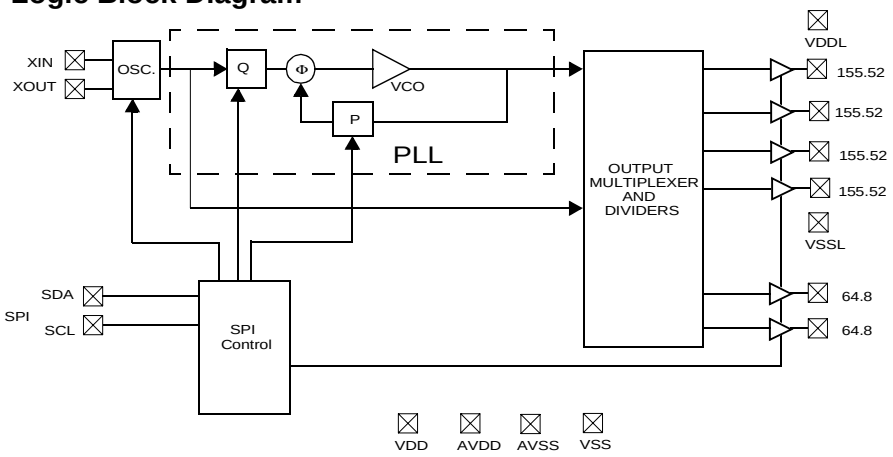
CY2414

One-PLL General Purpose Programmable Clock Generator

Features	Benefits
• **Integrated phase-locked loop**	Internal PLL with up to 333 MHz internal operation
• **Low skew, low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **Serial Programming Interface**	Industry Standard Interface for easy customization
• **3.3V Operation with 2.5 V Output Option**	Enables application compatibility

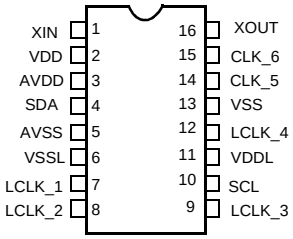
Part Number	Outputs	Input Frequency Range	Output Frequency Range
CY2414	6	10 MHz-30 MHz (external crystal) 250 kHz - 133 MHz (driven)	80 kHz-166 MHz (3.3V)

Logic Block Diagram



Pin Configurations

CY2414
16-pin TSSOP



Output	Default Frequency	Unit
XIN	64.8	MHz
LCLK_1	155.52	MHz
LCLK_2	155.52	MHz
LCLK_3	155.52	MHz
LCLK_4	155.52	MHz
CLK_5	64.8	MHz
CLK_6	64.8	MHz

Summary

Name	Pin Number CY2414	Description
XIN	1	Reference Crystal Input
VDD	2	Voltage Supply
AVDD	3	Analog Voltage Supply
SDA	4	SPI Serial Data
AVSS	5	Analog Ground
VSSL	6	LCLK Ground
LCLK_1	7	Configurable clock output 1 at VDDL level
LCLK_2	8	Configurable clock output 2 at VDDL level
LCLK_3	9	Configurable clock output 3 at VDDL level
SCL	10	SPI Serial Clock
VDDL	11	LCLK Voltage Supply (2.5V or 3.3V)
LCLK_4	12	Configurable clock output 4 at VDDL level
VSS	13	Ground
CLK_5	14	Configurable clock output 5
CLK_6	15	Configurable clock output 6
XOUT[11]	16	Reference Crystal Output

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	–0.5	7.0	V
VDDL	I/O Supply Voltage		7.0	V
T_S	Storage Temperature[2]	–65	100	° C
T_J	Junction Temperature		100	° C
	Digital Inputs	AVSS – 0.3	AVDD + 0.3	V
	Digital Outputs referred to VDD	VSS – 0.3	VDD + 0.3	V
	Digital Outputs referred to VDDL	VSS – 0.3	VDDL +0.3	V
XIN	Electro-Static Discharge	2		kV

Notes:
1. Float XOUT if XIN is externally driven.
2. Rated for 10 years.

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	3.0	3.3	3.6	V
VDDL	Operating Voltage	2.375	2.5	3.6	V
T_A	Ambient Temperature	0		70	° C
C_{LOAD}	Max. Load Capacitance VDD/VDDL=3.3V			15	pF
C_{LOAD}	Max. Load Capacitance VDDL=2.5V			15	pF
P_{max}	Max. Output Power Dissipation			210	° C /W
f_{REF}	Driven Reference Frequency		64.8		MHz

DC Electrical Characteristics

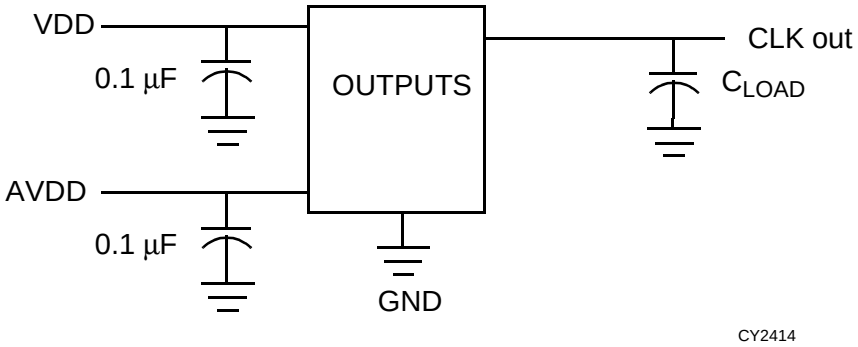
Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	VOH = VDD – 0.5, VDD/VDDL=3.3 V	12	24		mA
I_{OL}	Output Low Current	VOL = 0.5, VDD/VDDL = 3.3V	12	24		mA
I_{OH}	Output High Current	VOH = VDDL– 0.5, VDDL = 2.5V	8	16		mA
I_{OL}	Output Low Current	VOH = VDDL – 0.5, VDDL = 2.5V	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of VDD	0.7			VDD
V_{IL}	Input Low Voltage	CMOS levels, 30% of VDD			0.3	VDD
C_{IN}	Input Capacitance	SPI Pins			7	pF
I_{IZ}	Input Leakage Current	SPI Pins		5		µA
I_{VDD}	Supply Current	AVDD/VDD Current		30	36	mA
I_{VDDL}	Supply Current	VDDL Current (VDDL = 3.6V)		50	60	mA
I_{VDDL}	Supply Current	VDDL Current (VDDL = 2.625V)		35	44	mA

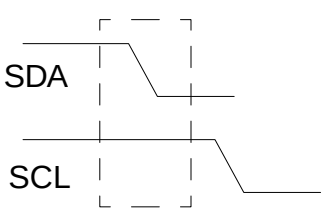
AC Electrical Characteristics (VDD/VDDL = 3.3V)

Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 2; t1/t2 fOUT> 100 MHz, 50% of VDD	40	50	60	%
		Duty Cycle is defined in Figure 2; t1/t2 fOUT<100 MHz, 50% of VDD	45	50	55	%
t3	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of VDD/VDDL	0.8	1.4		V/ns
t4	Falling Edge Slew Rate	Output Clock Fall Time, 80% to 20% of VDD/VDDL	0.8	1.4		V/ns
t9	Clock Jitter	Peak to Peak period jitter			250	ps
t10	PLL Lock Time				3	ms

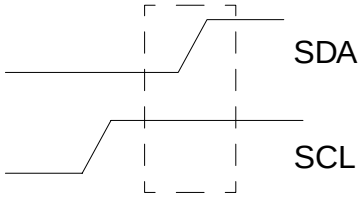
Note:
3. Not 100% tested.

Test Circuit

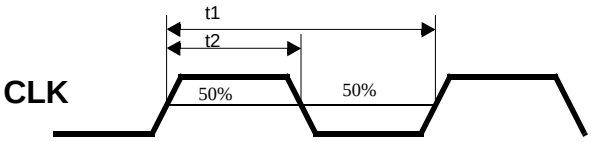




START Condition



STOP Condition



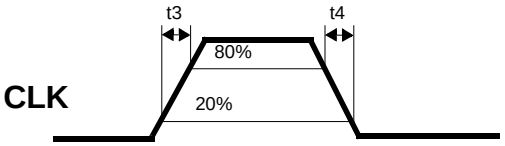


Figure 1. Duty Cycle Definition; DC = t2/t1

Figure 2. Rise and Fall Time Definitions

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
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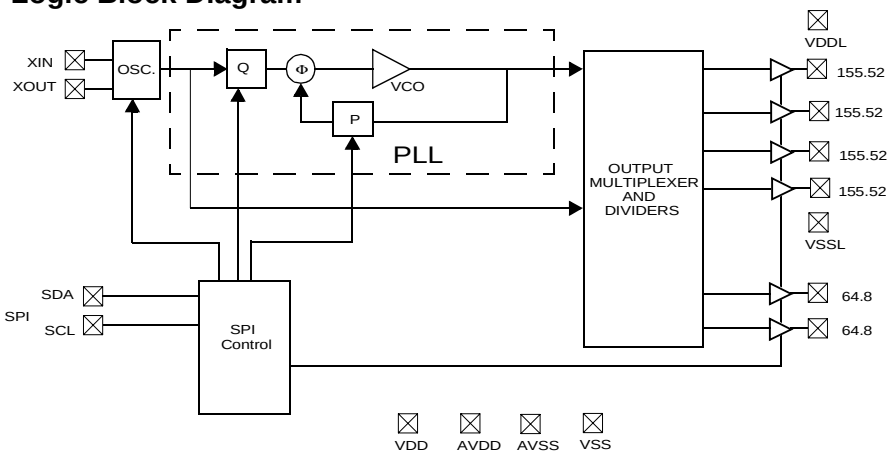

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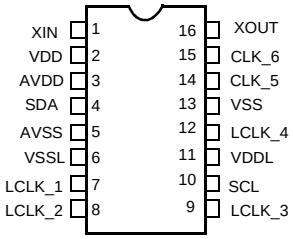

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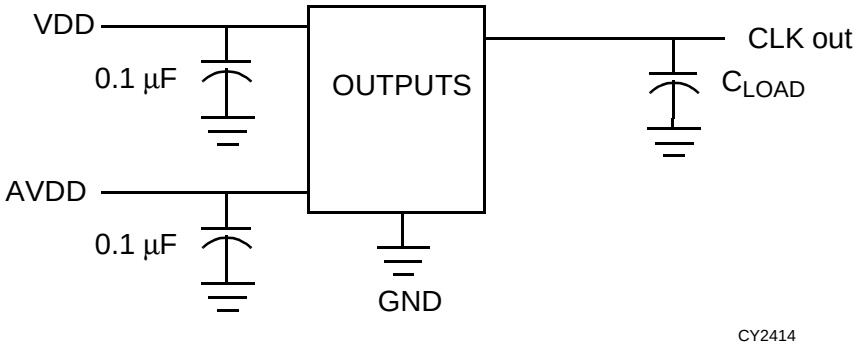

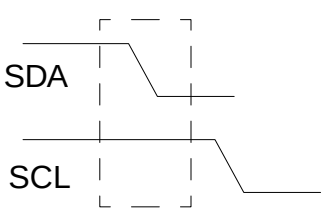

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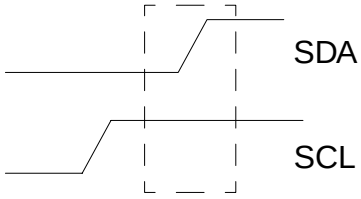

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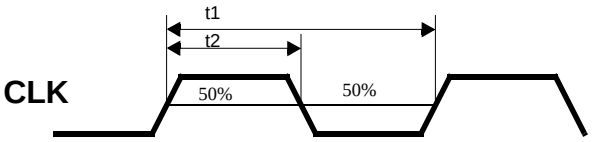

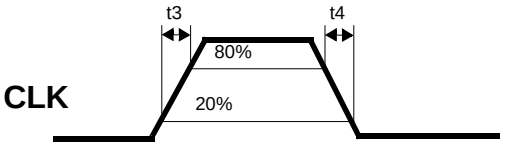

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