PRELIMINARY

CY28258

Memory Clock Buffer for 3 DDR and 2 SDRAM DIMMS

Features

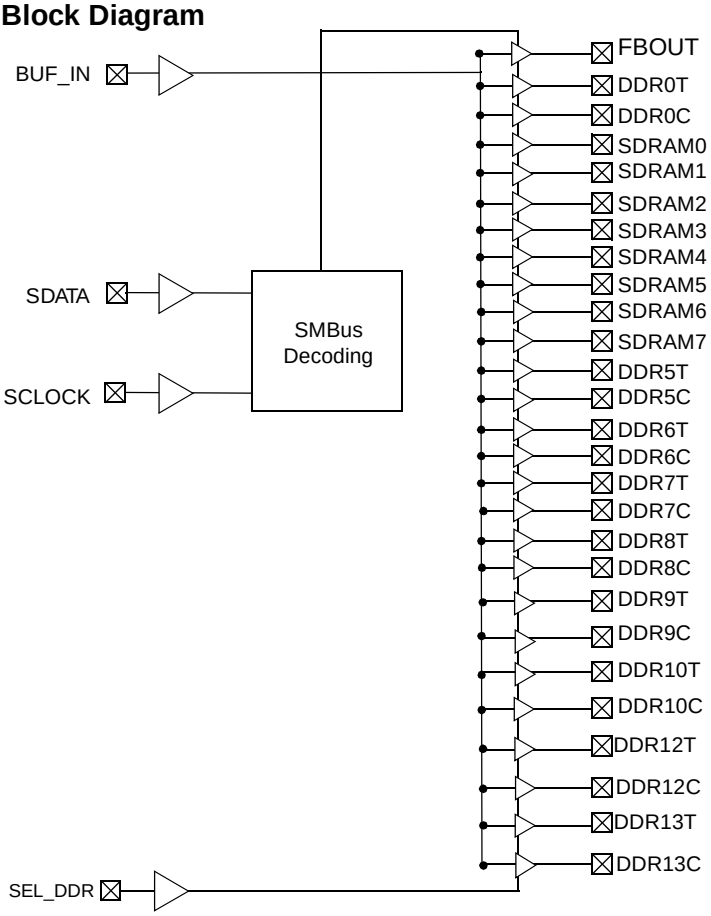
- **One input to 26 output buffer/driver**
- **Supports up to 3 DDR and 2 SDRAM DIMMS**
- **One additional output for feedback**
- **SMBus interface for individual output control**
- **Low skew outputs (< 100 ps)**
- **Supports 266 MHz DDR SDRAM**
- **56-Pin SSOP Package**

Functional Description

The CY28258 is a 3.3V/2.5V buffer designed to distribute high-speed clocks in PC applications.The part has 26 outputs. Designers can configure these outputs to support 3 unbuffered standard DDR DIMMS and 2 SDRAM DIMMS. The CY28258 can be used in conjunction with the W311 or similar clock synthesizer for the VIA Pro 266 chipset.

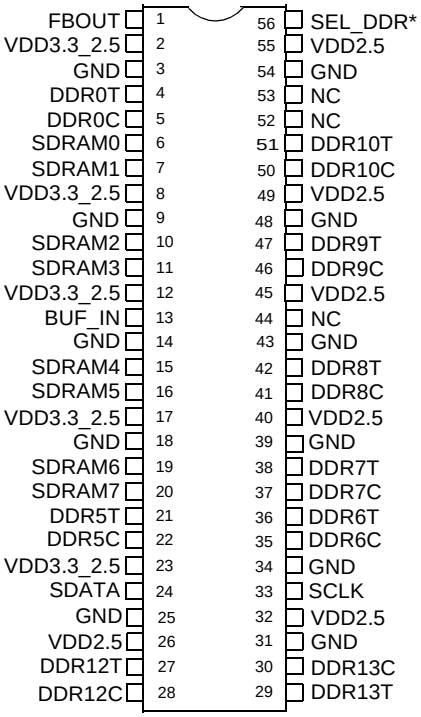
The CY28258 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull up).

Block Diagram



Pin Configuration

SSOP
Top View



Note:

1. Internal 100K pull-up resistors present on inputs marked with *. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

Pin Summary

Name	Pins	Description
SEL_DDR	56	Input to configure for DDR-ONLY mode or STANDARD SDRAM mode. 1 = DDR-ONLY mode. 0 = STANDARD SDRAM mode. When SEL_DDR is pulled high or configured for DDR-ONLY mode, pin 4, 5, 21, 22, 27, 28, 29, 30, 35, 36, 37, 38, 41, 42, 46, 47, 50 and 51 will be configured as DDR outputs. Connect VDD3.3_2.5 to a 2.5V power supply in DDR-ONLY mode. When SEL_DDR is pulled LOW or configured for STANDARD SDRAM output, pin 6, 7, 10, 11, 15, 16, 19 and 20 will be configured as STANDARD SDRAM outputs. Connect VDD3.3_2.5 to a 3.3V power supply in STANDARD SDRAM mode.
SCLK	33	SMBus clock input
SDATA	24	SMBus data input
BUF_IN	13	Reference input from chipset. 2.5V input for DDR-ONLY mode; 3.3V input for STANDARD SDRAM mode.
FBOUT	1	Feedback clock for chipset. Output voltage depends on VDD3.3_2.5V.
NC	44, 52, 53	No Connect.
DDR[0,5:11,12,13]T	4, 21, 27, 29, 36, 38, 42, 47, 51	Clock outputs. These outputs provide copies of BUF_IN.
DDR[0,5:11, 12, 13]C	5, 22, 28, 30, 35, 37, 41, 46, 50	Clock outputs. These outputs provide complementary copies of BUF_IN.
SDRAM[0:7]	6, 7, 10, 11, 15, 16, 19, 20	Clock outputs. These outputs provide copies of BUF_IN. Voltage swing depends on VDD3.3_2.5 power supply.
VDD3.3_2.5	2, 8, 12, 17, 23	Connect to 2.5V power supply when CY28258 is configured for DDR-ONLY mode. Connect to 3.3V power supply, when CY28258 is configured for standard SDRAM mode.
VDD2.5	26, 32, 40, 45, 49, 55	2.5V voltage supply
GND	3, 9, 14, 18, 25, 31, 34, 39, 43, 48, 54	Ground

Note:
2. Internal pull-up resistor to V_{DD} (value > 100 kohms)

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:
  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  .
  .
  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to “0”.
- SMBus Address for the CY28258 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 6: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7	--	Reserved, drive to 0	0
Bit 6	--	Reserved, drive to 0	0
Bit 5	--	Reserved, drive to 0	0
Bit 4	1	FBOUT	1
Bit 3	51, 50	DDR10T, DDR10C	1
Bit 2	47, 46	DDR9T, DDR9C	1
Bit 1	42, 41	DDR8T, DDR8C	1
Bit 0	38, 37	DDR7T, DDR7C	1

Byte 7: Outputs Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description	Default
Bit 7	35,36	DDR6T, DDR6C	1
Bit 6	29, 30	DDR13T, DDR13C	1
Bit 5	27, 28	DDR12T, DDR12C	1
Bit 4	21, 22	DDR5T, DDR5C	1
Bit 3	15,16, 19, 20	SDRAM4:7	1
Bit 2	--	Reserved, drive to 0	0
Bit 1	6, 7, 10, 11	SDRAM0:3	1
Bit 0	4, 5	DDR0T, DDR0C	1

Maximum Ratings

Supply Voltage to Ground Potential .....–0.5 to +7.0V

DC Input Voltage (except BUF_IN) ..... –0.5V to V_{DD}+0.5

Storage Temperature..... –65°C to +150°C

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD3.3	Supply Voltage	3.135		3.465	V
VDD2.5	Supply Voltage	2.375		2.625	V
T_A	Operating Temperature (Ambient Temperature)	0		70	°C
C_{OUT}	Output Capacitance		6		pF
C_{IN}	Input Capacitance		5		pF

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage	For all pins except SMBus			0.8	V
V_{IH}	Input HIGH Voltage		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			50	µA
I_{OH}	Output HIGH Current	V_{DD} = 2.375V V_{OUT} = 1V	–18	–32		mA
I_{OL}	Output LOW Current	V_{DD} = 2.375V V_{OUT} = 1.2V	26	35		mA
V_{OL}	Output LOW Voltage[3]	I_{OL} = 12 mA, V_{DD} = 2.375V			0.6	V
V_{OH}	Output HIGH Voltage[3]	I_{OH} = –12 mA, V_{DD} = 2.375V	1.7			V
I_{DD}	Supply Current[3] (DDR-Only mode)	Unloaded outputs, 133 MHz			400	mA
I_{DD}	Supply Current (DDR-Only mode)	Loaded outputs, 133 MHz			500	mA
I_{DDS}	Supply Current	PWR_DWN# = 0			100	µA
V_{OUT}	Output Voltage Swing	See Test Circuity (Refer to *Figure 1*)	0.7		V_{DD} +0.6	V
V_{OC}	Output Crossing Voltage		(V_{DD}/2) -0.1	V_{DD}/2	(V_{DD}/2) +0.1	V
IN_{DC}	Input Clock Duty Cycle		48		52	%

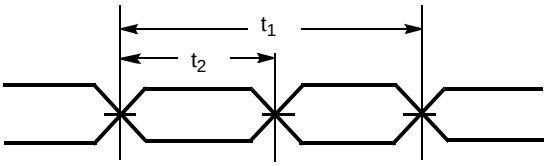
Note:

3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

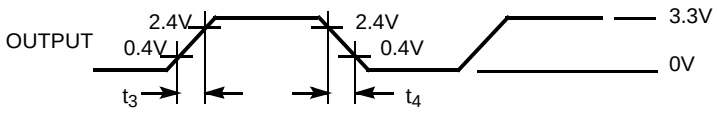
Switching Characteristics[4]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
--	Operating Frequency		66		133	MHz
--	Duty Cycle[3, 5] = $t_2 \div t_1$	Measured at 1.4V for 3.3V outputs Measured at VDD/2 for 2.5V outputs.	IN_{DC} –5%		IN_{DC} +5%	%
t_3	SDRAM Rising Edge Rate[3]	Measured between 0.4V and 2.4V	1.0		2.50	V/ns
t_4	SDRAM Falling Edge Rate[3]	Measured between 2.4V and 0.4V	1.0		2.50	V/ns
t_{3d}	DDR Rising Edge Rate[3]	Measured between 20% to 80% of output (Refer to *Figure 1*)	0.5		1.50	V/ns
t_{4d}	DDR Falling Edge Rate[3]	Measured between 20% to 80% of output (Refer to *Figure 1*)	0.5		1.50	V/ns
t_5	Output to Output Skew[3]	All outputs equally loaded			100	ps
t_6	SDRAM Buffer HH Prop. Delay[3]	Input edge greater than 1V/ns	5		10	ns
t_7	SDRAM Buffer LL Prop. Delay[3]	Input edge greater than 1V/ns	5		10	ns

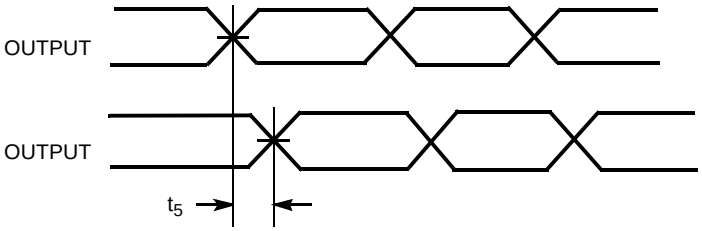
Duty Cycle Timing



All Outputs Rise/Fall Time



Output-Output Skew



Notes:
4. All parameters specified with loaded outputs.
5. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1 V/ns.

SDRAM Buffer HH and LL Propagation Delay

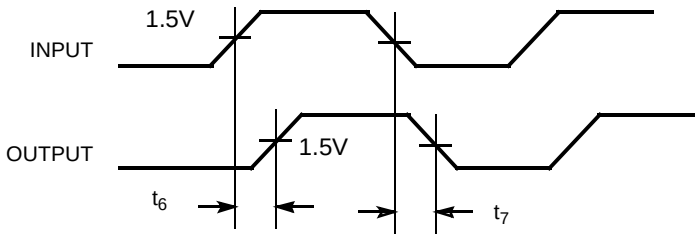


Figure 1 shows the differential clock directly terminated by a 120 Ω resistor

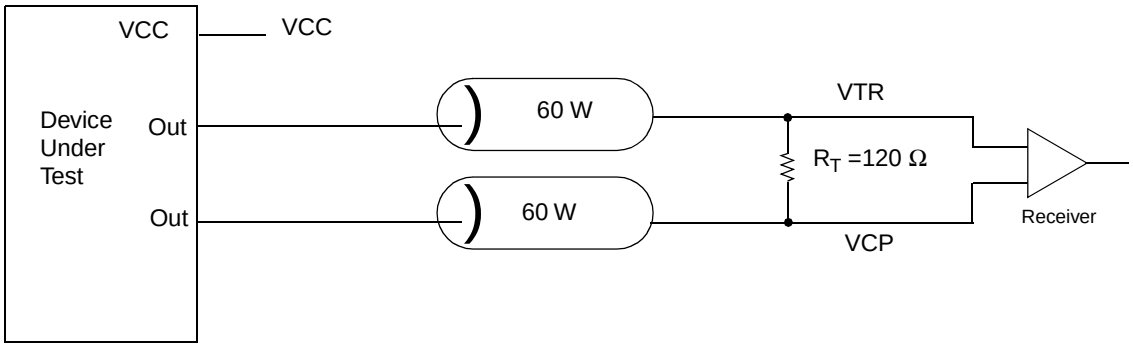


Figure 1. Differential Signal Using Direct Termination Resistor.

Ordering Information

Ordering Code	Package Type	Operating Range
CY28258PVC	56-pin SSOP	Commercial

Document #: 38-01113-**

Package Diagram

56-Lead Shrunk Small Outline Package O56