



CYPRESS

PRELIMINARY

CY28317

# FTG for Mobile VIA PL133T and PLE133T Chipsets

## Features

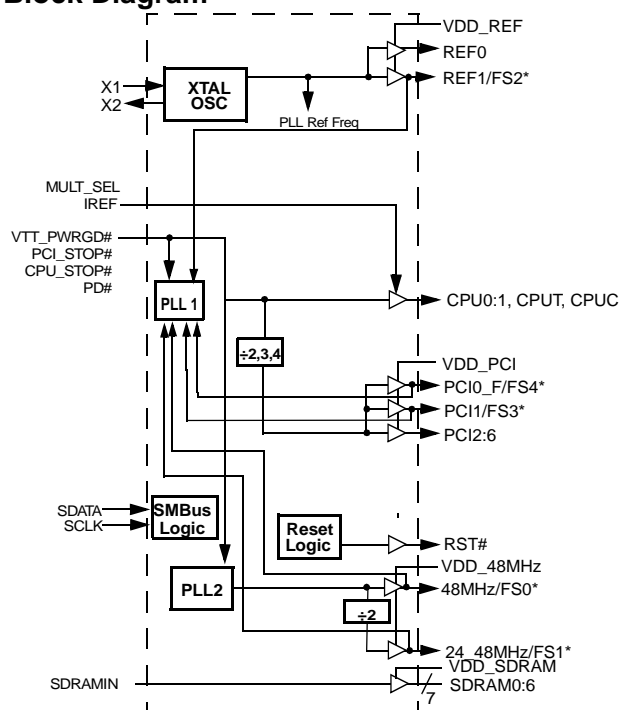
- Single-chip system frequency synthesizer for mobile VIA PL133T and PLE133T chipsets
- Programmable clock output frequency with less than 1 MHz increment
- Integrated fail-safe Watchdog Timer for system recovery
- Automatically switch to HW selected or SW programmed clock frequency when watchdog timer time-out
- Capable of generating system RESET after a Watchdog Timer time-out occurs or a change in output frequency via SMBus interface

- Support SMBus byte read/write and block read/write operations to simplify system BIOS development
- Vendor ID and Revision ID support
- Programmable drive strength for SDRAM and PCI output clocks
- Programmable output skew for CPU, PCI and SDRAM
- Maximized EMI Suppression using Cypress's Spread Spectrum technology
- Available in 48-pin SSOP

## Key Specifications

CPU to CPU Output Skew:..... 175 ps  
 PCI to PCI Output Skew:..... 500 ps  
 SDRAMIN to SDRAM0:12 Delay: ..... 3.7 ns typ.

## Block Diagram



## Pin Configuration<sup>[1]</sup>

GND_CPU	1	48	CPU0
*FS2/REF1	2	47	CPU1
REF0	3	46	VDD_CPU_2.5
VTT_PWRGD#	4	45	VDD_CPU_3.3
GND_REF	5	44	CPUT
X1	6	43	CPUC
X2	7	42	GND_CPU
VDD_PCI	8	41	RST#
*FS4/PCIO_F	9	40	IREF
*FS3/PCI1	10	39	SDRAM6
GND_PCI	11	38	GND_SDRAM
PCI2	12	37	SDRAM0
PCI3	13	36	SDRAM1
PCI4	14	35	VDD_SDRAM
PCI5	15	34	SDRAM2
PCI6	16	33	SDRAM3
SDRAMIN	17	32	GND_SDRAM
*CPU_STOP#	18	31	SDRAM4
*PCI_STOP#	19	30	SDRAM5
*PD#	20	29	VDD_SDRAM
*MULT_SEL	21	28	VDD_48MHz
GND_48MHz	22	27	48MHz/FS0*
SDATA	23	26	24_48MHz/FS1*
	24	25	SCLK

### Note:

1. Signals marked with "\*" have internal pull-up resistors.

**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
CPU0, CPU1	48, 47	O	<b>CPU Clock Output 0 through 1:</b> CPU clocks for processor and chipset.
CPUT, CPUC	44, 43	O	<b>Differential CPU Clock Output:</b> Differential CPU clocks for processor.
PCI2:6	13, 14, 15, 16, 17	O	<b>PCI Clock Outputs 2 through 6:</b> 3.3V 33-MHz PCI clock outputs. Frequency is set by FS0:4 inputs or through serial data interface.
PCI1/FS3	11	I/O	<b>Fixed PCI Clock Output/Frequency Select 3:</b> 3.3V PCI clock outputs. As an output, frequency is set by FS0:4 inputs or through serial data interface. This pin also serves as a power-on strap option to determine device operating frequency as described in 6.
PCI0_F/FS4	10	I/O	<b>Fixed PCI Clock Output/Frequency Select 4:</b> 3.3V Free-running PCI clock outputs. This pin also serves as a power-on strap option to determine device operating frequency as described in 6.
RST#	41	O (open-drain)	<b>Reset# Output:</b> Open drain system reset output.
48MHz/FS0	27	I/O	<b>48-MHz Output/Frequency Select 0:</b> 3.3V 48-MHz non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in 6.
24_48MHz/ FS1	26	I/O	<b>24_48MHz Output/Frequency Select 1:</b> 3.3V 24- or 48-MHz non-spread spectrum output. This pin also serves as a power-on strap option to determine device operating frequency as described in 6.
REF1/FS2	2	I/O	<b>Reference Clock Output 1/Frequency Select 2:</b> 3.3V 14.318-MHz output clock. This pin also serves as a power-on strap option to determine device operating frequency as described in 6.
REF0	3	O	<b>Reference Clock Output 0 :</b> 3.3V 14.318-MHz output clock.
SDRAMIN	18	I	<b>SDRAM Buffer Input Pin:</b> Reference input for SDRAM buffer.
SDRAM0:6	37, 36, 34, 33, 31, 30, 39	O	<b>SDRAM Outputs:</b> These thirteen dedicated outputs provide copies of the signal provided at the SDRAMIN input.
SCLK	25	I	Clock pin for SMBus circuitry.
SDATA	24	I/O	Data pin for SMBus circuitry.
X1	7	I	<b>Crystal Connection or External Reference Frequency Input:</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	8	O	<b>Crystal Connection:</b> An output connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
PD#	21	I	<b>Power Down Control:</b> LVTTTL-compatible input that places the device in power-down mode when held LOW.
CPU_STOP#	19	I	<b>CPU Output Control:</b> 3.3V LVTTTL compatible input that stop CPU0, CPU1, CPUT and CPUC when held LOW.
PCI_STOP#	20	I	<b>PCI Output Control:</b> 3.3V LVTTTL compatible input that stop PCI1:6 when held LOW.
IREF	40	I	<b>Current Reference Input:</b> Current reference for differential CPU output.
MULT_SEL	22	I	<b>CPUT and CPUC Output Control:</b> Control the current multiplier for differential CPU output. Set this pin LOW for 1.0V output swing and set this pin HIGH for 0.7V output swing.
VTT_PWRGD#	4	I	<b>VTT_PWRGD#:</b> 3.3V LVTTTL compatible input that controls the FS0:4 to be latched and enables all the outputs. CY28316 will sample the FS0:4 inputs and enable all the clock outputs after all the VDD become valid and VTT_PWRGD# is held LOW.

**Pin Definitions** (continued)

Pin Name	Pin No.	Pin Type	Pin Description
VDD_REF, VDD_PCI, VDD_SDRAM, VDD_48MHz, VDD_CPU_3.3	5, 9, 28, 29, 35, 45	P	<b>Power Connection:</b> Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48-MHz output, and 24_48-MHz output. Connect to 3.3V supply.
VDD_CPU_2.5	46	P	<b>Power Connection:</b> Power supply for CPU outputs. Connect to 2.5V supply.
GND_REF, GND_PCI, GND_SDRAM, VDD_48MHz, VDD_CPU	1, 6, 12, 23, 32, 38, 42	G	<b>Ground Connections:</b> Connect all ground pins to the common system ground plane.

**Table 1. Swing Select Functions**

Mult0	Board Target Trace/Term Z	Reference R, IREF= VDD/(3*Rr)	Output Current	V <sub>OH</sub> @ Z
0	60Ω	Rr = 221 1% IREF = 5.00 mA	I <sub>OH</sub> = 4*IREF	1.0V @ 50
1	50Ω	Rr = 475 1% IREF = 2.32 mA	I <sub>OH</sub> = 6*IREF	0.7V @ 50

### Serial Data Interface

The CY28317 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

### Data Protocol

The clock driver serial protocol supports byte/word write, byte/word read, block write and block read operations from the

controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. For byte/word write and byte read operations, system controller can access individual indexed byte. The offset of the indexed byte is encoded in the command code.

The definition for the command code is defined as shown in 2.

**Table 2. Command Code Definition**

Bit	Descriptions
7	0 = Block read or block write operation 1 = Byte/Word read or byte/word write operation
6:0	Byte offset for byte/word read or write operation. For block read or write operations, these bits need to be set at '0000000'.

**Table 3. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '00000000' stands for block operation	11:18	Command Code - 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
...	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
...	Data Byte N - 8 bits	47	Acknowledge
...	Acknowledge from slave	48:55	Data byte from slave - 8 bits
...	Stop	56	Acknowledge
		...	Data bytes from slave/Acknowledge
		...	Data byte N from slave - 8 bits
		...	Not Acknowledge
		...	Stop

**Table 4. Word Read and Word Write Protocol**

Word Write Protocol		Word Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxx' stands for byte or word operation bit[6:0] of the command code represents the off-set of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxx' stands for byte or word operation bit[6:0] of the command code represents the off-set of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte low- 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte high - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38	Stop	30:37	Data byte low from slave - 8 bits
		38	Acknowledge
		39:46	Data byte high from slave - 8 bits
		47	NOT acknowledge
		48	Stop

**Table 5. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxx' stands for byte operation bit[6:0] of the command code represents the off-set of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxx' stands for byte operation bit[6:0] of the command code represents the off-set of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

**CY28317 Serial Configuration Map**

1. The serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a "0" level.
3. All register bits labeled "Write with 1" must be written to one during initialization.

**Byte 0: Control Register 0**

Bit	Pin#	Name	Default	Description
Bit 7	--	Spread Select1	0	See definition in Bit[0]
Bit 6	--	SEL2	0	See Table 6
Bit 5	--	SEL1	0	See Table 6
Bit 4	--	SEL0	0	See Table 6
Bit 3	--	FS_Override	0	0 = Select operating frequency by FS[4:0] input pins 1 = Select operating frequency by SEL[4:0] settings
Bit 2	--	SEL4	0	See Table 6
Bit 1	--	SEL3	0	See Table 6
Bit 0	--	Spread Select0	0	'00' = OFF '01' = - 0.5% '10' = ± 0.5% '11' = ± 0.25%

**Byte 1: Control Register 1**

Bit	Pin#	Name	Default	Description
Bit 7	10	Latched FS4 input	X	Latched FS[4:0] inputs. These bits are read only.
Bit 6	11	Latched FS3 input	X	
Bit 5	2	Latched FS2 input	X	
Bit 4	26	Latched FS1 input	X	
Bit 3	27	Latched FS0 input	X	
Bit 2	48	CPU0	1	(Active/Inactive)
Bit 1	47	CPU1	1	(Active/Inactive)
Bit 0	44, 43	CPUT, CPUC	1	(Active/Inactive)

**Byte 2: Control Register 2**

Bit	Pin#	Name	Default	Description
Bit 7	39	SDRAM6	1	(Active/Inactive)
Bit 6	10	PCI0_F	1	(Active/Inactive)
Bit 5	17	PCI6	1	(Active/Inactive)
Bit 4	16	PCI5	1	(Active/Inactive)
Bit 3	15	PCI4	1	(Active/Inactive)
Bit 2	14	PCI3	1	(Active/Inactive)
Bit 1	13	PCI2	1	(Active/Inactive)
Bit 0	11	PCI1	1	(Active/Inactive)

**Byte 3: Control Register 3**

Bit	Pin#	Name	Default	Description
Bit 7	--	Reserved	1	Reserved
Bit 6	--	SEL_48MHz	0	0 = 24 MHz 1 = 48 MHz
Bit 5	27	48MHz	1	(Active/Inactive)
Bit 4	26	24_48MHz	1	(Active/Inactive)
Bit 3	--	Reserved	1	Reserved
Bit 2	31, 30	SDRAM4:5	1	(Active/Inactive)
Bit 1	34, 33	SDRAM2:3	1	(Active/Inactive)
Bit 0	37, 36	SDRAM0:1	1	(Active/Inactive)

**Byte 4: Control Register 4**

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	0	Reserved
Bit 0	-	Reserved	0	Reserved

**Byte 5: Control Register 5**

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	CPUT & CPUC Stop Control	0	0 = CPUT & CPUC will be stopped when CPU_STOP# is active 1 = CPUT & CPUC will NOT be stopped when CPU_STOP# is active
Bit 1	2	REF1	1	(Active/Inactive)
Bit 0	3	REF0	1	(Active/Inactive)

**Byte 6: Watchdog Timer Register**

Bit	Name	Default	Pin Description
Bit 7	PCI_Skew1	0	PCI skew control 00 = Normal 01 = -500 ps 10 = Reserved 11 = +500 ps
Bit 6	PCI_Skew0	0	

**Byte 6: Watchdog Timer Register (continued)**

Bit	Name	Default	Pin Description
Bit 5	WD_TIMER4	1	These bits store the time-out value of the Watchdog Timer. The scale of the timer is determined by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0," it will set the WD_TO_STATUS bit and generate Reset if RST_EN_WD is enabled.
Bit 4	WD_TIMER3	1	
Bit 3	WD_TIMER2	1	
Bit 2	WD_TIMER1	1	
Bit 1	WD_TIMER0	1	
Bit 0	WD_PRE_SCALER	0	0 = 150 ms 1 = 2.5 sec

**Byte 7: Control Register 7**

Bit	Pin#	Name	Default	Pin Description
Bit 7	--	Reserved	0	Reserved
Bit 6	25	24_48MHz_DRV	1	0 = Norm, 1 = High Drive
Bit 5	26	48MHz_DRV	1	0 = Norm, 1 = High Drive
Bit 4	--	Reserved	0	Reserved
Bit 3	--	Reserved	0	Reserved
Bit 2	--	Reserved	0	Reserved
Bit 1	--	Reserved	0	Reserved
Bit 0	--	Reserved	0	Reserved

**Byte 8: Vendor ID & Revision ID Register (Read Only)**

Bit	Name	Default	Pin Description
Bit 7	Revision_ID3	0	Revision ID bit[3]
Bit 6	Revision_ID2	0	Revision ID bit[2]
Bit 5	Revision_ID1	0	Revision ID bit[1]
Bit 4	Revision_ID0	0	Revision ID bit[0]
Bit 3	Vendor_ID3	1	Bit[3] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 2	Vendor_ID2	0	Bit[2] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 1	Vendor_ID1	0	Bit[1] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 0	Vendor_ID0	0	Bit[0] of Cypress Semiconductor's Vendor ID. This bit is read only.

**Byte 9: System RESET and Watchdog Timer Register**

Bit	Name	Default	Pin Description
Bit 7	SDRAM_DRV	0	SDRAM clock output drive strength 0 = Normal 1 = High Drive
Bit 6	PCI_DRV	0	PCI clock output drive strength 0 = Normal 1 = High Drive
Bit 5	Reserved	0	Reserved
Bit 4	RST_EN_WD	0	This bit will enable the generation of a Reset pulse when a Watchdog Timer time-out occurs. 0 = Disabled 1 = Enabled



**Byte 9: System RESET and Watchdog Timer Register (continued)**

Bit	Name	Default	Pin Description
Bit 3	RST_EN_FC	0	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled
Bit 2	WD_TO_STATUS	0	Watchdog Timer Time-out Status bit 0 = No time-out occurs (READ); Ignore (WRITE) 1 = Time-out occurred (READ); Clear WD_TO_STATUS (WRITE)
Bit 1	WD_EN	0	0 = Stop and re-load Watchdog Timer. Unlock CY28317 from recovery frequency mode. 1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs. <b>Note:</b> CY28317 will generate system reset, re-load a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog Timer time-out occurs. Under recovery frequency mode, CY28317 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock CY28317 from its recovery frequency mode by clearing the WD_EN bit.
Bit 0	CPU0:1_DRV	0	CPU0:1 clock output drive strength 0 = Normal 1 = High Drive

**Byte 10: Skew Control Register**

Bit	Name	Default	Description
Bit 7	CPU0:1_Skew2	0	CPU 0:1 output skew control 000 = Normal 001 = -150 ps 010 = -300 ps 011 = -450 ps 100 = +150 ps 101 = +300 ps 110 = +450 ps 111 = +600 ps
Bit 6	CPU0:1_Skew1	0	
Bit 5	CPU0:1_Skew0	0	
Bit 4	Reserved	0	
Bit 3	Reserved	0	Reserved
Bit 2	Reserved	0	Reserved
Bit 1	CPUT&C_Skew1	0	CPUT and CPUC output skew control 00 = Normal 01 = -150 ps 10 = +150 ps 11 = +300 ps
Bit 0	CPUT&C_Skew0	0	

**Byte 11: Recovery Frequency N-Value Register**

Bit	Name	Default	Pin Description
Bit 7	ROCV_FREQ_N7	0	<p>If ROCV_FREQ_SEL is set, CY28317 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs.</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU and PCI. When it is cleared, CY28317 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28317 will use the frequency ratio stated in the SEL[4:0] register.</p> <p>CY28317 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.</p> <p>CY28317 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.</p>
Bit 6	ROCV_FREQ_N6	0	
Bit 5	ROCV_FREQ_N5	0	
Bit 4	ROCV_FREQ_N4	0	
Bit 3	ROCV_FREQ_N3	0	
Bit 2	ROCV_FREQ_N2	0	
Bit 1	ROCV_FREQ_N1	0	
Bit 0	ROCV_FREQ_N0	0	

**Byte 12: Recovery Frequency M-Value Register**

Bit	Name	Default	Pin Description
Bit 7	ROCV_FREQ_SEL	0	<p>ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog Timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.</p> <p>0 = From latched FS[4:0] 1 = From the settings of ROCV_FREQ_N[7:0] &amp; ROCV_FREQ_M[6:0]</p>
Bit 6	ROCV_FREQ_M6	0	<p>If ROCV_FREQ_SEL is set, CY28317 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs.</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM and PCI. When it is cleared, CY28317 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28317 will use the frequency ratio stated in the SEL[4:0] register.</p> <p>CY28317 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.</p> <p>CY28317 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.</p>
Bit 5	ROCV_FREQ_M5	0	
Bit 4	ROCV_FREQ_M4	0	
Bit 3	ROCV_FREQ_M3	0	
Bit 2	ROCV_FREQ_M2	0	
Bit 1	ROCV_FREQ_M1	0	
Bit 0	ROCV_FREQ_M0	0	

**Byte 13: Programmable Frequency Select N-Value Register**

Bit	Name	Default	Pin Description
Bit 7	CPU_FSEL_N7	0	<p>If Prog_Freq_EN is set, CY28317 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated.</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM and PCI. When it is cleared, CY28317 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28317 will use the frequency ratio stated in the SEL[4:0] register.</p> <p>CY28317 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.</p>
Bit 6	CPU_FSEL_N6	0	
Bit 5	CPU_FSEL_N5	0	
Bit 4	CPU_FSEL_N4	0	
Bit 3	CPU_FSEL_N3	0	
Bit 2	CPU_FSEL_N2	0	
Bit 1	CPU_FSEL_N1	0	
Bit 0	CPU_FSEL_N0	0	

**Byte 14: Programmable Frequency Select M-Value Register**

Bit	Name	Default	Description
Bit 7	Pro_Freq_EN	0	Programmable output frequencies enabled 0 = Disabled 1 = Enabled
Bit 6	CPU_FSEL_M6	0	If Prog_Freq_EN is set, CY28317 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM and PCI. When it is cleared, CY28317 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28317 will use the frequency ratio stated in the SEL[4:0] register. CY28317 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.
Bit 5	CPU_FSEL_M5	0	
Bit 4	CPU_FSEL_M4	0	
Bit 3	CPU_FSEL_M3	0	
Bit 2	CPU_FSEL_M2	0	
Bit 1	CPU_FSEL_M1	0	
Bit 0	CPU_FSEL_M0	0	

**Byte 15: Reserved Register**

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Vendor test Mode	0	Reserved. Write with '0'
Bit 1	-	Vendor test mode	1	Test mode. Write with '1'
Bit 0	-	Vendor test mode	1	Test mode. Write with '1'

**Byte 16: Reserved Register**

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	0	Reserved

**Byte 17: Reserved Register**

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Reserved	0	Reserved
Bit 5	-	Reserved	0	Reserved
Bit 4	-	Reserved	0	Reserved

**Byte 17: Reserved Register** (continued)

Bit	Pin#	Name	Default	Description
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	-	Reserved	0	Reserved

**Table 6. Additional Frequency Selections through Serial Data Interface Data Bytes**

Input Conditions					Output Frequency		PLL Gear Constant (G)
FS4 SEL4	FS3 SEL3	FS2 SEL2	FS1 SEL1	FS0 SEL0	CPU	PCI	
0	0	0	0	0	200.0	33.3	48.000741
0	0	0	0	1	190.0	38.0	48.000741
0	0	0	1	0	180.0	36.0	48.000741
0	0	0	1	1	170.0	34.0	48.000741
0	0	1	0	0	166.0	33.2	48.000741
0	0	1	0	1	160.0	32.0	48.000741
0	0	1	1	0	150.0	37.5	48.000741
0	0	1	1	1	145.0	36.3	48.000741
0	1	0	0	0	140.0	35.0	48.000741
0	1	0	0	1	136.0	34.0	48.000741
0	1	0	1	0	130.0	32.5	48.000741
0	1	0	1	1	124.0	31.0	48.000741
0	1	1	0	0	67.2	33.6	48.000741
0	1	1	0	1	100.8	33.6	48.000741
0	1	1	1	0	118.0	39.3	48.000741
0	1	1	1	1	134.4	33.6	48.000741
1	0	0	0	0	67.0	33.5	48.000741
1	0	0	0	1	100.5	33.5	48.000741
1	0	0	1	0	115.0	38.3	48.000741
1	0	0	1	1	134.0	33.5	48.000741
1	0	1	0	0	66.8	33.4	48.000741
1	0	1	0	1	100.2	33.4	48.000741
1	0	1	1	0	110.0	36.7	48.000741
1	0	1	1	1	133.6	33.4	48.000741
1	1	0	0	0	105.0	35.0	48.000741
1	1	0	0	1	90.0	30.0	48.000741
1	1	0	1	0	85.0	28.3	48.000741
1	1	0	1	1	78.0	39.0	48.000741
1	1	1	0	0	66.6	33.3	48.000741
1	1	1	0	1	100.0	33.3	48.000741
1	1	1	1	0	75.0	37.5	48.000741
1	1	1	1	1	133.3	33.3	48.000741

## Programmable Output Frequency, Watchdog Timer and Recovery Output Frequency Functional Description

The Programmable Output Frequency feature allows users to generate any CPU output frequency from the range of 50 MHz to 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism when the system hangs or getting unstable. System BIOS or other control software can enable the Watchdog timer before they attempt to make a frequency change. If the system hangs and a Watchdog Timer time-out occurs, a system reset will be generated and a recovery frequency will be activated.

All the related registers are summarized in 7.

**Table 7. Register Summary**

Name	Description
Pro_Freq_EN	<p>Programmable output frequencies enabled 0 = Disabled (default) 1 = Enabled</p> <p>When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If FS_Override bit is set, programmed value of SEL[4:0] will be used.</p> <p>When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs</p>
FS_Override	<p>When Pro_Freq_EN is cleared or disabled, 0 = Select operating frequency by FS input pins (default) 1 = Select operating frequency by SEL bits in SMBus control bytes</p> <p>When Pro_Freq_EN is set or enabled, 0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default) 1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes</p>
CPU_FSEL_N, CPU_FSEL_M	<p>When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determines the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU and PCI. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes.</p>
ROCV_FREQ_SEL	<p>ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog Timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL. 0 = From latched FS[4:0] 1 = From the settings of ROCV_FREQ_N[7:0] &amp; ROCV_FREQ_M[6:0]</p>
ROCV_FREQ_N[7:0], ROCV_FREQ_M[6:0]	<p>When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU and SDRAM. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.</p> <p>The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.</p>

Name	Description
WD_EN	0 = Stop and re-load Watchdog Timer. Unlock CY28317 from recovery frequency mode. 1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs. <b>Note:</b> CY28317 will generate system reset, reload a recovery frequency, and lock itself into a recovery frequency mode after a Watchdog Timer time-out occurs. Under recovery frequency mode, CY28317 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock CY28317 from its recovery frequency mode by clearing the WD_EN bit.
WD_TO_STATUS	Watchdog Timer Time-out Status bit 0 = No time-out occurs (READ); Ignore (WRITE) 1 = Time-out occurred (READ); Clear WD_TO_STATUS (WRITE)
WD_TIMER[4:0]	These bits store the time-out value of the Watchdog Timer. The scale of the timer is determine by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0," it will set the WD_TO_STATUS bit.
WD_PRE_SCALER	0 = 150 ms 1 = 2.5 sec
RST_EN_WD	This bit will enable the generation of a Reset pulse when a watchdog timer time-out occurs. 0 = Disabled 1 = Enabled
RST_EN_FC	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled

#### How to program CPU output frequency?

When the programmable output frequency feature is enabled (Pro\_Freq\_EN bit is set), the CPU output frequency is determined by the following equation:

$$F_{cpu} = G * (N+3)/(M+3)$$

"N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

"G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 4*.

The ratio of (N+3) and (M+3) need to be greater than "1"  $[(N+3)/(M+3) > 1]$ .

The following table lists set of N and M values for different frequency output ranges. This example use a fixed value for the M-Value Register and select the CPU output frequency by changing the value of the N-Value Register.

**Table 8. Examples of N and M Value for Different CPU Frequency Range**

Frequency Ranges	Gear Constants	Fixed Value for M-Value Register	Range of N-Value Register for Different CPU Frequency
50 MHz – 129 MHz	48.00741	93	97 – 255
130 MHz – 248 MHz	48.00741	45	127 – 245

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability..

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C
$T_A$	Operating Temperature	0 to +70	°C
$ESD_{PROT}$	Input ESD Protection	2 (min.)	kV

## DC Electrical Characteristics: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{DDQ3} = 3.3\text{V} \pm 5\%$ <sup>[2]</sup>

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit	
Supply Current							
I <sub>DD3</sub>	3.3V Supply Current	V <sub>DD</sub> = 3.465V, FCPU = 133 MHz		250		mA	
I <sub>DDPD3</sub>	3.3V Shut down Current	V <sub>DD</sub> = 3.465V		25		mA	
Logic Inputs							
V <sub>IL</sub>	Input Low Voltage		GND – 0.3		0.8	V	
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>DD</sub> + 0.3	V	
I <sub>IL</sub>	Input Low Current <sup>[3]</sup>				–25	μA	
I <sub>IH</sub>	Input High Current <sup>[3]</sup>				10	μA	
Clock Outputs							
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 1 mA			50	mV	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = –1 mA	3.1			V	
I <sub>OL</sub>	Output Low Current	PCI0:5	V <sub>OL</sub> = 1.5V	70	110	135	mA
		REF0:1	V <sub>OL</sub> = 1.5V	50	70	100	mA
		48 MHz	V <sub>OL</sub> = 1.5V	50	70	100	mA
		24 MHz	V <sub>OL</sub> = 1.5V	50	70	100	mA
		SDRAM	V <sub>OL</sub> = 1.5V	70	110	135	mA
I <sub>OH</sub>	Output High Current	PCI0:5	V <sub>OH</sub> = 1.5V	70	110	135	mA
		REF0:1	V <sub>OH</sub> = 1.5V	50	70	100	mA
		48 MHz	V <sub>OH</sub> = 1.5V	50	70	100	mA
		24 MHz	V <sub>OH</sub> = 1.5V	50	70	100	mA
		SDRAM	V <sub>OH</sub> = 1.5V	70	110	135	mA

### Notes:

- All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
- CY28317 logic inputs (except FS3) have internal pull-up devices (pull-ups not full CMOS level). Logic input FS3 has an internal pull-down device.



**DC Electrical Characteristics:**  $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ <sup>[2]</sup> (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
<b>Crystal Oscillator</b>						
$V_{TH}$	X1 Input Threshold Voltage <sup>[4]</sup>	$V_{DDQ3} = 3.3\text{V}$		1.65		V
$C_{LOAD}$	Load Capacitance, Imposed on External Crystal <sup>[5]</sup>			18		pF
$C_{IN,X1}$	X1 Input Capacitance <sup>[6]</sup>	Pin X2 unconnected		TBD		pF
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance	Except X1 and X2			5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

**AC Electrical Characteristics**
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $f_{XTL} = 14.31818\text{ MHz}$ 

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum is disabled.

**CPU Clock Outputs (CPUT0, CPUC0, CPU\_CS)<sup>[7]</sup>**

Parameter	Description	Test Condition/Comments	CPU = 100 MHz			CPU = 133 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_R$	Output Rise Edge Rate				2.0			2.0	%
$t_F$	Output Fall Edge Rate				2.0			2.0	%
$t_D$	Duty Cycle	Measured at 50% point	45		55	45		55	%
$t_{JC}$	Jitter, Cycle to Cycle				250			250	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.		3			3		ms
$Z_O$	AC Output Impedance	$V_O = V_X$		50			50		$\Omega$

**Notes:**

- X1 input threshold voltage (typical) is  $V_{DD}/2$ .
- The CY28317 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
- X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
- Determined as a fraction of  $2^*$  ( $T_{rp} - T_{rn}$ ). Where  $T_{rp}$  is a rising edge and  $T_{rn}$  is an intersection falling edge.

**PCI Clock Outputs, PCI (Lump Capacitance Test Load = 30 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$t_P$	Period	Measured on rising edge at 1.5V	30			ns
$t_H$	High Time	Duration of clock cycle above 2.4V	12			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	12			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.5V			500	ps
$t_O$	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		$\Omega$

**REF Clock Outputs (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$f$	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		$\Omega$

**48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$f$	Frequency, Actual	Determined by PLL divider ratio (see m/n below)	48.008			MHz
$f_D$	Deviation from 48 MHz	$(48.008 - 48)/48$	+167			ppm
m/n	PLL Ratio	$(14.31818 \text{ MHz} \times 57/17 = 48.008 \text{ MHz})$	57/17			
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		$\Omega$

**24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

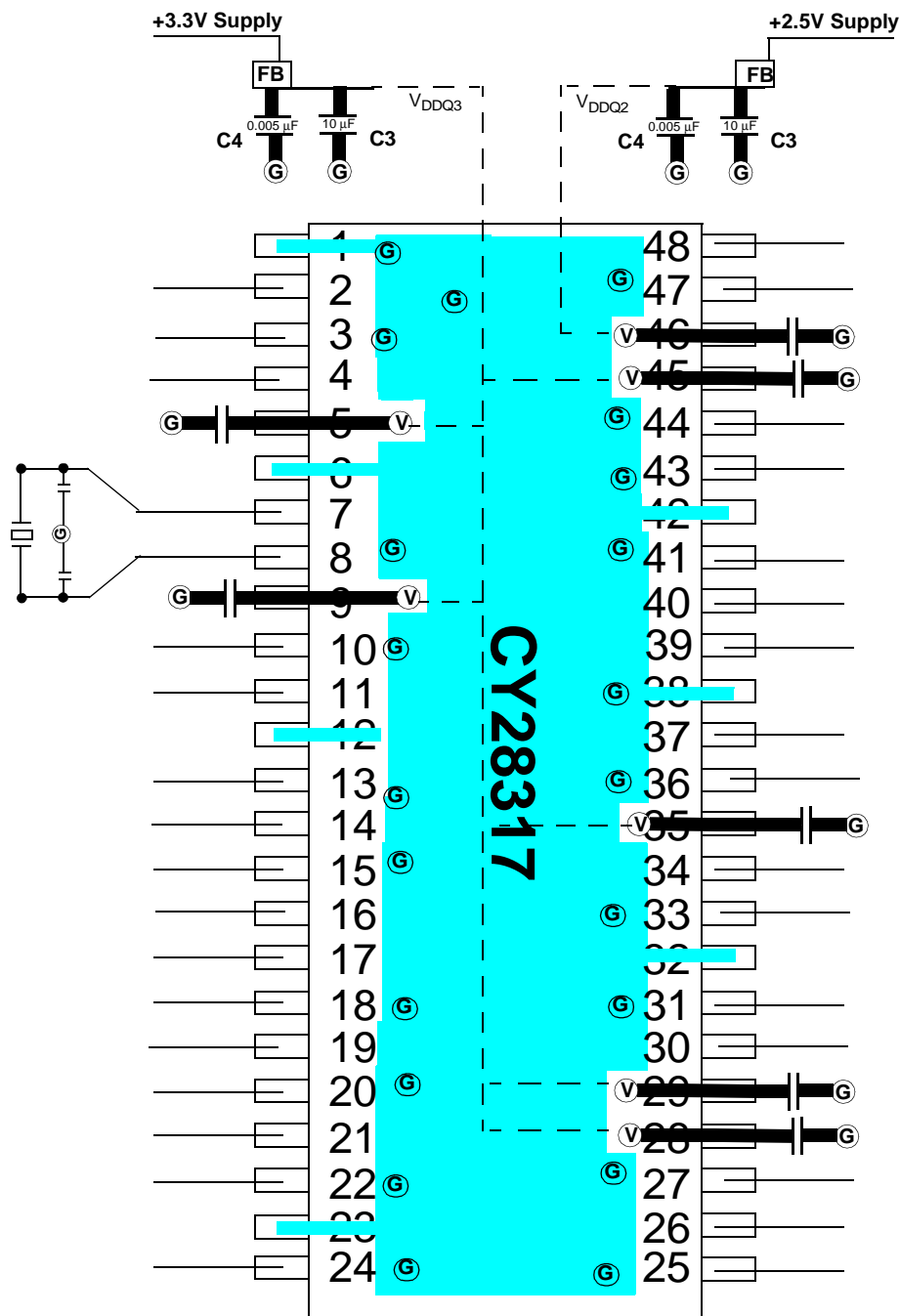
Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)	24.004			MHz
f <sub>D</sub>	Deviation from 24 MHz	(24.004 – 24)/24	+167			ppm
m/n	PLL Ratio	(14.31818 MHz x 57/34 = 24.004 MHz)	57/34			
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z <sub>O</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY28317	PVC	48-pin SSOP (300 mils)	Commerical

Document #: 38-01150-\*\*

## Layout Diagram

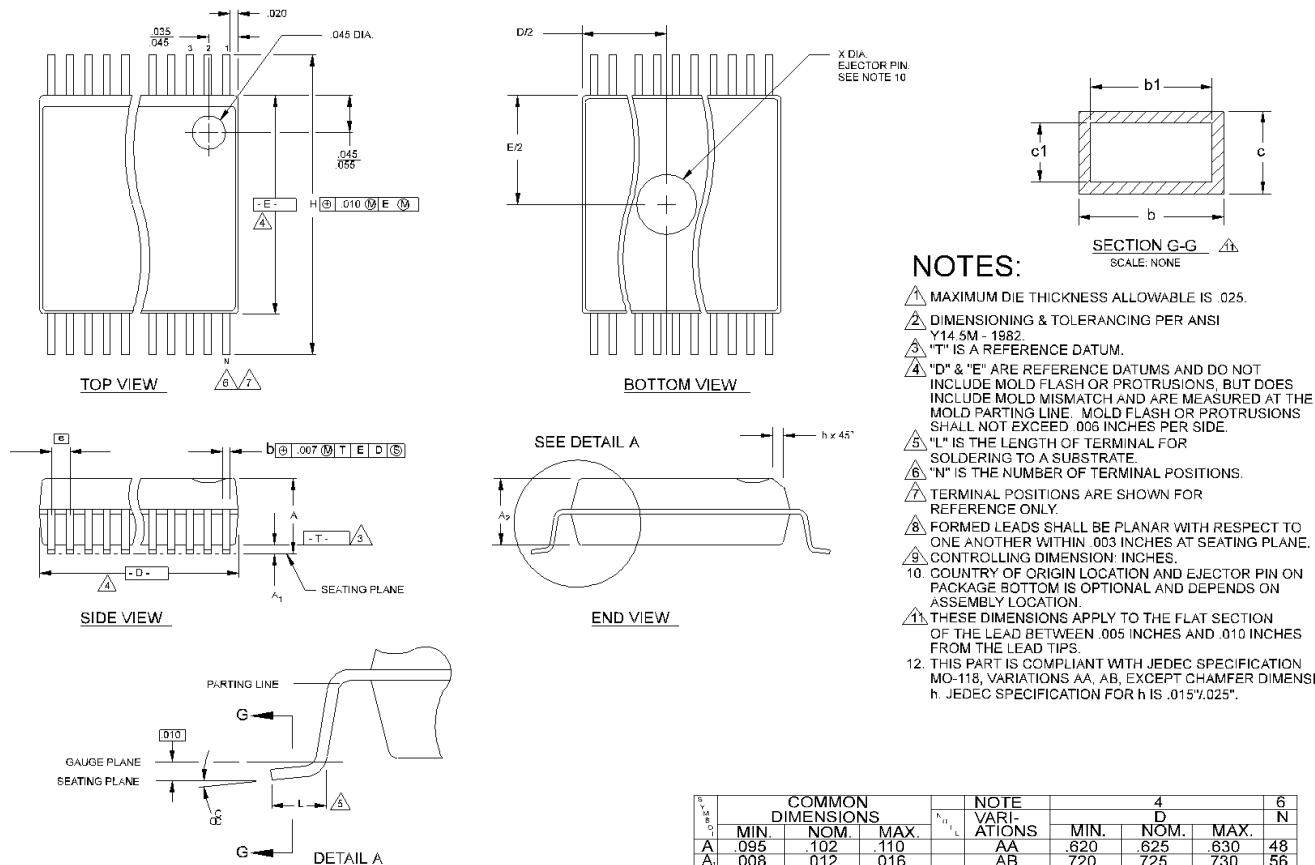


FB = Dale ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB2012L-120

Ceramic Caps C3 = 10–22 μF C4 = 0.005 μF C6 = 0.01 μF

⊗ = VIA to GND plane layer ⊙ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors

**Package Diagram**
**48-Pin Small Shrink Outline Package (SSOP, 300 mils)**

**Summary of nominal dimensions in inches:**

**Body Width: 0.296**  
**Lead Pitch: 0.025**  
**Body Length: 0.625**  
**Body Height: 0.102**

DIMENSION	COMMON DIMENSIONS			NOTE	4			6
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AA	.620	.625	.630	48
A <sub>1</sub>	.008	.012	.016	AB	.720	.725	.730	56
A <sub>2</sub>	.088	.090	.092					
b	.008	.010	.0135					
b <sub>1</sub>	.008	.010	.012					
c	.005	-	.010					
c <sub>1</sub>	.005	.006	.0085					
D	SEE VARIATIONS			4				
E	.292	.296	.299					
e	.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	SEE VARIATIONS			6				
X	.085	.093	.100	10				
α	0°	5°	8°					

THIS TABLE IN INCHES

DIMENSION	COMMON DIMENSIONS			NOTE	4			6
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	AA	15.75	15.88	16.00	48
A <sub>1</sub>	0.20	0.31	0.41	AB	18.29	18.42	18.54	56
A <sub>2</sub>	2.24	2.29	2.34					
b	0.203	0.254	0.343					
b <sub>1</sub>	0.203	0.254	0.305					
c	0.127	-	0.254					
c <sub>1</sub>	0.127	0.152	0.216					
D	SEE VARIATIONS			4				
E	7.42	7.52	7.59					
e	0.635 BSC							
H	10.16	10.31	10.41					
h	0.25	0.33	0.41					
L	0.61	0.81	1.02					
N	SEE VARIATIONS			6				
X	2.16	2.36	2.54	10				
α	0°	5°	8°					

THIS TABLE IN MILLIMETERS