



CYPRESS

Preliminary

CY28319

## FTG for VIA Pro-266T DDR Chipset

### Features

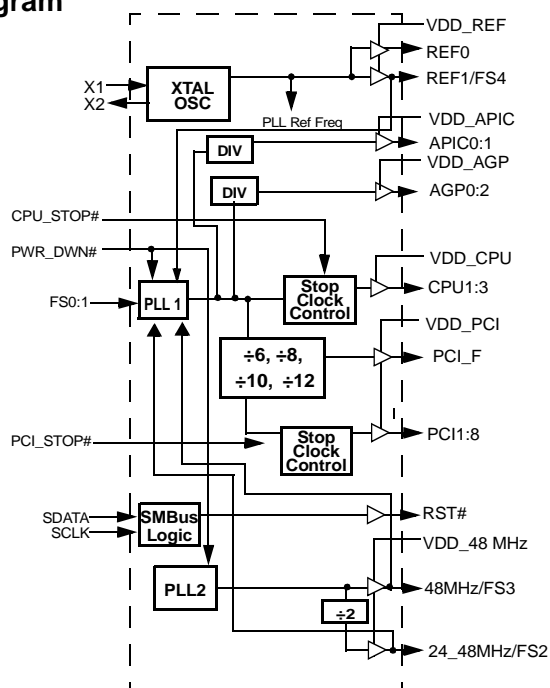
- Maximized EMI Suppression using Cypress's Spread Spectrum Technology
- System frequency synthesizer for VIA Pro-266T
- Programmable clock output frequency with less than 1 MHz increment
- Integrated fail-safe Watchdog Timer for system recovery
- Automatically switch to HW selected or SW programmed clock frequency when Watchdog Timer time-out
- Capable of generating system RESET after a Watchdog Timer time-out occurs or a change in output frequency via SMBus interface
- Support SMBus byte read/write and block read/write operations to simplify system BIOS development
- Vendor ID and Revision ID support
- Programmable drive strength for CPU and PCI output clocks
- Programmable output skew between CPU, AGP and PCI

- Supports Intel® Celeron® and Pentium® III class processor
- Three copies of CPU output
- Nine copies of PCI output
- One 48-MHz output for USB
- One 24-MHz or 48-MHz output for SIO
- Two buffered reference outputs
- Three copies of APIC output
- Supports frequencies up to 200 MHz
- SMBus interface for programming
- Power management control inputs
- Available in 48-pin SSOP

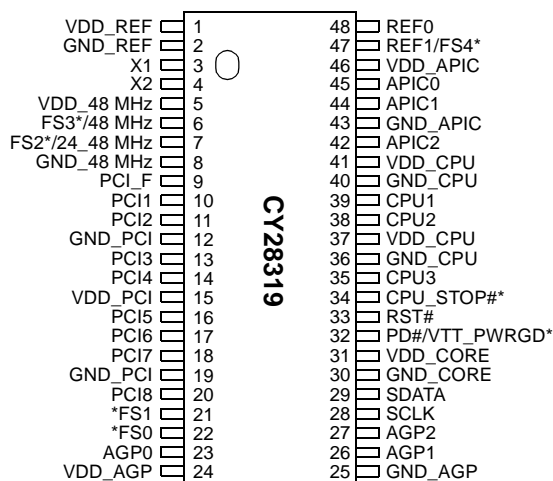
### Key Specifications

CPU Cycle-to-Cycle Jitter:	250 ps
CPU to CPU Output Skew:	175 ps
PCI Cycle to Cycle Jitter:	500 ps
PCI to PCI Output Skew:	500 ps

### Block Diagram



### Pin Configuration<sup>[1]</sup>



#### Note:

1. Signals marked with '\*' have internal pull-up resistors.

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**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
RST#	33	O (open-drain)	<b>System Reset Output:</b> Open-drain system reset output.
CPU1:3	39, 38, 35	O	<b>CPU Clock Output:</b> Frequency is set by the FS0:4 input or through serial input interface. The CPU1:3 outputs are gated by the CLK_STOP# input.
CPU_STOP#	34	I	<b>CPU Output Control:</b> 3.3V LVTTL-compatible input that stop CPU1:3.
PCI1:8	10, 11, 13, 14, 16, 17, 18, 20	O	<b>PCI Clock Outputs 1 through 8:</b> Frequency is set by FS0:4 inputs or through serial input interface; see Table 5 for details. PCI1:8 outputs are gated by the PCI_STOP# input.
PD#/VTT_PWRGD*	32	I	<b>PD# or VTT_PWRGD Input:</b> This pin can be used as either a Power Down input function or a VTT_PWRGD input for Intel VRM 8.5 implementation.
PCI_F	9	O	<b>Free-Running PCI Clock Output:</b> Frequency is set by FS0:4 inputs or through serial input interface; see Table 5 for details.
APIC0:2	45, 44, 42	O	<b>APIC Clock Output:</b> APIC clock outputs.
48MHz/FS3	6	I/O	<b>48-MHz Output/Frequency Select 3:</b> 48 MHz is provided in normal operation. In standard PC systems, this output can be used as the reference for the Universal Serial Bus host controller. This pin also serves as a power-on strap option to determine device operating frequency as described in Table 5.
24_48MHz/ FS2	7	I/O	<b>24_48-MHz Output/Frequency Select 2:</b> In standard PC systems, this output can be used as the clock input for a Super I/O chip. The output frequency is controlled by Configuration Byte 3 bit[6]. The default output frequency is 24 MHz. This pin also serves as a power-on strap option to determine device operating frequency as described in Table 5.
REF1/FS4	47	I/O	<b>Reference Clock Output 1/Frequency Select 4:</b> 3.3V 14.318-MHz output clock. This pin also serves as a power-on strap option to determine device operating frequency as described in Table 5.
REF0	48	O	<b>Reference Clock Output 0:</b> 3.3V 14.318-MHz output clock.
AGP0:2	23,26,27	O	<b>AGP Clock Output:</b> Frequency is set by FS0:4 inputs or through serial input interface, see Table 5 for details.
FS0:1	22,21	I	<b>Frequency Select 0 through 1:</b> 3.3V input to determine the device operating frequency as described in Table 5.
SCLK	28	I	Clock pin for SMBus circuitry.
SDATA	29	I/O	Data pin for SMBus circuitry.
X1	3	I	<b>Crystal Connection or External Reference Frequency Input:</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	4	I	<b>Crystal Connection:</b> An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDD_REF, VDD_48MHz, VDD_PCI, VDD_AGP, VDD_CORE	1, 5,15, 24, 31	P	<b>Power Connection:</b> Power supply for core logic, PLL circuitry, PCI outputs, reference outputs, 48-MHz output, and 24_48-MHz output, connect to 3.3V supply.
VDD_CPU, VDD_APIC	41, 46, 37	P	<b>Power Connection:</b> Power supply for APIC and CPU output buffers, connect to 2.5V.
GND_REF, GND_48MHz, GND_PCI, GND_AGP, GND_CORE, GND_CPU, GND_APIC	2, 8, 12, 19, 25, 30, 36, 40, 43	G	<b>Ground Connections:</b> Connect all ground pins to the common system ground plane.

### Serial Data Interface

The W312 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

### Data Protocol

The clock driver serial protocol supports byte/word write, byte/word read, block write, and block read operations from the

controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. For byte/word write and byte read operations, system controller can access individual indexed byte. The offset of the indexed byte is encoded in the command code.

The definition for the command code is defined as follows:

**Table 1. Command Code Definition**

Bit	Descriptions
7	0 = Block read or block write operation 1 = Byte/Word read or byte/word write operation
6:0	Byte offset for byte/word read or write operation. For block read or write operations, these bits need to be set at '0000000'.

**Table 2. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '00000000' stands for block operation	11:18	Command Code - 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
...	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
...	Data Byte N - 8 bits	47	Acknowledge
...	Acknowledge from slave	48:55	Data byte from slave - 8 bits
...	Stop	56	Acknowledge
		...	Data bytes from slave/Acknowledge
		...	Data byte N from slave - 8 bits
		...	Not Acknowledge
		...	Stop

**Table 3. Word Read and Word Write Protocol**

Word Write Protocol		Word Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxx' stands for byte or word operation bit[6:0] of the command code represents the off-set of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxx' stands for byte or word operation bit[6:0] of the command code represents the off-set of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte low- 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte high - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38	Stop	30:37	Data byte low from slave - 8 bits
		38	Acknowledge
		39:46	Data byte high from slave - 8 bits
		47	NOT acknowledge
		48	Stop

**Table 4. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxx' stands for byte operation bit[6:0] of the command code represents the off-set of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxx' stands for byte operation bit[6:0] of the command code represents the off-set of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

**CY28319 Serial Configuration Map**

1. The serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a "0" level.

3. All register bits labeled "Initialize to 0" must be written to zero during initialization.

**Byte 0: Control Register 0**

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	SEL2	0	See Table 5
Bit 5	-	SEL1	0	See Table 5
Bit 4	-	SEL0	0	See Table 5
Bit 3	-	FS_Override	0	0 = Select operating frequency by FS[4:0] input pins 1 = Select operating frequency by SEL[4:0] settings
Bit 2	-	SEL4	1	See Table 5
Bit 1	-	SEL3	0	See Table 5
Bit 0	-	Reserved	0	Reserved

**Byte 1: Control Register 1**

Bit	Pin#	Name	Default	Description
Bit 7	-	Reserved	0	Reserved
Bit 6	-	Spread Select2	0	'000' = Normal (spread off) '001' = Test Mode '010' = Reserved '011' = Three-States '100' = -0.5% '101' = ± 0.5% '110' = ± 0.25% '111' = ± 0.38%
Bit 5	-	Spread Select1	0	
Bit 4	-	Spread Select0	0	
Bit 3	35	CPU3	1	
Bit 2	38	CPU2	1	(Active/Inactive)
Bit 1	39	CPU1	1	(Active/Inactive)
Bit 0	42	APIC2	1	(Active/Inactive)

**Byte 2: Control Register 2**

Bit	Pin#	Name	Default	Description
Bit 7	20	PCI8	1	(Active/Inactive)
Bit 6	18	PCI7	1	(Active/Inactive)
Bit 5	17	PCI6	1	(Active/Inactive)
Bit 4	16	PCI5	1	(Active/Inactive)
Bit 3	14	PCI4	1	(Active/Inactive)
Bit 2	13	PCI3	1	(Active/Inactive)
Bit 1	11	PCI2	1	(Active/Inactive)
Bit 0	10	PCI1	1	(Active/Inactive)

**Byte 3: Control Register 3**

Bit	Pin#	Name	Default	Description
Bit 7	--	Reserved	0	Reserved
Bit 6	7	SEL_48MHz	0	0 = Select 24 MHz as output 1 = Select 48 MHz as output
Bit 5	6	48MHz	1	(Active/Inactive)
Bit 4	7	24_48MHz	1	(Active/Inactive)
Bit 3	9	PCI_F	1	(Active/Inactive)
Bit 2	27	AGP2	1	(Active/Inactive)
Bit 1	26	AGP1	1	(Active/Inactive)
Bit 0	23	AGP0	1	(Active/Inactive)

**Byte 4: Control Register 4**

Bit	Pin#	Name	Default	Description
Bit 7	-	PCI_Skew1	0	PCI skew control 00 = Normal 01 = -500 ps 10 = Reserved 11 = +500 ps
Bit 6	-	PCI_Skew0	0	
Bit 5	-	WD_TIMER4	1	These bits store the time-out value of the Watchdog Timer. The scale of the timer is determine by the pre-scaler. The timer can support a value of 150 ms to 4.8 sec when the pre-scalar is set to 150 ms. If the pre-scalar is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0," it will set the WD_TO_STATUS bit and generate Reset if RST_EN_WD is enabled.
Bit 4	-	WD_TIMER3	1	
Bit 3	-	WD_TIMER2	1	
Bit 2	-	WD_TIMER1	1	
Bit 1	-	WD_TIMER0	1	
Bit 0	-	WD_PRE_SCAL ER	0	0 = 150 ms 1 = 2.5 sec

**Byte 5: Control Register 5**

Bit	Pin#	Name	Default	Description
Bit 7	6	48Mhz_DRV	1	0 = Norm, 1 = High Drive
Bit 6	7	24_48MHz_DR V	1	0 = Norm, 1 = High Drive
Bit 5	44	APIC1	1	(Active/Inactive)
Bit 4	45	APIC0	1	(Active/Inactive)
Bit 3	-	Reserved	0	Reserved
Bit 2	-	Reserved	0	Reserved
Bit 1	47	REF1	1	(Active/Inactive)
Bit 0	48	REF0	1	(Active/Inactive)

**Byte 6: Reserved Register**

Bit	Pin#	Name	Default	Pin Description
Bit 7	-	Reserved	1	Reserved
Bit 6	-	Reserved	1	Reserved
Bit 5	-	Reserved	1	Reserved
Bit 4	-	Reserved	1	Reserved
Bit 3	-	Reserved	1	Reserved
Bit 2	-	Reserved	1	Reserved
Bit 1	-	Reserved	1	Reserved
Bit 0	-	Reserved	1	Reserved

**Byte 7: Reserved Register**

Bit	Pin#	Name	Default	Pin Description
Bit 7	-	Reserved	1	Reserved
Bit 6	-	Reserved	1	Reserved
Bit 5	-	Reserved	1	Reserved
Bit 4	-	Reserved	1	Reserved
Bit 3	-	Reserved	1	Reserved
Bit 2	-	Reserved	1	Reserved
Bit 1	-	Reserved	1	Reserved
Bit 0	-	Reserved	1	Reserved

**Byte 8: Vendor & Revision ID Register (Read Only)**

Bit	Name	Default	Pin Description
Bit 7	Revision_ID3	0	Revision ID bit[3]
Bit 6	Revision_ID2	0	Revision ID bit[2]
Bit 5	Revision_ID1	0	Revision ID bit[1]
Bit 4	Revision_ID0	0	Revision ID bit[0]
Bit 3	Vendor_ID3	1	Bit[3] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 2	Vendor_ID2	0	Bit[2] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 1	Vendor_ID1	0	Bit[1] of Cypress Semiconductor's Vendor ID. This bit is read only.
Bit 0	Vendor_ID0	0	Bit[0] of Cypress Semiconductor's Vendor ID. This bit is read only.

**Byte 9: System RESET and Watchdog Timer Register**

Bit	Name	Default	Pin Description
Bit 7	Reserved	0	Reserved
Bit 6	PCI_DRV	0	PCI clock output drive strength 0 = Normal 1 = High Drive
Bit 5	Reserved	0	Reserved
Bit 4	RST_EN_WD	0	This bit will enable the generation of a Reset pulse when a watchdog timer time-out occurs. 0 = Disabled 1 = Enabled
Bit 3	RST_EN_FC	0	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled
Bit 2	WD_TO_STATUS	0	Watchdog Timer Time-out Status bit 0 = No time-out occurs (READ); Ignore (WRITE) 1 = time-out occurred (READ); Clear WD_TO_STATUS (WRITE)
Bit 1	WD_EN	0	0 = Stop and re-load Watchdog Timer 1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs. <b>Note:</b> CY28319 will generate system reset, reload a recovery frequency, and lock itself into a recovery frequency mode after a watchdog timer time-out occurs. Under recovery frequency mode, CY28319 will not respond to any attempt to change output frequency via the SMBus control bytes. System software can unlock CY28319 from its recovery frequency mode by clearing the WD_EN bit.
Bit 0	Reserved	0	Reserved

**Byte 10: Skew Control Register**

Bit	Name	Default	Description
Bit 7	CPU_Skew2	0	CPU skew control 000 = Normal 001 = -150 ps 010 = -300 ps 011 = -450 ps 100 = +150 ps 101 = +300 ps 110 = +450 ps 111 = +600 ps
Bit 6	CPU_Skew1	0	
Bit 5	CPU_Skew0	0	
Bit 4	Reserved	0	
Bit 3	Reserved	0	Reserved
Bit 2	Reserved	0	Reserved
Bit 1	AGP_Skew1	0	AGP skew control 00 = Normal 01 = -150 ps 10 = +150 ps 11 = +300 ps
Bit 0	AGP_Skew0	0	



**Byte 11: Recovery Frequency N-Value Register**

Bit	Name	Default	Pin Description
Bit 7	ROCV_FREQ_N7	0	<p>If ROCV_FREQ_SEL is set, CY28319 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs.</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, CY28319 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28319 will use the frequency ratio stated in the SEL[4:0] register.</p> <p>CY28319 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.</p> <p>CY28319 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.</p>
Bit 6	ROCV_FREQ_N6	0	
Bit 5	ROCV_FREQ_N5	0	
Bit 4	ROCV_FREQ_N4	0	
Bit 3	ROCV_FREQ_N3	0	
Bit 2	ROCV_FREQ_N2	0	
Bit 1	ROCV_FREQ_N1	0	
Bit 0	ROCV_FREQ_N0	0	

**Byte 12: Recovery Frequency M-Value Register**

Bit	Name	Default	Pin Description
Bit 7	ROCV_FREQ_SEL	0	<p>ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog Timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.</p> <p>0 = From latched FS[4:0]  1 = From the settings of ROCV_FREQ_N[7:0] &amp; ROCV_FREQ_M[6:0]</p>
Bit 6	ROCV_FREQ_M6	0	<p>If ROCV_FREQ_SEL is set, CY28319 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, CY28319 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28319 will use the frequency ratio stated in the SEL[4:0] register.</p> <p>CY28319 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.</p> <p>CY28319 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.</p>
Bit 5	ROCV_FREQ_M5	0	
Bit 4	ROCV_FREQ_M4	0	
Bit 3	ROCV_FREQ_M3	0	
Bit 2	ROCV_FREQ_M2	0	
Bit 1	ROCV_FREQ_M1	0	
Bit 0	ROCV_FREQ_M0	0	

**Byte 13: Programmable Frequency Select N-Value Register**

Bit	Name	Default	Pin Description
Bit 7	CPU_FSEL_N7	0	<p>If Prog_Freq_EN is set, CY28319 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated.</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, CY28319 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28319 will use the frequency ratio stated in the SEL[4:0] register.</p> <p>CY28319 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.</p>
Bit 6	CPU_FSEL_N6	0	
Bit 5	CPU_FSEL_N5	0	
Bit 4	CPU_FSEL_N4	0	
Bit 3	CPU_FSEL_N3	0	
Bit 2	CPU_FSEL_N2	0	
Bit 1	CPU_FSEL_N1	0	
Bit 0	CPU_FSEL_N0	0	

**Byte 14: Programmable Frequency Select M-Value Register**

Bit	Name	Default	Description
Bit 7	Pro_Freq_EN	0	Programmable output frequencies enabled 0 = disabled 1 = enabled
Bit 6	CPU_FSEL_M6	0	If Prog_Freq_EN is set, CY28319 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated. The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, CY28319 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28319 will use the frequency ratio stated in the SEL[4:0] register. CY28319 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.
Bit 5	CPU_FSEL_M5	0	
Bit 4	CPU_FSEL_M4	0	
Bit 3	CPU_FSEL_M3	0	
Bit 2	CPU_FSEL_M2	0	
Bit 1	CPU_FSEL_M1	0	
Bit 0	CPU_FSEL_M0	0	

**Byte 15: Reserved Register**

Bit	Pin#	Name	Default	Description
Bit 7	47	Latched FS4 input	X	Latched FS[4:0] inputs. These bits are read only.
Bit 6	6	Latched FS3 input	X	
Bit 5	7	Latched FS2 input	X	
Bit 4	21	Latched FS1 input	X	
Bit 3	22	Latched FS0 input	X	
Bit 2	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 1	-	Vendor test mode	1	Reserved. Write with '1'
Bit 0	-	Vendor test mode	1	Reserved. Write with '1'

**Byte 16: Reserved Register**

Bit	Pin#	Name	Default	Description
Bit 7	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 6	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 5	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 4	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 3	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 2	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 1	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 0	-	Vendor test mode	0	Reserved. Write with '0'.

**Byte 17: Reserved Register**

Bit	Pin#	Name	Default	Description
Bit 7	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 6	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 5	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 4	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 3	-	Vendor test mode	0	Reserved. Write with '0'.

**Byte 17: Reserved Register** (continued)

Bit	Pin#	Name	Default	Description
Bit 2	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 1	-	Vendor test mode	0	Reserved. Write with '0'.
Bit 0	-	Vendor test mode	0	Reserved. Write with '0'.

**Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes**

Input Conditions					Output Frequency			PLL Gear Constants (G)
FS4 SEL4	FS3 SEL3	FS2 SEL2	FS1 SEL1	FS0 SEL0	CPU	3V66	PCI	
0	0	0	0	0	200.0	66.6	33.3	48.00741
0	0	0	0	1	190.0	76.0	38.0	48.00741
0	0	0	1	0	180.0	72.0	36.0	48.00741
0	0	0	1	1	170.0	68.0	34.0	48.00741
0	0	1	0	0	166.0	66.4	33.2	48.00741
0	0	1	0	1	160.0	64.0	32.0	48.00741
0	0	1	1	0	150.0	75.0	37.5	48.00741
0	0	1	1	1	145.0	72.5	36.3	48.00741
0	1	0	0	0	140.0	70.0	35.0	48.00741
0	1	0	0	1	136.0	68.0	34.0	48.00741
0	1	0	1	0	130.0	65.0	32.5	48.00741
0	1	0	1	1	124.0	62.0	31.0	48.00741
0	1	1	0	0	66.6	66.6	33.3	48.00741
0	1	1	0	1	100.0	66.6	33.3	48.00741
0	1	1	1	0	118.0	78.7	39.3	48.00741
0	1	1	1	1	133.3	66.6	33.3	48.00741
1	0	0	0	0	66.8	66.8	33.4	48.00741
1	0	0	0	1	100.2	66.8	33.4	48.00741
1	0	0	1	0	115.0	76.7	38.3	48.00741
1	0	0	1	1	133.6	66.8	33.4	48.00741
1	0	1	0	0	66.8	66.8	33.4	48.00741
1	0	1	0	1	100.2	66.8	33.4	48.00741
1	0	1	1	0	110.0	73.3	36.7	48.00741
1	0	1	1	1	133.6	66.8	33.4	48.00741
1	1	0	0	0	105.0	70.0	35.0	48.00741
1	1	0	0	1	90.0	60.0	30.0	48.00741
1	1	0	1	0	85.0	56.7	28.3	48.00741
1	1	0	1	1	78.0	78.0	39.0	48.00741
1	1	1	0	0	66.6	66.6	33.3	48.00741
1	1	1	0	1	100.0	66.6	33.3	48.00741
1	1	1	1	0	75.0	75.0	37.5	48.00741
1	1	1	1	1	133.3	66.6	33.3	48.00741

## Programmable Output Frequency, Watchdog Timer and Recovery Output Frequency Functional Description

The Programmable Output Frequency feature allows users to generate any CPU output frequency from the range of 50 MHz to 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism when the system hangs or getting unstable. System BIOS or other control software can enable the Watchdog timer before they attempt to make a frequency change. If the system hangs and a Watchdog Timer time-out occurs, a system reset will be generated and a recovery frequency will be activated.

All the related registers are summarized *Table 6*.

**Table 6. Register Summary**

Name	Description
Pro_Freq_EN	<p>Programmable output frequencies enabled 0 = Disabled (default) 1 = Enabled</p> <p>When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If FS_Override bit is set, programmed value of SEL[4:0] will be used.</p> <p>When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs.</p>
FS_Override	<p>When Pro_Freq_EN is cleared or disabled, 0 = Select operating frequency by FS input pins (default) 1 = Select operating frequency by SEL bits in SMBus control bytes</p> <p>When Pro_Freq_EN is set or enabled, 0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default) 1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes</p>
CPU_FSEL_N, CPU_FSEL_M	<p>When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determines the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PCI. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes.</p>
ROCV_FREQ_SEL	<p>ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog Timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL. 0 = From latched FS[4:0] 1 = From the settings of ROCV_FREQ_N[7:0] &amp; ROCV_FREQ_M[6:0]</p>
ROCV_FREQ_N[7:0], ROCV_FREQ_M[6:0]	<p>When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog Timer time-out occurs</p> <p>The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PCI. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.</p> <p>The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use word or block write to update both registers within the same SMBus bus operation.</p>
WD_EN	<p>0 = Stop and reload Watchdog Timer 1 = Enable Watchdog Timer. It will start counting down after a frequency change occurs.</p>

**Table 6. Register Summary (continued)**

Name	Description
WD_TO_STATUS	Watchdog Timer Time-out Status bit 0 = No time-out occurs (READ); Ignore (WRITE) 1 = Time-out occurred (READ); Clear WD_TO_STATUS (WRITE)
WD_TIMER[4:0]	These bits store the time-out value of the Watchdog Timer. The scale of the timer is determine by the prescaler. The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. When the Watchdog Timer reaches "0." it will set the WD_TO_STATUS bit.
WD_PRE_SCALER	0 = 150 ms 1 = 2.5 sec
RST_EN_WD	This bit will enable the generation of a Reset pulse when a Watchdog Timer time-out occurs. 0 = Disabled 1 = Enabled
RST_EN_FC	This bit will enable the generation of a Reset pulse after a frequency change occurs. 0 = Disabled 1 = Enabled

**How to Program CPU Output Frequency**

When the programmable output frequency feature is enabled (Pro\_Freq\_EN bit is set), the CPU output frequency is determined by the following equation:

$$F_{cpu} = G * (N+3)/(M+3)$$

"N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

"G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 5*.

The ratio of (N+3) and (M+3) need to be greater than "1" [(N+3)/(M+3) > 1].

The following table lists set of N and M values for different frequency output ranges. This example use a fixed value for the M-Value Register and select the CPU output frequency by changing the value of the N-Value Register.

**Table 7. Examples of N and M Value for Different CPU Frequent Range**

Frequency Ranges	Gear Constants	Fixed Value for M-Value Register	Range of N-Value Register for Different CPU Frequency
50 MHz – 129 MHz	48.00741	93	97 – 255
130 MHz – 248 MHz	48.00741	45	127 – 245

### Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on Any Pin with Respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C
$T_A$	Operating Temperature	0 to +70	°C
$ESD_{PROT}$	Input ESD Protection	2 (min.)	kV

### DC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , 3.3V, $V_{DD} = 3.3V \pm 5\%$ , 2.5V, $V_{DD} = 2.5V \pm 5\%$

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I <sub>DD</sub>	3.3V Supply Current		CPU1:3 = 133 MHz <sup>[2]</sup>		TBD		mA
I <sub>DD</sub>	2.5V Supply Current				TBD		mA
Logic Inputs							
V <sub>IL</sub>	Input Low Voltage			GND – 0.3		0.8	V
V <sub>IH</sub>	Input High Voltage			2.0		V <sub>DD</sub> + 0.3	V
I <sub>IL</sub>	Input Low Current <sup>[3]</sup>					–25	μA
I <sub>IH</sub>	Input High Current <sup>[3]</sup>					10	μA
Clock Outputs							
V <sub>OL</sub>	Output Low Voltage		I <sub>OL</sub> = 1 mA			50	mV
V <sub>OH</sub>	Output High Voltage		I <sub>OH</sub> = –1 mA	3.1			V
V <sub>OH</sub>	Output High Voltage	CPU1:3, APIC0:2	I <sub>OH</sub> = –1 mA	2.2			V
I <sub>OL</sub>	Output Low Current	CPU1:3	V <sub>OL</sub> = 1.25V	27	57	97	mA
		PCI_F, PCI1:8	V <sub>OL</sub> = 1.5V	20.5	53	139	mA
		AGP0:2	V <sub>OL</sub> = 1.25V	40	85	140	mA
		APIC0:2	V <sub>OL</sub> = 1.25V	40	85	140	mA
		REF0:1	V <sub>OL</sub> = 1.5V	25	37	76	mA
		48-MHz	V <sub>OL</sub> = 1.5V	25	37	76	mA
		24-MHz	V <sub>OL</sub> = 1.5V	25	37	76	mA
I <sub>OH</sub>	Output High Current	CPU1:3	V <sub>OH</sub> = 1.25V	25	55	97	mA
		PCI_F, PCI1:8	V <sub>OH</sub> = 1.5V	31	55	139	mA
		AGP0:2	V <sub>OL</sub> = 1.25V	40	85	140	mA
		APIC0:1	V <sub>OH</sub> = 1.5V	27	44	94	mA
		48-MHz	V <sub>OH</sub> = 1.5V	27	44	94	mA
		24-MHz	V <sub>OH</sub> = 1.5V	25	37	76	mA

#### Notes:

2. All clock outputs loaded with 6" 60Ω transmission lines with 22-pF capacitors.
3. Inputs have internal pull-up resistors.

**DC Electrical Characteristics:**  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , 3.3V,  $V_{DD} = 3.3\text{V} \pm 5\%$ , 2.5V,  $V_{DD} = 2.5\text{V} \pm 5\%$  (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
<b>Crystal Oscillator</b>						
$V_{TH}$	X1 Input Threshold Voltage <sup>[4]</sup>	$V_{DDQ3} = 3.3\text{V}$		1.65		V
$C_{LOAD}$	Load Capacitance, Imposed on External Crystal <sup>[5]</sup>			18		pF
$C_{IN,X1}$	X1 Input Capacitance <sup>[6]</sup>	Pin X2 unconnected		28		pF
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance	Except X1 and X2			5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

**AC Electrical Characteristics**
 $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , 3.3V,  $V_{DD} = 3.3\text{V} \pm 5\%$ , 2.5V,  $V_{DD} = 2.5\text{V} \pm 5\%$   $f_{XTL} = 14.31818\text{ MHz}$ 

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum is disabled.

**CPU Clock Outputs (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/ Comments	CPU = 66.6 MHz			CPU = 100 MHz			CPU = 133 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.25	15		15.5	10		10.5	7.5		8.0	ns
$t_H$	High Time	Duration of clock cycle above 2.0V	5.2			3.0			1.87			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			1.67			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250			250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.25V			175			175			175	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3			3	ms
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20			20		$\Omega$

**Notes:**

- X1 input threshold voltage (typical) is 3.3V/2.
- The CY28319 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
- X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).



**PCI Clock Outputs, PCI0:5 (Lump Capacitance Test Load = 30 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$t_P$	Period	Measured on rising edge at 1.5V	30			ns
$t_H$	High Time	Duration of clock cycle above 2.4V	12			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	12			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.5V			500	ps
$t_O$	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		$\Omega$

**AGP Clock Outputs, (Lump Capacitance test Load = 30 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$t_P$	Period	Measured on rising edge at 1.5V	15			ns
$t_H$	High Time	Duration of clock cycle above 2.4V	5.25			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	5.05			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.5V			250	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		$\Omega$

**APIC Clock Output (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$f$	Frequency, Actual	Frequency generated from PCI divided by 2	PCI/2			MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		$\Omega$



**REF Clock Outputs (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z <sub>o</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

**48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)	48.008			MHz
f <sub>D</sub>	Deviation from 48 MHz	(48.008 – 48)/48	+167			ppm
m/n	PLL Ratio	14.31818 MHz x 57/17 = 48.008 MHz	57/17			
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z <sub>o</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

**24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

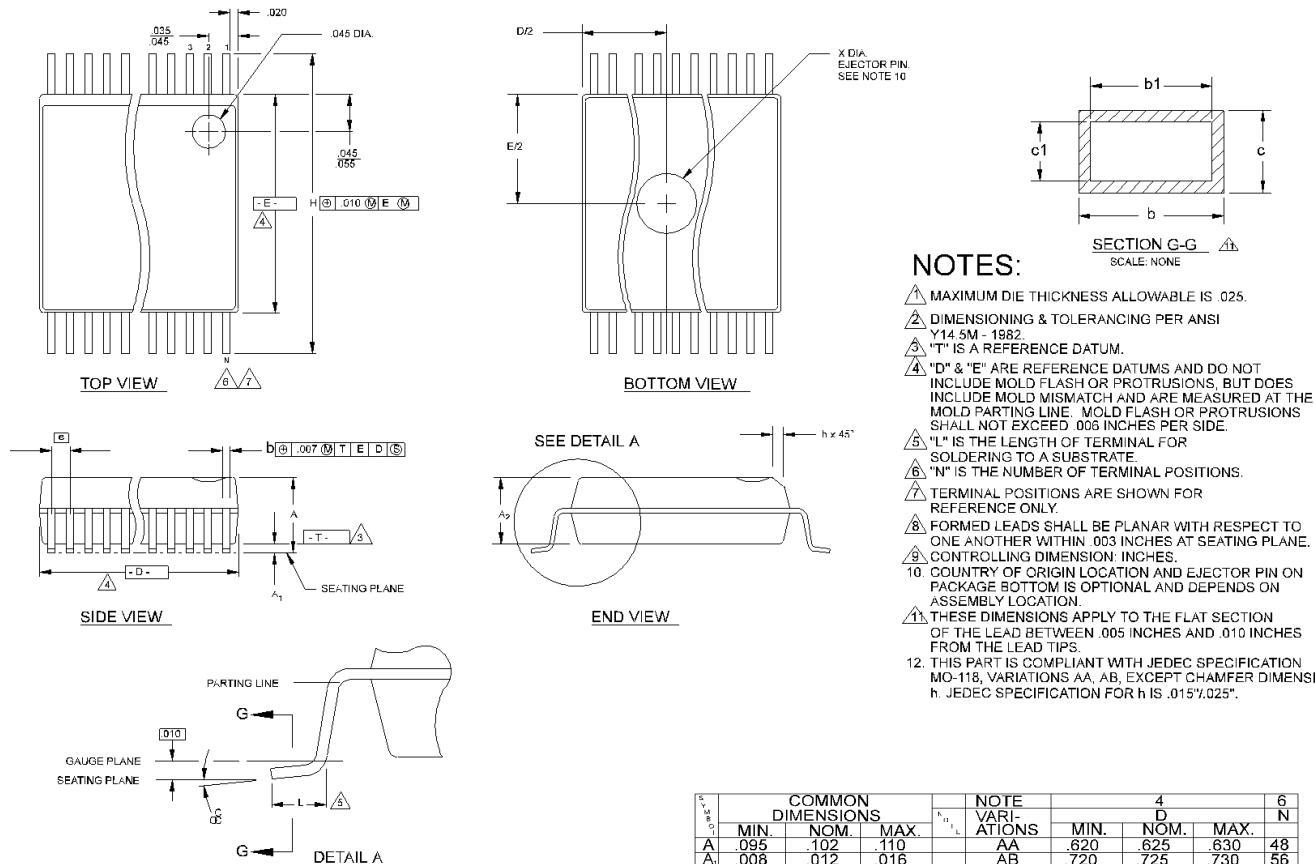
Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)	24.004			MHz
f <sub>D</sub>	Deviation from 24 MHz	(24.004 – 24)/24	+167			ppm
m/n	PLL Ratio	(14.31818 MHz x 57/34 = 24.004 MHz)	57/34			
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z <sub>o</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY28319	PCV	48-pin SSOP (300 mils)	Commercial

## Package Diagram

### 48-Pin Small Shrink Outline Package (SSOP, 300 mils)



#### Summary of nominal dimensions in inches:

**Body Width: 0.296**  
**Lead Pitch: 0.025**  
**Body Length: 0.625**  
**Body Height: 0.102**

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AA	.620	.625	.630	48
A	.008	.012	.016	AB	.720	.725	.730	56
b	.008	.010	.0135					
b	.008	.010	.012					
c	.005	-	.010					
c	.005	.006	.0085					
D	SEE VARIATIONS			4				
E	.292	.296	.299					
e	.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	SEE VARIATIONS			6				
X	.085	.093	.100	10				
α	0°	5°	8°					

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	2.41	2.59	2.79	AA	15.75	15.88	16.00	48
A	0.20	0.31	0.41	AB	18.29	18.42	18.54	56
b	2.24	2.29	2.34					
b	0.203	0.254	0.343					
b	0.203	0.254	0.305					
c	0.127	-	0.254					
c	0.127	0.152	0.216					
D	SEE VARIATIONS			4				
E	7.42	7.52	7.59					
e	0.635 BSC							
H	10.16	10.31	10.41					
h	0.25	0.33	0.41					
L	0.61	0.81	1.02					
N	SEE VARIATIONS			6				
X	2.16	2.36	2.54	10				
α	0°	5°	8°					

THIS TABLE IN MILLIMETERS



<b>Document Title: CY28319 FTG for VIA Pro-266T DDR Chipset</b> <b>Document Number: 38-07009</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	106363	06/27/01	IKA	New Data Sheet