



**CY2907**

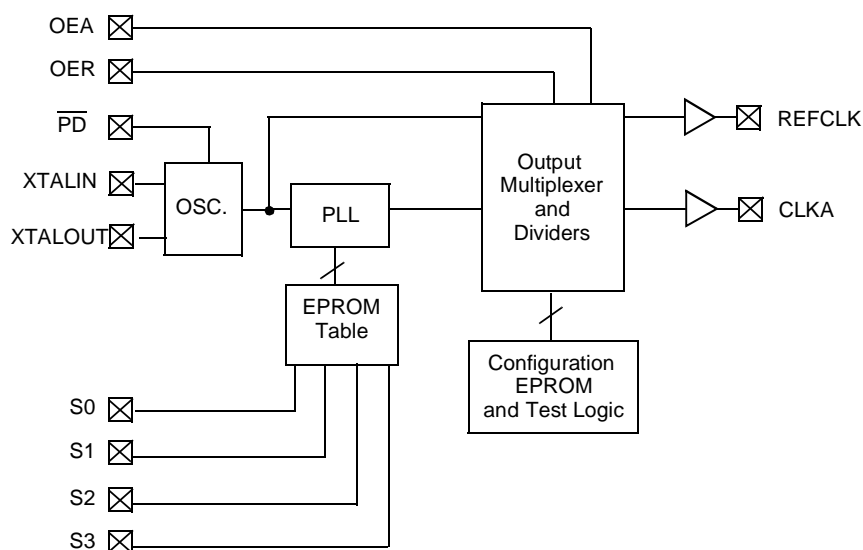
# Single-PLL General-Purpose EPROM Programmable Clock Generator

Features	Benefits
Single phase-locked loop architecture	Generates a custom frequency from an external source
EPROM programmability	Easy customization and fast turnaround
Factory-programmable (CY2907, CY2907I) or field-programmable (CY2907F & CY2907FI) device options	Programming support available for all opportunities
Up to two configurable outputs	Provides clocking requirements from a single device
Low-skew, low-jitter, high-accuracy outputs	Meets critical industry standard timing requirements
Power management (Power-Down, OE)	Supports low-power applications
Frequency select option	Up to 16 user-selectable frequencies
Configurable 5V or 3.3V operation	Supports industry-standard design platforms
8-pin or 14-pin SOIC packages	Industry-standard packaging saves on board space

## Selector Guide

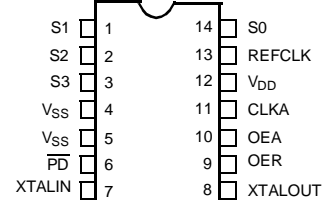
Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2907	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–130 MHz (5V) 500 kHz–100 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2907I	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2907F8 CY2907F14	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	<b>Field Programmable</b> Commercial Temperature
CY2907F8I CY2907F14I	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–90 MHz (5V) 500 kHz–66.66 MHz (3.3V)	<b>Field Programmable</b> Industrial Temperature

## Logic Block Diagram

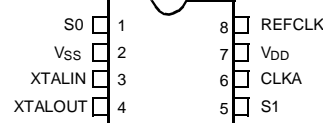


## Pin Configurations

### Top View 14-Pin SOIC



### 8-Pin SOIC



CyClocks is a trademark of Cypress Semiconductor Corporation.

## Pin Summary

Name	Pin Number		Description
	14-Pin SOIC	8-Pin SOIC	
S1	1	5	Frequency Select (CLKA) (Internal pull-up resistor to $V_{DD}$ )
S2	2	NA	Frequency Select (CLKA) (Internal pull-up resistor to $V_{DD}$ )
S3	3	NA	Frequency Select (CLKA) (Internal pull-up resistor to $V_{DD}$ )
$V_{SS}$	4	2	Ground
$V_{SS}$	5	NA	Ground
PD	6	NA	Power-Down (active LOW) (Internal pull-up resistor to $V_{DD}$ )
XTALIN <sup>[1]</sup>	7	3	Reference Crystal Input
XTALOUT <sup>[1, 2]</sup>	8	4	Reference Crystal Feedback
OER	9	NA	REFCLK Output Enable (active HIGH) (Internal pull-up resistor to $V_{DD}$ )
OEA	10	NA	CLKA Output Enable (active HIGH) (Internal pull-up resistor to $V_{DD}$ )
CLKA	11	6	Clock Output
$V_{DD}$	12	7	Voltage Supply
REFCLK	13	8	Reference Clock Output (Default, can be driven by PLL if desired)
S0	14	1	Frequency Select (CLKA) (Internal pull-up resistor to $V_{DD}$ )

### Notes:

- For best accuracy, use a parallel-resonant crystal,  $C_{LOAD} \approx 17$  pF.
- Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).

## Functional Description

The CY2907 is a general-purpose Clock Generator designed for use in a wide variety of applications—from graphics to PC peripherals to disk drives. It generates selectable system clock frequencies from a single reference input (crystal or reference clock). The CY2907 is configured with an EPROM array, much like the other devices in the Cypress EPROM Programmable Clock Family, making it easily customizable for any application. Furthermore, the CY2907 is compatible with all industry-standard 9107 and 9108 clock synthesizers.

## CyClocks™ Software

CyClocks is an easy-to-use software application that allows you to configure any one of the EPROM Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Please note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. You can download a copy of CyClocks free on the Cypress Semiconductor website at [www.cypress.com](http://www.cypress.com).

Consider using the CY2081, CY2291, or CY2292 for applications that require unrelated and multiple output frequencies. Consider using the CY2071A for applications that require more than one output clock.

## Cypress FTG Programmer

The Cypress Frequency Timing Generator (FTG) Programmers are portable programmers designed to custom program our family of EPROM **Field** Programmable Clock Devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

## Maximum Ratings

(Beyond which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....	–0.5 to +7.0V
Input Voltage.....	–0.5V to $V_{DD}+0.5V$
Storage Temperature (Non-Condensing) ...	–65°C to +150°C
Max. Soldering Temperature (10 sec) .....	+260°C
Junction Temperature .....	+150°C
Static Discharge Voltage .....	>2000V (per MIL-STD-883, Method 3015)

**Operating Conditions<sup>[3]</sup>**

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage, 5V Operation	4.5	5.5	V
	Supply Voltage, 3.3V Operation	3.0	3.6	V
T <sub>A</sub>	Commercial Operating Temperature, Ambient	0	70	°C
	Industrial Operating Temperature, Ambient	-40	85	°C
C <sub>L</sub>	Max. Capacitive Load		15	pF
f <sub>REF</sub>	External Reference Crystal	10.0	25.0	MHz
	External Reference Clock <sup>[4, 5]</sup>	1.0	30.0	MHz

**Electrical Characteristics at 5.0V Commercial** V<sub>DD</sub> = 4.5V to 5.5V, T<sub>A</sub> = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V <sub>IH</sub>	High-level Input Voltage	Except Crystal Inputs			2.0		V
V <sub>IL</sub>	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V <sub>OH</sub> <sup>[4]</sup>	High-level Output Voltage	V <sub>DD</sub> = V <sub>DD</sub> Min.	I <sub>OH</sub> = -30 mA	CLKA	2.4		V
V <sub>OL</sub> <sup>[4]</sup>	Low-level Output Voltage	V <sub>DD</sub> = V <sub>DD</sub> Min.	I <sub>OL</sub> = 10 mA	CLKA		0.4	V
I <sub>OH</sub> <sup>[4]</sup>	Output High Current	V <sub>OH</sub> = 2.0V				-35	mA
I <sub>OL</sub> <sup>[4]</sup>	Output Low Current	V <sub>OL</sub> = 0.8V			22		mA
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>			-2	2	μA
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V				20	μA
I <sub>DD</sub> <sup>[5]</sup>	Power Supply Current	PD HIGH, CLKA = 50 MHz				42	mA
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs LOW				100	μA
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs HIGH				40	μA
R <sub>PU</sub> <sup>[4]</sup>	Pull-up Resistor	V <sub>IN</sub> = V <sub>DD</sub> - 1.0 V				700	kΩ

**Electrical Characteristics at 3.3V Commercial** V<sub>DD</sub> = 3.0V to 3.6V, T<sub>A</sub> = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V <sub>IH</sub>	High-level Input Voltage	Except Crystal Inputs			0.7*V <sub>DD</sub>		V
V <sub>IL</sub>	Low-level Input Voltage	Except Crystal Inputs				0.2*V <sub>DD</sub>	V
V <sub>OH</sub> <sup>[4]</sup>	High-level Output Voltage	CLKA, I <sub>OH</sub> = -5 mA			0.85*V <sub>DD</sub>		V
V <sub>OL</sub> <sup>[4]</sup>	Low-level Output Voltage	CLKA, I <sub>OL</sub> = 6 mA				0.1*V <sub>DD</sub>	V
I <sub>OH</sub> <sup>[4]</sup>	Output High Current	V <sub>OH</sub> = 0.7*V <sub>DD</sub>				-10	mA
I <sub>OL</sub> <sup>[4]</sup>	Output Low Current	V <sub>OL</sub> = 0.2*V <sub>DD</sub>			15		mA
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>			-2	2	μA
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V				10	μA
I <sub>DD</sub> <sup>[5]</sup>	Power Supply Current	PD HIGH, CLKA = 50 MHz				40	mA
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs LOW				40	μA
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs HIGH				12	μA
R <sub>PU</sub> <sup>[4]</sup>	Pull-up Resistor	V <sub>IN</sub> = V <sub>DD</sub> - 0.5V				900	kΩ

**Notes:**

- Electrical parameters are guaranteed with these operating conditions.
- Guaranteed by design, not 100% tested in production.
- Load = max. typical configuration, f<sub>REF</sub> = 14.318 MHz. Specific configurations may vary. A close approximation of I<sub>DD</sub> can be derived by the following formula:  

$$I_{DD} \text{ (mA)} = V_{DD} * (6.25 + (0.055 * F_{REF}) + (0.0017 * C_{LOAD} * (F_{CLKA} + REFCLK)))$$
C<sub>LOAD</sub> is specified in pF and F is specified in MHz.

**Electrical Characteristics at 5.0V Industrial**  $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ 

Parameter	Description	Test Conditions			Min.	Max.	Unit
$V_{IH}$	High-level Input Voltage	Except Crystal Inputs			2.0		V
$V_{IL}$	Low-level Input Voltage	Except Crystal Inputs				0.8	V
$V_{OH}^{[4]}$	High-level Output Voltage	$V_{DD} = V_{DD} \text{ Min.}$	$I_{OH} = -30 \text{ mA}$	CLKA	2.4		V
$V_{OL}^{[4]}$	Low-level Output Voltage	$V_{DD} = V_{DD} \text{ Min.}$	$I_{OL} = 10 \text{ mA}$	CLKA		0.4	V
$I_{OH}^{[4]}$	Output High Current	$V_{OH} = 2.0V$				-45	mA
$I_{OL}^{[4]}$	Output Low Current	$V_{OL} = 0.8V$			20		mA
$I_{IH}$	Input High Current	$V_{IH} = V_{DD}$			-2	2	$\mu A$
$I_{IL}$	Input Low Current	$V_{IL} = 0V$				20	$\mu A$
$I_{DD}^{[5]}$	Power Supply Current	$\overline{PD}$ HIGH, CLKA = 50 MHz				54	mA
$I_{DD}$	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW				110	$\mu A$
$I_{DD}$	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH				45	$\mu A$
$R_{PU}^{[4]}$	Pull-up Resistor	$V_{IN} = V_{DD} - 1.0 \text{ V}$				700	k $\Omega$

**Electrical Characteristics at 3.3V Industrial**  $V_{DD} = 3.0V$  to  $3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ 

Parameter	Description	Test Conditions			Min.	Max.	Unit
$V_{IH}$	High-level Input Voltage	Except Crystal Inputs			$0.7 \cdot V_{DD}$		V
$V_{IL}$	Low-level Input Voltage	Except Crystal Inputs				$0.2 \cdot V_{DD}$	V
$V_{OH}^{[4]}$	High-level Output Voltage	CLKA, $I_{OH} = -5 \text{ mA}$			$0.85 \cdot V_{DD}$		V
$V_{OL}^{[4]}$	Low-level Output Voltage	CLKA, $I_{OL} = 6 \text{ mA}$				$0.1 \cdot V_{DD}$	V
$I_{OH}^{[4]}$	Output High Current	$V_{OH} = 0.7 \cdot V_{DD}$				-12	mA
$I_{OL}^{[4]}$	Output Low Current	$V_{OL} = 0.2 \cdot V_{DD}$			14		mA
$I_{IH}$	Input High Current	$V_{IH} = V_{DD}$			-2	2	$\mu A$
$I_{IL}$	Input Low Current	$V_{IL} = 0V$				10	$\mu A$
$I_{DD}^{[5]}$	Power Supply Current	$\overline{PD}$ HIGH, CLKA = 50 MHz				50	mA
$I_{DD}$	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW				50	$\mu A$
$I_{DD}$	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH				15	$\mu A$
$R_{PU}^{[4]}$	Pull-up resistor	$V_{IN} = V_{DD} - 0.5V$				900	k $\Omega$

**Switching Characteristics at 5.0V Commercial<sup>[4]</sup>**

Parameter	Output <sup>[6]</sup>	Description	Test Conditions	Min.	Max.	Unit
t <sub>R</sub>	CLKA	Output Rise Time 0.8V to 2.0V	15-pF Load		1.40	ns
t <sub>F</sub>	CLKA	Output Fall Time 2.0V to 0.8V	15-pF Load		1.00	ns
t <sub>R</sub>	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t <sub>F</sub>	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t <sub>D</sub>	CLKA	Duty Cycle	15-pF Load at 1.4V	45.0	55.0	%
F <sub>I</sub>	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F <sub>I</sub>	XTALIN	Input Frequency	External Input Clock <sup>[7]</sup>	1	30	MHz
F <sub>O</sub>	CLKA	Output Frequency	CY2907, 15-pF Load	0.5	130.0	MHz
			CY2907F, 15-pF Load	0.5	100.0	MHz
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	20 MHz to 130 MHz		150	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	14 MHz to 20 MHz		200	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	20 MHz to 130 MHz	-250	+ 250	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	14 MHz to 20 MHz	-500	+ 500	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t <sub>PU</sub>		Power-up Time			18	ms
t <sub>FT</sub>	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

**Switching Characteristics at 3.3V Commercial<sup>[4]</sup>**

Parameter	Output <sup>[6]</sup>	Description	Test Conditions	Min.	Max.	Unit
t <sub>R</sub>	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t <sub>F</sub>	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t <sub>D</sub>	CLKA	Duty Cycle	15-pF Load at 1.4V	40.0	53.0	%
F <sub>I</sub>	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F <sub>I</sub>	XTALIN	Input Frequency	External Input Clock <sup>[7]</sup>	1	30	MHz
F <sub>O</sub>	CLKA	Output Frequency	CY2907, 15-pF Load	0.5	100.0	MHz
			CY2907F, 15-pF Load	0.5	80.0	MHz
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	25 MHz to 100 MHz		150	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	14 MHz to 25 MHz		200	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	25 MHz to 120 MHz	-250	+250	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	14 MHz to 25 MHz	-500	+500	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t <sub>PU</sub>		Power-up Time			18	ms
t <sub>FT</sub>	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

**Notes:**

6. REFCLK output can also be configured to be driven by the PLL, in which case the above characteristics are valid.
7. Please refer to the application note "Crystal Oscillator Topics" when using an external reference clock as an input frequency source.

**Switching Characteristics at 5.0V Industrial**

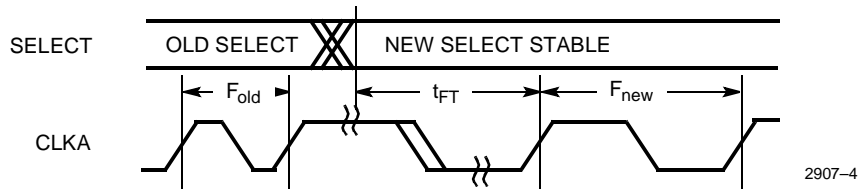
Parameter	Output <sup>[6]</sup>	Description	Test Conditions	Min.	Max.	Unit
t <sub>R</sub>	CLKA	Output Rise Time 0.8V to 2.0V	15-pF Load		1.40	ns
t <sub>F</sub>	CLKA	Output Fall Time 2.0V to 0.8V	15-pF Load		1.00	ns
t <sub>R</sub>	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t <sub>F</sub>	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t <sub>D</sub>	CLKA	Duty Cycle	15-pF Load at 1.4V	45.0	55.0	%
F <sub>I</sub>	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F <sub>I</sub>	XTALIN	Input Frequency	External Input Clock <sup>[7]</sup>	1	30	MHz
F <sub>O</sub>	CLKA	Output Frequency	CY2907, 15-pF Load	0.5	100.0	MHz
			CY2907F, 15-pF Load	0.5	90	MHz
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	20 MHz to 130 MHz		150	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	14 MHz to 20 MHz		200	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	20 MHz to 130 MHz	-250	+ 250	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	14 MHz to 20 MHz	-500	+ 500	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t <sub>PU</sub>		Power-up Time			18	ms
t <sub>FT</sub>	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

**Switching Characteristics at 3.3V Industrial**

Parameter	Output <sup>[6]</sup>	Description	Test Conditions	Min.	Max.	Unit
t <sub>R</sub>	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t <sub>F</sub>	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t <sub>D</sub>	CLKA	Duty Cycle	15-pF Load at 1.4V	40.0	53.0	%
F <sub>I</sub>	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F <sub>I</sub>	XTALIN	Input Frequency	External Input Clock <sup>[7]</sup>	1	30	MHz
F <sub>O</sub>	CLKA	Output Frequency	CY2907I, 15-pF Load	0.5	80.0	MHz
			CY2907FI, 15-pF Load	0.5	66.6	MHz
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	25 MHz to 100 MHz		150	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	14 MHz to 25 MHz		200	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	25 MHz to 120 MHz	-250	+250	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	14 MHz to 25 MHz	-500	+500	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t <sub>PU</sub>		Power-up Time			18	ms
t <sub>FT</sub>	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

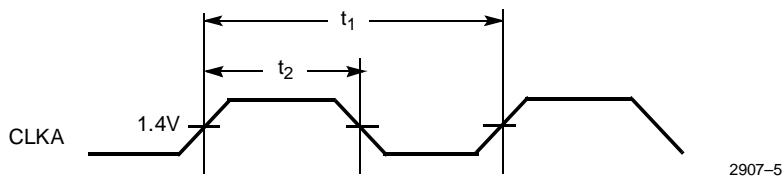
## Switching Waveforms

### Frequency Select Change (Transition Time)

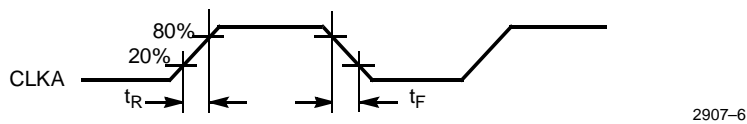


### Duty Cycle Timing

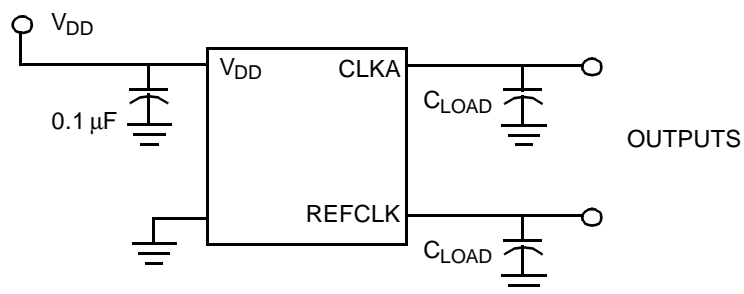
$$t_D = t_2 \div t_1$$



### All Outputs Rise/Fall Time



## Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

## Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2907SC-xxx	S8, S14	8-pin or 14-pin SOIC	5.0V, Commercial, Factory Programmable
CY2907SL-xxx	S8, S14	8-pin or 14-pin SOIC	3.3V, Commercial, Factory Programmable
CY2907SI-xxx	S8, S14	8-pin or 14-pin SOIC	5.0V/3.3V, Industrial, Factory Programmable
CY2907F8	S8	8-pin SOIC	5.0V/3.3V, Commercial, Field Programmable
CY2907F8I	S8	8-pin SOIC	5.0V/3.3V, Industrial, Field Programmable
CY2907F14	S14	14-pin SOIC	5.0V/3.3V, Commercial, Field Programmable
CY2907F14I	S14	14-pin SOIC	5.0V/3.3V, Industrial, Field Programmable
CY3670		Cypress FTG Programmer	Custom Programming for Field Programmable Clocks

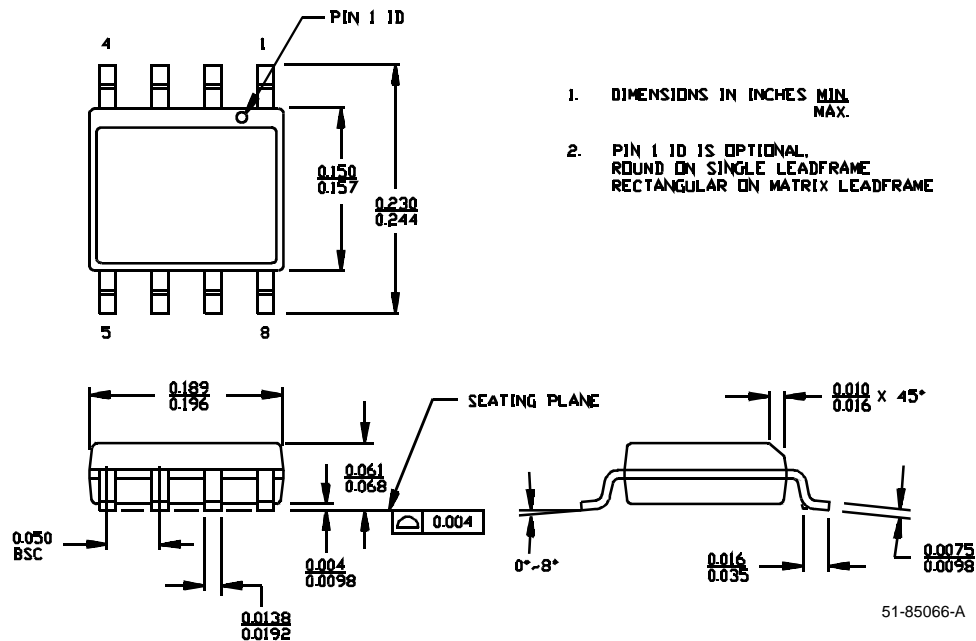
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## Package Characteristics

Package	$\theta_{JA}$ (C/W)	$\theta_{JC}$ (C/W)	Transistor Count
8-pin SOIC	170	35	5436
14-pin SOIC	140	31	5436

## Package Diagrams

8-Lead (150-Mil) SOIC S8





Package Diagrams (continued)

14-Lead (150-Mil) SOIC S14

