Programming the W30X Series Clock Generators

Introduction to Cypress W30X series parts

Overview

This application note provides a description, from a users point of view, of the individual register and bit functions of the Cypress W30X series of clock generators. It is intended as an aid to those who are and will be using the device in their designs or efforts. It also provides a global view of the programming and usage of the device's "Watchdog Timer" circuitry.

The Cypress semiconductors W30X series of clock generator components contains a standard SMbus control interface so that the host system may read and control the configuration of its electrical functionality.

These devices contain 18 control registers. Each register contains 8 data bits and are described, in programming terms, as being SMBus slave device Byte 0 through Byte 17. And they are further subdivided into Bits 0 through 7 of each Byte.

These control bytes may be accessed in 3 distinct ways. The methods are:

1. Byte (8-bit word) read and write commands
2. Page read and write commands
3. Block read and write commands

Byte reading and writing is used to read or write data into any desired single register byte in the device.

Page read and write operations are much like the byte read and write operations. The difference being that bytes are read or written into two or more sequentially increasing numbered registers. Here the starting address is specified and the byte writing sequence is terminated by a stop condition occurring on its SMBus data and clock line.

Block read and write operations are performed also into single or sequentially increasing byte numbered registers. This operation is exactly like the page operation. The difference being that no start address is provided by the host. A starting address of 00 is inferred and the operation is terminated by the host issuing a valid clock/data stop condition.

To operate correctly, the W30X device expects a valid bus start condition followed by either a 2 or 3 byte preamble to be sent to the device to set it up to execute the desired commands function. The length of the preamble depends on the command mode (byte, page, or word) being used.

ADDRESS BYTE

After the start condition, the first byte of data sent to the device, to begin a register access, is the address byte. This byte contains the data value D2 (H) 1101 0010(B) if the operation is to be a write operation (data being written from the external controller (master) into the W30X slave device). If the command will be used to read the contents of the device W30X registers), then the address byte data will be D3 (H) 1101 0011(B).

COMMAND BYTE

The second byte that is sent to the device is the command byte. Further, if Bit 7 (the MSB) of this command byte is a logic 0 then the command will be understood to be a block command. In the case of a block command all eight bits of this byte must be logic 0s and, a third byte (the byte count) is then sent.

For byte and page operation Bit 7 (the MSB) of the command byte is set to a logical 1 state. When this is done the lower seven bits of the command byte become an offset value. This value is used as an index pointer that indicated the beginning byte that will be accessed by the command. For example if the command word is 1000 0011(B) then the first register accessed by the command will be Byte 3.

BYTE COUNT BYTE

In the case of a block read, the third byte (after the start condition occurs) is the byte count. This data signifies the quantity of registers being accessed. All W30X devices ignore this data. The device will continue to receive incremental register data until either all registers have been written or a valid SMBus stop condition is detected. This is action is regardless of the byte count value that has been sent.

STARTING BYTE (Register) VALUE

In the case of page and byte operations the third byte contains the starting byte (register) address that the command will initially read or write.

Data Register 0 (BYTE 0)

Data register 0; Bits 0 through 2 enable or disable the devices EMI reducing spread spectrum frequency modulation feature. Furthermore, they are used to select the actual width or percentage of spread that the device will produce. One unique selection is used, set all outputs to a three-stated or floating condition and another is used to bypass the internal PLL with the input clock so that steady state (static) device and board level testing may be performed.

Bits 3 through 7 are used to select the devices output frequencies from an internal pre-programmed table. Please refer to the data sheet (*Table 5*) for the available frequencies.

Data Register 1 (BYTE 1)

This byte has dual functionality. Here Bits 3 through 7 are only readable. When read, they will return the values of the devices internally latched power up pins values. These reflect the logic values that were programmed on the devices external physical pins (11, 12, 34, 35 and 56) when it initially had power applied to it.

Bit 1 is a read/write bit. When written to it is used to enable or disable the REFX2 clock that appears on the devices physical pin 3. When read from it indicates the status of this control bit.

Bit 2 is reserved by Cypress and must be driven to a logic 0 whenever any writing operation is performed to this byte (register) to guarantee that the device will function to data sheet specification.

Data Register 2 (BYTE 2)

Byte 2 is used to control the enabling and disabling of the devices PCI (0:7) output clocks. Unused clocks should be turned off (disabled) by writing logic 0 the appropriate bits. This will reduce potential EMI issues and also device power dissipation from arising. The current status of these clocks may be queried at anytime by reading this register.

Data Register 3 (BYTE 3)

Byte 3 is used to control the enabling and disabling of the devices 3V66, APIC and the CPU clocks output. Unused clocks should be turned off (disabled) by writing a logic 0 to the appropriate bits. This, again, will reduce potential EMI issues and also device power dissipation.

Data Register 4 (BYTE 4)

Byte 4 is used to control the enabling and disabling of a portion of the device's SDRAM clocks output. Unused clocks should be turned off (disabled) by writing a logic 0 the appropriate bits. This will reduce potential EMI issues from arising and also device power dissipation. These clocks are typically turned off when and by the system BIOS when it senses memory sockets that do not contain any memory modules during power-up memory detection and mapping. SDRAM clocks that are not physically implemented in a specific design should be turned off during this time also.

Data Register 5 (BYTE 5)

Byte 5, like Byte 4, is also used to control the enabling and disabling of a portion of the device's SDRAM clocks output. The high three bits of this register (Bits 5 through 7) must be programmed to a logic 0 state to ensure the part functions to data sheet specifications.

Data Register 6 (BYTE 6)

Byte 6 is a read only register. Performing write operations to this register will have no effect on the device. When read back by the controlling host two pieces of information are retrieved. The first is the Vendors ID data. This is contained in the register's lowest 4 bits. The W30x series of components will always return Bits 0, 1 and 2, LOW and Bit 3, HIGH (8(H)) to identify the part as being manufactured by Cypress Semiconductor Incorporated. This ID nibble (4 bits) is returned by all Cypress manufactured parts if an ID register has been implemented for that device.

The high order nibble (4 bits) will return the unique revision ID number of the physical part being interrogated. This nibble data can be used to insure that when different revisions of the same socket compatible device can be substituted on a PCB assembly the system can identify the device and verify that the correct component is in place.

Data Register 7 (BYTE 7)

Byte 7 is used to control the enabling and disabling of the 24_48MHZ and 48MHZ clocks. It also provides a mechanism to control the output drive levels of these clocks. This byte is a system dependent register and is usually programmed, by the system BIOS, in the same way at initial power-up depending on the physical system the device is present in.

Data Register 8 (BYTE 8)

Byte 8 is used to control the device's "Watchdog" timer and the programmable PCI skew bits.

The intent of the Watchdog Timer is to supply the system with a hardware mechanism by which to recover from an expected and possible catastrophic lockup condition without operator intervention. It is anticipated that the "reset" output pin of the device will be electrically and logically "OR" tied with the systems soft (front panel) reset circuitry. Since the Watchdog's output (the reset pin) is an open drain buffer, in its passive state it does not electrically drive (sink or source) current from external circuitry. When activeit pulls down the circuit that it is connected to thereby sinking current from it.

The MSB of this register controls the granularity of the individual countdown ticks of the timer. Their value may be set to either 150 m/s or 2.5s depending on the state of this bit. Bits 1 through 5 control the actual skew value by specifying the exact number of these time ticks that will occur between the time the timer is triggered and the time the reset pin of the device will be driven LOW by the timer's terminal count detection circuitry.

The two MSBs (Bits 6 and 7) permit the user access to control the timing skew between the APIC and 3V66 clocks and all of the PCI clocks. The three vials settings are in phase (data sheet spec values), 500 ps Leading and 500 ps lagging the data sheet values, The 10(B) setting is invalid and must not be used.

Data Register 9 (BYTE 9)

Byte 9 is used to control drive strength of SDRAM and PCI clock output buffers, select the programmed source of the operating frequency and access various watchdog control and status bits.

Bit 6 and 7

These bits are used to control the drive strength of the SDRAM (bit 7) and PCI (Bit 6) output buffers. They operate in the same way that is used in Register (Byte 7) Bits 5 and 6. This allows the user a mechanism to tune edge rates and, to a small extent, the timing of these clocks to all other system events.

Bit 5

This is one of two bits used to control which frequency specifying sources is used to program the device's main PLL. See the flow chart in this applications note to see its functionality.

If it is set to a logic 0 then the data value that was latched into the power-up register (was on pins 3, 11, 12, 13 and 23 at the time the device as initially powered up) will be used (if the SMBus register is not selected).

If this bit is set to a logic 1 then register 0 Bit 3:7 will define the data source that is used to control the PLL (if the SMBus register is not selected).

Bit 4

Reset on Enable on terminal count of Watchdog Timer:

There are two conditions that will generate a reset pulse on pin 30. This bit enables the pulse to occur ANY TIME the Watchdog Timer times out (counts down to 0). It is one of the

intended functions of the watchdog timer to have an applications program start the counter and set this bit when a possible system hang condition might be expected. If no hang condition occurs then the applications program resets the bit before it can reach terminal count. If the system hangs then the program cannot reset the bit and the reset output pulse resets the system and initiates a recovery process.

Bit 3 (R/W)

Reset Enable on Frequency Change:

There are 2 conditions that will generate a reset pulse on pin 30. This bit enables the pulse to occur ANY TIME the devices frequency is changed, This can occur either by having the M and N registers written to or by having a new selection made from the devices frequency table (writing byte 0 of the device). When this occurs the device generates a reset pulse as soon as the SMBus write operation's stop condition is detected by the device.

Bit 2 (R/W)

Watchdog Timer time out status bit:

This bit indicates if the Watchdog Timer has reached its terminal count. It is most useful when an applications program is attempting to discover if the clock generator has had its Watchdog Timer enabled, was triggered and has subsequently reached terminal count without any intervention. In application this bit is tested by system or utility software to determine whether the system has recently had a hardware reset event due to the Watchdog Timer reaching its terminal count. Also this bit is used to indicate if the program has endured a possible catastrophic running condition that the Watchdog Timer needs to be cleared, Reading this bit returns its state. Writing a logic 1 to this bit causes (if the bit is a logic 1) the logic state read from the device to be reset to a 0. This is usually done in anticipation of the device being initialized for Watchdog Timer usage.

Bit 1

Watchdog Timer enable bit:

This is a write only bit. Setting it to a logic 1 state enables the Watchdog Timer. Once enabled it will begin its countdown if a frequency change occurs and Byte 9 Bit 3 is set (to a logic 1). When a watchdog time out event occurs the device locks itself into a recovery mode. In this mode all frequency changes to the device are locked out until the device is reset from its "recovery mode" using this bit.To cause the device to exit its "recovery mode" this bit must be written with a 0.

Bit 0

Bit 0 is reserved for Cypress use and must always be set to a logic 0 state when writing this SMBus byte.

Data Register 10 (BYTE 10)

Byte 10 is used to control the skewing of specific clock groups that the device creates. The intent is to permit the designer the functionality of adjusting system timing in completed products without PCBA changes. This often occurs when timing margins are not what they were calculated to be or when devices (such as SDRAMs) have more or less loading capacitance on the clock pins than was expected.

Bits 5 through 7 permit changing the skewing of the CPU clocks to the other clocks in the rest of the device. See the data sheet for the specific step values. A positive number indicates that the clocks will occur earlier and a negative value indicates that they will occur later (with respect to the reference clock.

Bits 4 through 2 permit changing the skewing of the SDRAM clocks to the other clocks in the rest of the device. See the data sheet for the specific step values. A positve number indicates that the clocks will occur earlier and a negative value indicates that they will occur later (with respect to the reference clock).

Bits 1 through 0 permit changing the skewing of the AGP clocks to the other clocks in the rest of the device. See the data sheet for the specific step values. A positive number indicates that the clocks will occur earlier and a negative value indicates that they will occur later (with respect to the reference clocks).

Data Register 11 and 12 (BYTE 11 and 12)

Byte 11 is used to access the devices PLL N register that may be used during Watchdog recovery. When and if the Watchdog Timer times out it will cause a reset pulse to be generated. The most common reason the timer times out is that an attempt was made to raise the system operating condition beyond its ability to run at that frequency. When this "time-out" event occurs both the reset pulse occur and the contents of Byte 11 and Byte 12 are loaded into the internal PLL's frequency determining register. It is the software programmer's responsibility to load these two bytes with a known safe system operating frequency before arming the Watchdog Timer. Failure to do so may create a system reset condition (when using the Watchdog Timer) that will cause a permanent hang if the Watchdog Timer arrives at its terminal count. See the flowchart in this application note for a graphic explanation of this process.

Please refer to the devices data sheet for the formula needed to program these bits correctly.

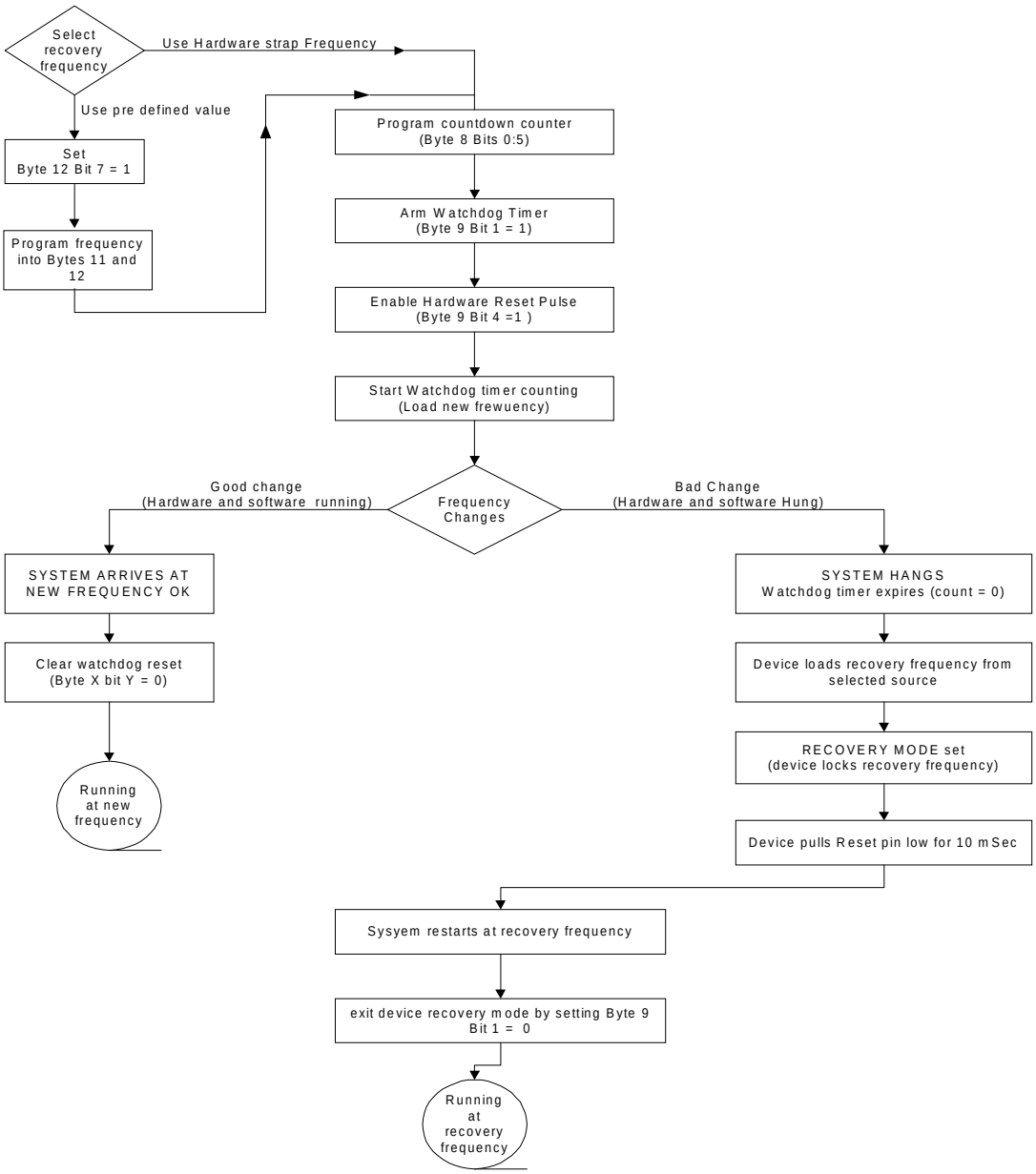
Data Register 13 and 14 (BYTE 13 and 14)

The PLL will take its frequency programming from the devices SMBus registers 13 and 14 if Byte 14 Bit 7 is set to a 1 state. If Byte 14 Bit 7 is a 0 then Byte 9 Bit 5 will control it.

The remainder of the bits in these two SMBus bytes are used to program the devices SMBus programmable frequency feature. See the data sheet for the formula needed to program these bits correctly.

Data Register 15, 16 and 16 (BYTE 15, 16 and 17)

These registers will acknowledge being written to and are reserved. To be guaranteed data sheet specification performance the user must ensure that all bits are logic 0 except for Byte 15, Bits 0 and 1 = logic 1.


Select recovery frequency
Use Hardware strap Frequency
Use pre defined value
Set Byte 12 Bit 7 = 1
Program frequency into Bytes 11 and 12
Program countdown counter (Byte 8 Bits 0:5)
Arm Watchdog Timer (Byte 9 Bit 1 = 1)
Enable Hardware Reset Pulse (Byte 9 Bit 4 =1)
Start Watchdog timer counting (Load new frewuency)
Frequency Changes
Good change (Hardware and software running)
Bad Change (Hardware and software Hung)
SYSTEM ARRIVES AT NEW FREQUENCY OK
Clear watchdog reset (Byte X bit Y = 0)
Running at new frequency
SYSTEM HANGS Watchdog timer expires (count = 0)
Device loads recovery frequency from selected source
RECOVERY MODE set (device locks recovery frequency)
Device pulls Reset pin low for 10 mSec
Sysyem restarts at recovery frequency
exit device recovery mode by setting Byte 9 Bit 1 = 0
Running at recovery frequency