RoboClock® Family Test Mode

This application note discusses the Test mode capabilities of the RoboClock® family. It begins with an introduction to these devices and then discusses how to use the Test mode features.

Introduction

The RoboClock family consists of seven parts: two RoboClocks (CY7B991/2), a 3.3V RoboClock (CY7B991V), a high speed RoboClock+ (CY7B9911), a 3.3V high-speed Roboclock+ (CY7B9911V) and two Robo Jr. devices (CY7B9910/20). The CY7B991/10/11 has TTL outputs, CY7B991V/11V LVTTL outputs and the CY7B992/20 has CMOS (0 to V_{CC}) outputs. Each device will drive 50Ω terminated transmission lines. *Figure 1* shows the PLCC and LCC pin configurations for the RoboClock and RoboClock+ devices.

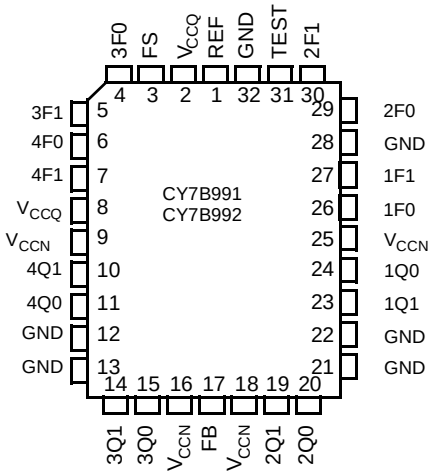

Figure 1. PLCC and LCC Pin Configuration

RoboClock (*Figure 2*) employs a phase-locked-loop architecture. Connecting an output to the FB (feedback) input of the device causes the PLL to synchronize and align this output both in phase and in frequency with the REF (reference) input. This results in very low input to output delay and allows a system to connect RoboClocks in parallel for clock distribution while maintaining very low skew between various clocks from different devices.

RoboClock contains eight outputs grouped in four sets of two. Two function select lines (xF0, xF1) control the functionality of each pair of outputs (xQ0, xQ1). The outputs of an output pair operate identically.

Each pair of three-level function select inputs allows you to hardwire the operation of each output pair to one of nine delay or functional configurations. Each function select input pin can be connected to V_{CC} (HIGH), left unconnected (MID), or connected to ground (LOW). *Table 1* shows the programmable skew configurations available on each output pair. The function select configurations in *Table 1* assume that the output connected to FB is set for "zero" skew.

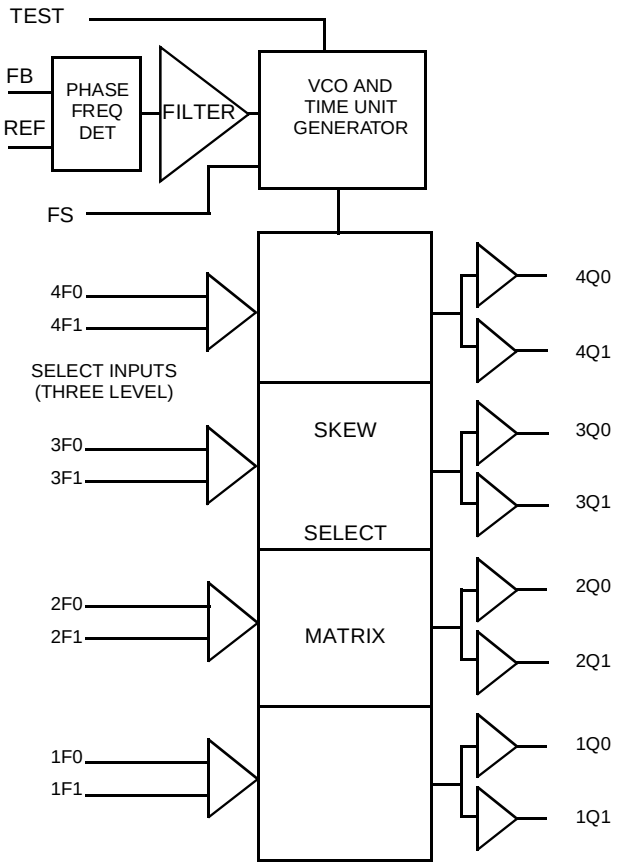

Figure 2. RoboClock Block Diagram

Table 1 shows the range of t_U over which an output may be skewed with respect to the REF input. t_U is a function of the frequency at which the 1Q0 output is operating. RoboClock offers frequency coverage with three ranges from 15 MHz to 80 MHz (100 MHz for the CY7B9911, and 110 MHz for the CY7B9911V) with the use of the three-level FS (frequency select) input. *Table 2* shows the operating frequency range for each of the three levels of FS. The appropriate FS level selection must be made such that the anticipated operating frequency of the 1Q0 output is within the specified limits. There may be two acceptable levels for the FS pin when operating at certain frequencies. The appropriate connection of the FS pin, in this case, would be based on the value of the time unit, t_U, required for the application. *Table 2* also shows an equation that can be used to calculate t_U as well as the approximate operating frequency where t_U is equal to 1 ns.

Table 1. Programmable Skew Configurations

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	**1F0, 2F0, 3F0, 4F0**	**1Q0, 1Q1, 2Q0, 2Q1**	**3Q0, 3Q1**	**4Q0, 4Q1**
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Table 2. Frequency Range Select and t_U Calculation

	f_{1Q0} (MHz)		$t_U = \frac{1}{f_{1Q0} \times N}$	
FS	**Min.**	**Max.**	**where N=**	**Approximate Frequency At Which t_U = 1.0 ns**
LOW	15	30	44	22.7 MHz
MID	25	50	26	38.5 MHz
HIGH	40	80[1]	16	62.5 MHz

Note:

1. The upper frequency limit for the CY7B9911 is 100 MHz. The LV CY7B9911V has an upper limit of 110 MHz.

For example, according to *Table 2*, a system using RoboClock with a clock speed of 33 MHz would leave the FS pin unconnected. The programmable time unit, t_U, based on this operating frequency, would be

$$t_U = \frac{1}{f_{1Q0} \times N} = \frac{1}{33MHz \times 26} = (1.17ns) \quad \text{Eq. 1}$$

In other words, you can adjust the position with which the rising and falling edges of the outputs move with respect to the corresponding REF input edge with a resolution of 1.17 ns when operating the device at 33 MHz. At 25 MHz, the t_U could be either 0.91 ns or 1.54 ns depending on whether the FS pin is tied LOW or left unconnected, respectively.

Test Mode Features

In some situations you may need to stop the PLL of the device. For instance, in many board-level testing applications you may need to supply a clock input to the system that may not meet the REF input requirements of RoboClock. This scenario can occur in bed-of-nails testing or single-step microprocessor execution. Use of the TEST input of RoboClock will allow operation in single-step mode.

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing RoboClock to operate as previously explained. (For testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase-locked-loop disconnected. The TEST input must be forced to less than 1V (0.13*Vcc for the low voltage (LV) parts) to insure its LOW level, to $V_{CC}/2 \pm 500$ mV (Vcc/2±100 mV for the LV parts) to insure its MID level, and to $V_{CC} - 1V$ (0.87*Vcc for the LV parts) to insure its HIGH level.

When RoboClock is put in Test mode, after a few REF cycles, input levels supplied to REF will appear at all outputs after a 15- to 80-ns delay. The circuit effectively becomes a long chain of delay elements. The level on the TEST input affects the length of time it takes for the REF signal to propagate through each delay element. When the TEST input is forced HIGH, each delay element will be selected to have its shortest delay (< 700 ps). This is known as “contracted” mode. When the TEST input is forced to its mid state, the delay through each element will be as long as possible (> 1.5 ns). This is referred to as “extended” mode.

The level placed on the FS pin also determines the operation of RoboClock when it is in Test mode. The FS input is used to control the number of delay elements that the REF input will propagate through, as shown in *Figure 3*. When FS is held HIGH, REF will pass through only the last 13 delay stages. When FS is placed in the MID or LOW position, REF will propagate through all 22 delay elements.

In contrast with normal operation (TEST tied LOW), FB will not have any affect on the operation of the outputs. All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Outputs that have the divide-by-two output configuration selected will change state at every second REF input, and outputs that have the divide-by-four option selected will change state at every fourth REF input. An output selected for inverted operation will drive the opposite sense of the REF input.

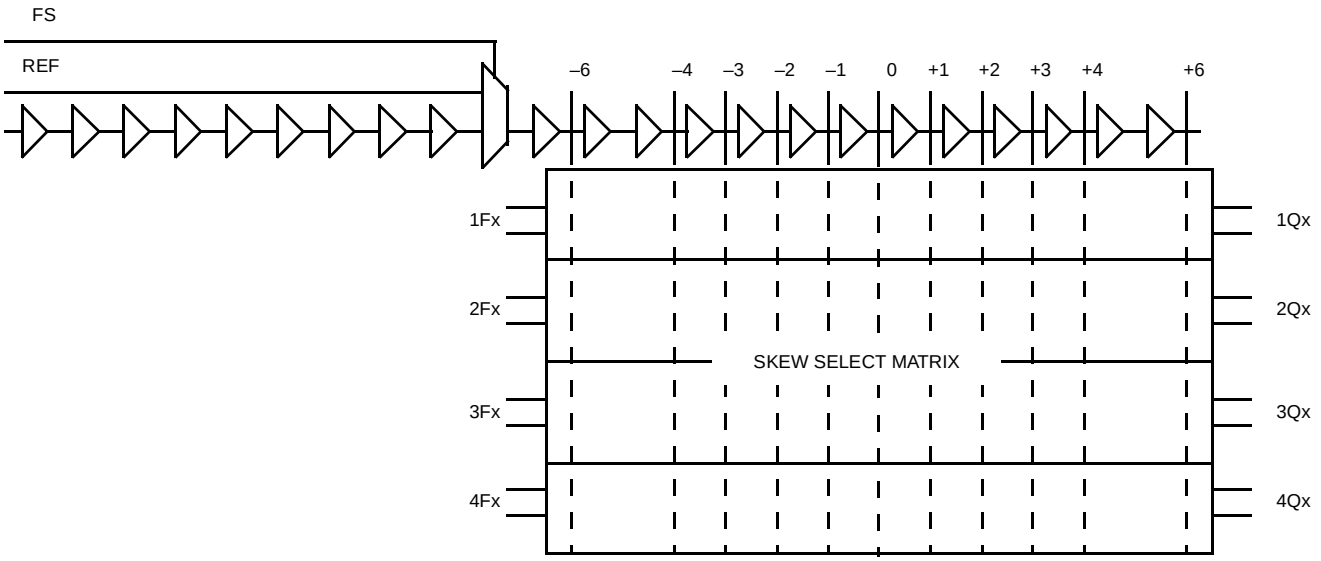

Figure 3. RoboClock Test Mode

A counter reset is available for the divided outputs. To reset the counters, the 3F0 and 4F0 function selects must be placed in their MID position and a clock applied to the REF input. If the 3Qx or 4Qx outputs are then selected for a divided function (3Fx = LOW, LOW, HIGH, HIGH or 4Fx = LOW, LOW) then the 4Qx or 3Qx outputs will be in their HIGH state. The first REF clock will cause these outputs selected for divided operation to transition LOW and, subsequent REF clocks will cause these outputs to continue their normal output divided output pattern.

Conclusion

RoboClock's Test mode feature stops the phase-locked-loop allowing board-level testing and evaluation. This mode allows operation at frequencies below the minimum operating frequency. It also provides the ability to apply input pulses with varying width and period to the device without requiring the cycle-to-cycle frequency accuracy necessary to keep the feedback loop in lock.

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