White Paper

The Blossoming Need for Advances in Frequency Timing Generators

Over the past twelve months, no other single component used in motherboard designs has grown in its complexity as has the Frequency Timing Generator (FTG). The basic function of an FTG is to take as input a common, inexpensive 14.318-MHz or other crystal, and provide all the timing signals necessary to run the digital components of the computer, or some other digital system.

The FTG became a critical building block for the computing system with increasing system frequency, compounded by an increasing number of timing signals needed to support synchronous memory architecture. *Figure 1* shows the peak operating frequency of Intel x86 processors produced since 1989. Over the last decade, CPU operating frequency increased at an average rate of 46% a year. The corresponding peak memory burst rate now reaches 400 MHz with Direct Rambus Architecture. Over the same period, the average number of timing signals in the system increased from eight to thirty-six.

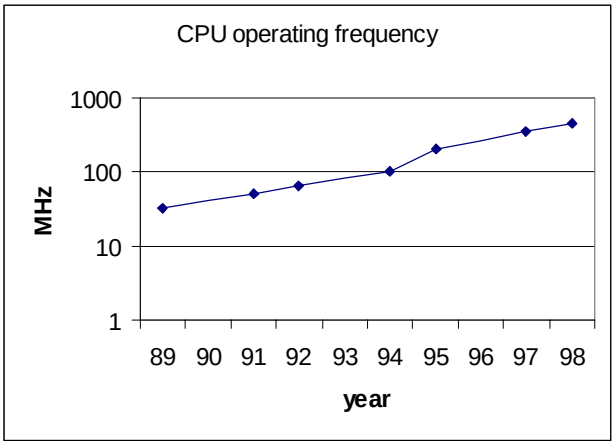

Figure 1. Peak Operating Frequency of Intel x86 Processors Produced Since 1989

By 1997, the challenges posed by high system speeds and synchronous architecture had changed the requirement for FTG vendors from merely churning out simple products quickly to offer a cost reduced timing solution into a collaborative effort with system designers to address implementation concerns.

One of the most significant implementation concerns being addressed by FTGs today is EMI (Electro-Magnetic Interference). EMI is the root cause when electronic or electro-mechanical equipment interferes with other electronic equipment, for example you turn on your hair dryer and new static appears on your TV or radio signal. The FCC and other regulatory agencies around the world have established specific limits for the amount of peak EMI they allow to radiate from any device sold in their sphere of control.

Why is a long-standing issue like EMI control suddenly blossoming into an opportunity for FTG vendors? There are a variety of reasons. System speeds are increasing to the point that existing methods for affecting the level of radiated EMI are unable to control it inexpensively enough. Implementation of Wireless Local Loops in the home environment has increased the sensitivity to EMI around the house. At the same time regulatory agencies have altered the landscape with 'open box' tests for anything which might be used without a case around it.

Historically, system designers have addressed EMI by adding more power and ground planes to their boards, using passive components to affect wave shapes, adding common mode chokes or ferrite beads, using metal shielding in their casing, and/or using better, more expensive gaskets. Additionally, once sample boards were available, EMC engineers might tinker with the passive component values and layout to reduce EMI at any specific frequency exhibiting dangerously high levels. With the regulations regarding open box testing, one of a designers easiest-to-use tools (shielding) has been taken away. SSFTGs allow designers to cut back some of their other efforts, simplifying the design effort and thereby reducing the amount of time required to complete their project.

The peak EMI margin gained by enabling the SS function on an FTG can also be applied to reducing the noise limitations on other devices. A higher noise tolerance on other board components provides an avenue for additional cost savings and the security of alternate sourcing.

Regulated EMI limits are peak limits. SSFTGs do not reduce the radiated power, rather they distribute it over a range of frequencies. Standard FTGs are significant contributors to peak EMI because they are designed to provide a constant single frequency, and as a result all their energy is emitted at that specific frequency and its harmonics. SSFTGs are designed to provide a signal whose frequency is swept in a slow and controlled method through a defined range. This reduces the peak EMI of not only the signal and its harmonics, but also the peak EMI of any other signal on board that is synchronized to it.

SSFTGs have existed for a few years now, and have proven their worth not only in motherboards, but also in a wide variety of other applications from peripherals (such as printers) to set top boxes and home video game systems.

This Is Not Your Father's Spread Spectrum

The term 'spread spectrum' as it applies to timing technology needs to be understood separately from other technologies using the same term. Let's start by further exploring why the technology was developed.

Energy discharged by electro-mechanical equipment radiates from the equipment. This is described as Electro-Magnetic Interference (EMI). The energy is emitted in the form of waves of magnetic energy. These waves introduce new currents in other electronic equipment that they reach. These new currents affect the signals on the impacted system and, if great enough, will create errors because the designer of this system could not anticipate nor design for every possible type and range of interference that their system might get exposed to.

If one looks at system performance without consideration of the impact it has on its surroundings, it is easy to accept that the ideal timing signal would be one which had a constant period/frequency with rise and fall times nearing zero. This would maximize the percentage of time a designer could utilize. In this ideal world, if a designer needed 5ns of high time and 5ns of low time to accomplish the tasks required in one period, then he could run his system at 100 MHz (=1/10 ns). If he has to allow for 500 ps of jitter, and 2 ns each of rise and fall time, he can then only run his system at around 69 MHz [1/(10 ns+0.5 ns+4 ns)], over a 30% drop in performance (see *Figure 2*). However, in this electronic age, system impacts such as interference are a significant factor.

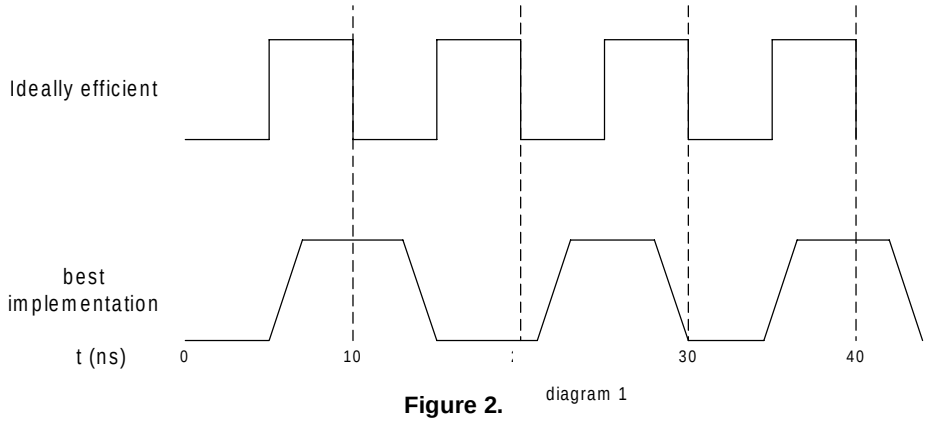

Figure 2.

As we forge ahead, FTG companies will need to continue to find new benefits to offer in order to be successful. In addition, it will be increasingly important to provide significant assistance to our customers as they design with shrinking timing budgets and growing EMC needs. By sharing our knowledge and understanding of how to construct boards around our products, vendors provide potentially significant reduction in time-to-market, which is always vital.

The largest current challenge in the motherboard FTG market is developing clocks to support the new Rambus DRAM architecture. With device speeds four times higher than any previous motherboard FTG, the Direct Rambus Frequency Timing Generator presents new challenges in timing. Characteristics such as skew and jitter must get tighter, and the rise time vs. EMI issue must be addressed again, placing an even higher value on use of an SSFTG.

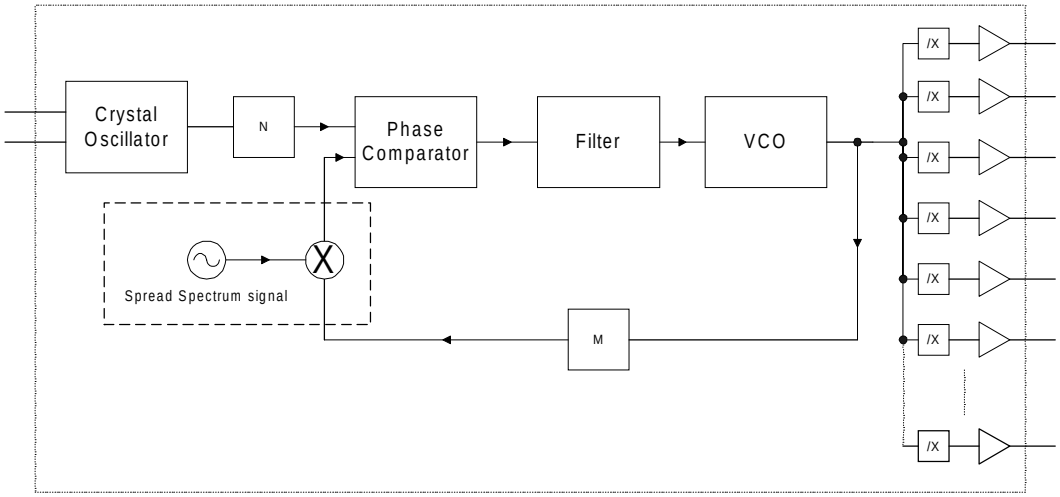

Figure 3.

SSFTG Implementation

FTGs, by their very nature, emit high peak levels of EMI even though they consume relatively little power. This is because the standard FTG discharges that power in a very narrow band of frequency. Spread spectrum FTGs expand the band of frequency by slowly sweeping the timing signal generated through a controlled range of frequencies, in a tightly controlled manner.

The basic implementation concept is that a low-frequency signal is injected into the PLL. *Figure 3* is a simple block diagram of an FTG. The block in dashed lines shows how the spread signal is injected. The waveform, frequency, and magnitude of this signal all have impact on the amount of EMI reduction which will occur.

Triangular and sine waves are easier to implement, however they result in less than optimal peak reduction. Mathematical proofs show the ideal waveform for maximum reduction. This waveform is shown in *Figure 4*, and the resultant effect can be seen in *Figure 5*, a plot in the frequency domain of the power discharged.

The implementation depicted in *Figure 5* is referred to as 'center spread'. In some systems, the device being driven by the FTG has a certain minimum period, which would be used to calculate the frequency of a non-spread FTG. In such instances, a 'down spread' version can be developed which changes nothing else, but moves the center spike of *Figure 5* over to the far right so that the maximum frequencies of both spread and non-spread are equal.

Numerous systems have been tested with SSFTGs in which the EMI is measured with the SS function both enabled and disabled. These tests have shown typical reduction on the order of ~13 dB, and overall variation between 8 and 20 dB, for the harmonics of the signal that was spread.

An important design consideration when utilizing SSFTGs for EMI reduction is downstream PLLs. If a signal with the SS feature is routed through another PLL (either a separate chip like a Zero Delay Buffer, or as an integrated part of an ASIC) the PLL may filter the spreading signal off. For an ASIC, the system may not see a problem, but the whole point of a Zero Delay Buffer is to fan out and synchronize extra timing signals. If the SS feature is filtered off, the intended synchronization will not occur.

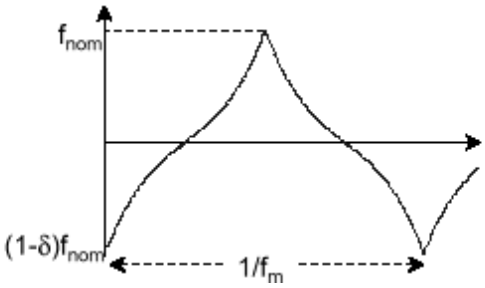

Figure 4.

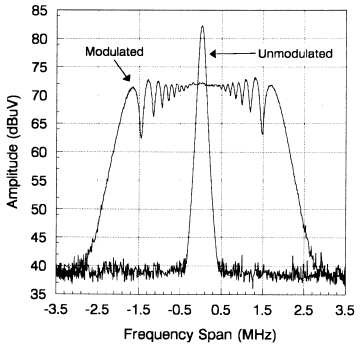

Figure 5.