Terminating RoboClockII™ Outputs

Why RoboClockII™ Outputs Need to be Terminated

Transmission line effects are present on all electrical interconnections. However, these effects only really become a concern with increasing rising and falling edge rates. Given the typical operating frequencies of RoboClock systems, a clear understanding of transmission effects is paramount to proper implementation of the part. This application note will describe transmission line effects and how to accommodate them in your design.

When Does a Trace Become a Transmission Line?

The first step in any analysis is to determine whether your interconnection can be treated as a simple trace or whether you have to adopt transmission line rules. A good rule of thumb involves comparing the rise time of the driver to the propagation delay of the trace you're driving. If the round trip delay of the trace (twice the propagation delay) is greater than the faster of the rise or fall time, the transmission line effects will not be masked by the rising (falling) edge of the driving device. Thus, the rise (fall) time and propagation delay of the trace are principal to transmission line analysis.

Transmission Line Effects on Clock Signals

The cause of transmission line effects is impedance mismatch.

These impedance mismatches occur because of impedance differences between the driver, trace and load. They can also be caused by discontinuities (vias, stubs, different loading, etc.) along the transmission line. Any time the impedance along a transmission line changes, a reflection will occur. Reflections cause ringing, which is voltage overshoot and undershoot above and below the final state of the signal (see *Figure 1*). One way to work around the effects of ringing is to wait until the voltage levels have stabilized. This, however, required the addition of extra clock cycles and can slow down a system considerably. The unwelcome overshoot due to reflections can cause latch-up in a sensitive system. The unwanted over and undershoot will radiate larger fields, thus transferring more crosstalk to neighboring traces. The ringing can also reduce noise margin and induce false clocking.

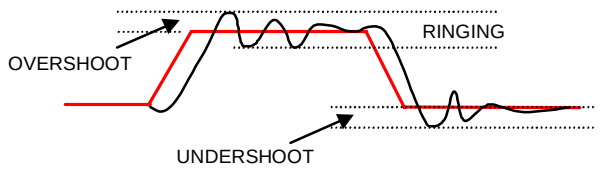


Figure 1. Transmission Line Effects

Sample Transmission Line Calculation

As stated, the two critical parameters that must be analyzed when determining whether to treat a trace as a transmission line are the rising (and falling) time of the driver and the propagation delay of the trace being driven. The rise and fall times of the driver will usually be listed in the device data sheet. The propagation delay for the trace can be calculated using the appropriate formula for the respective transmission line type. The following is a typical analysis for a PCB board with microstrip traces.

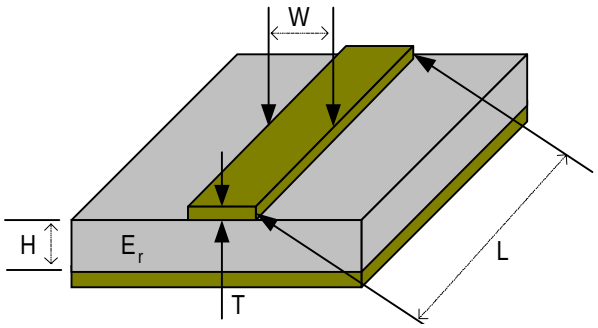


Figure 2. Microstrip

Assume a 5-in microstrip line is being driven by a RoboClockII output with rise time of 1 ns. The line is loaded at the end with 1 device. The load adds 20 pF of capacitance. Is termination required in this instance?

Given W=0.008 in, H=0.005 in, T=0.0025 in, L=5.000 in and E_R=4.6, calculate the impedance and propagation delay of the microstrip trace:

$$Z_0 = \frac{87}{\sqrt{E_R + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) = 43.03\text{ohms}$$

$$t_{PD} = 1.017\sqrt{0.475E_R + 0.67} = 1.718\text{ns/ft} = 0.143\text{ns/in}$$

This is the new one way propagation delay for the 5" trace. The round trip delay is 2 X t_{PD}', 3.436 ns/ft. Again, the trace must be treated as a transmission line if:

$$2 \times t_{PD} \times \text{TRACELENGTH} \geq t_{RISE}$$

$$2 \times t_{PD} \times \text{TRACE LENGTH} = 2 \times 1.718\text{ns/ft} \times 5/12\text{ft} = 1.432\text{ns}$$

Since 1.432 ns is greater than the rise time of the output buffer (1ns), the trace must be treated as a transmission line and termination is required.

Termination Techniques

Transmission line theory states that a signal sent down a transmission line that has constant characteristic impedance will propagate undistorted along the line. At the load a voltage reflection will occur if the load impedance is not equal to that of the line. The goal of transmission line termination is to match the source and/or load impedance to that of the transmission line. This ensures an optimal delivery of the signal to the load. There are several methods of transmission line termination, all with their own advantages and disadvantages. The two most popular termination techniques employed with clock lines are Thevenin and series termination.

Thevenin Termination

Thevenin termination attempts to match the load impedance with that of the transmission line. It employs the use of a pull-up and pull-down resistor to achieve this (see *Figure 3*). The Thevenin equivalent resistance is set equal to the characteristic impedance of the trace, Z_0. A disadvantage of this termination technique is the DC current path from V_{CC} to GND through the termination. Thevenin termination also uses more components than series termination.

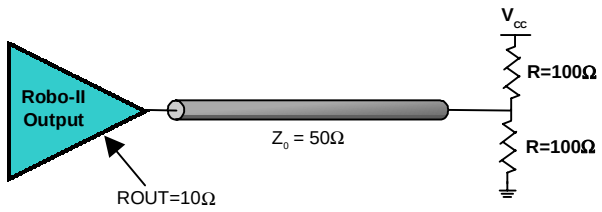


Figure 3. Thevenin Termination.

Series Termination

The objective of series termination is to match the source impedance with that of the transmission line. The value of the series resistor is chosen such that the series combination of the output impedance of the source driver and the series resistor is equal to the characteristic impedance of the transmission line. This configuration will then absorb any reflections from the load. However, this only works if there is a no DC load. This may not be as straightforward as it seems though, as drivers can have different HIGH-to-LOW and LOW-to-HIGH output impedance. RoboClockII's output buffer is designed to have the same output impedance when driving both HIGH and LOW. This is typically about 10Ω. Series termination is a good choice when power dissipation is critical and the load is a capacitive load. With this termination, however, loads must be located at the end of the trace. The series-terminating resistor should be placed as close as possible to the RoboClockII output.

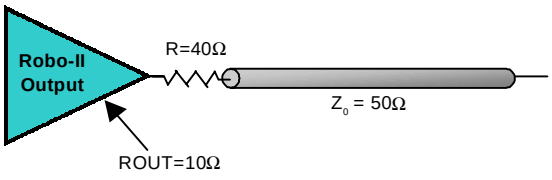


Figure 4. Series Termination

Either of the above schemes can be used to terminate RoboClock outputs. The data sheet specifications are quoted and tested based on the Thevein termination shown in *Figure 3*. Thus, specifications may vary slightly for different termination techniques.

Driving Multiple Loads

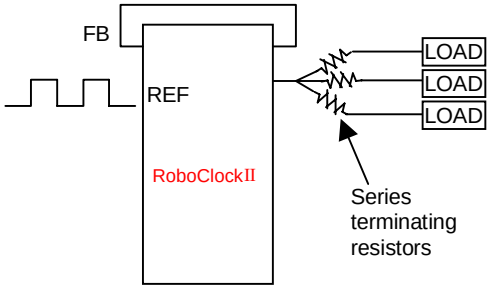


Figure 5. Multi-Series Termination

For point to point connections, either series or Thevenin termination suffices. However, when driving multiple loads, series termination should be employed. A star network should be configured with a series-terminating resistor for each load as illustrated in *Figure 5*. The value of the series resistor in this case is calculated using the following equation:

$$R_{SERIES} = Z_0 - \left(\frac{10}{\text{Number of Traces}} \right)$$

If layout constraints prohibit this, or if you are daisy chaining loads, the configuration in *Figure 6* should be used. Note the resistor values in this instance should be about 100Ω. Thevenin termination should not be used if you are driving three or more loads. This is due to the fact that the effective resistance of the combined termination may be too low for the driver to drive.

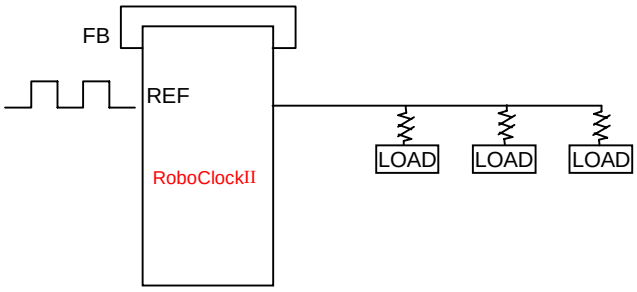
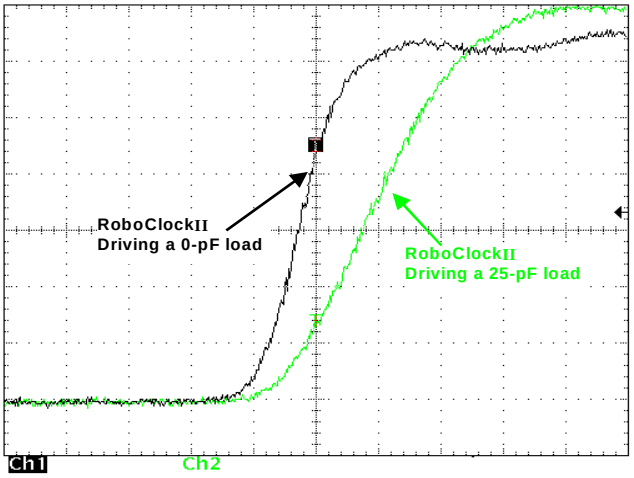


Figure 6. Alternative Method for Terminating Multiple Loads

The Effects of Capacitive Load

When a trace is loaded with devices, the load capacitance adds to the trace's capacitance. A heavily loaded trace slows the rise and fall times of the driver due to the increased RC time constant associated with the load capacitance.

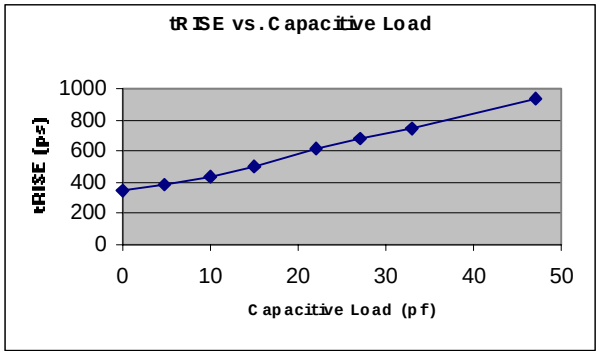
The RoboClockII outputs are designed to drive a capacitive load of up to 25 pF. The effects of capacitive load on the rise time of the output buffers are illustrated in *Figure 7*, which compares a RoboClock-II output buffer driving a 0-pF load and a 25-pF load.



This 'scope waveform compares the rise time of an output loaded with a 25-pF load to that of an unloaded output. The loaded output has a rise time of 650 ps whereas the unloaded output has a rise time of 310 ps.

Figure 7. A Loaded vs. an Unloaded Output

The data sheet is specified for an output load of 25 pF or less. The effects of capacitive load on rise time are graphed in *Figure 8*. You can use this graph to determine the effects of your capacitive load on the output buffer's rise time under quiescent operating conditions.



This graph shows the effects of capacitive load on rise time. The data here is for typical silicon operating at 24 MHz, at room temperature with a 3.3V V_{CC}.

Figure 8. Capacitive Load vs. Rise Time