Understanding Zero Delay Buffer Programming

Scope

This document outlines the recommended procedure for programming zero delay buffers offered by Cypress. In particular, this document addresses details applicable to the:

- W42B930, 3.3V PLL-Based System Clock Driver
- W42B931, 3.3V PLL-Based System Clock Driver
- W42B950, 3.3V PLL-Based System Clock Driver
- W42B951, 3.3V PLL-Based System Clock Driver
- W42B972, Low Voltage PLL Clock Driver
- W42B973, Low Voltage PLL Clock Driver
- W42B974, 3.3/5.0V PLL Clock Driver

Discussion

A zero delay buffer is used to generate multiple output clocks with rising edges synchronized to the rising edges of the input clock. The frequency of the output signals will be the same frequency, or an integer multiple of the input clock. As an example, if you set the Zero Delay Buffer to double the input clock, every second rising edge of the output clock would be synchronous with an edge of the input clock.

Some of the Zero Delay Buffers offered by Cypress have rather complex multiplication schemes allowing those buffers to produce an integer multiple of the input frequency. To understand how to program these parts, the most basic concepts of the PLL circuit must first be understood.

First, a reference input from a clock source (i.e., crystal, oscillator, or external signal source) is required. The output clock is synchronized to this signal. The second input to the PLL circuit is the feedback signal selected from the available outputs. The on-chip circuitry adjusts the selected output frequency(s) until the positive edges of the inputs to the phase detector (the feedback and reference clocks) are matched. The output frequency(s) speed is/are then equal to the input frequency times the ratio of the corresponding output divisor to the feedback divisor.

Below is a mathematical representation of this calculation:

$f_{VCO} = f_{IN} * D_{FB}$

$f_{OUT} = f_{VCO} / D_{OUT}$

Solving for f_{VCO} yields:

$f_{IN} / f_{OUT} = D_{OUT}/D_{FB}$

OR

$f_{OUT} = D_{FB} / D_{OUT} * f_{IN}$

Where:

f_{IN} = Input frequency
f_{VCO} = VCO frequency
f_{OUT} = Output frequency
D_{FB} = Feedback divisor
D_{OUT} = Output divisor

Table 1. W42B930/931 Multiplication Possibilities

Feedback	D_{FB}	QA, D_{OUT} =		QB, D_{OUT} =		QC, D_{OUT} =	
		2	4	2	4	4	6
Internal	8	x4	x2	x4	x2	x2	x4/3
QA	2	x1	NA	x1	/2	/2	/3
QA	4	NA	x1	x2	x1	x1	x2/3
QB	2	x1	/2	x1	NA	/2	/3
QB	4	x2	x1	NA	x1	x1	x2/3
QC	4	x2	x1	x2	x1	x1	NA
QC	6	x3	x3/2	x3	x3/2	NA	x1

Table 2. W42B950 Multiplication Possibilities

Feedback	D_{FB}	QA. D_{OUT} =		QB, D_{OUT} =		QC0:1, D_{OUT} =		QD0:4, D_{OUT} =	
		2	4	4	8	4	8	4	8
Internal, FB_SEL = 0	16	x8	x4	x4	x2	x4	x2	x4	x2
Internal, FB_SEL = 1	8	x4	x2	x2	x1	x2	x1	x2	x1

Table 3. W42B951 Multiplication Possibilities

Feedback	D_{FB}	QA, D_{OUT} =		QB, D_{OUT} =		QC0:1, D_{OUT} =		QD0:4, D_{OUT} =	
		2	4	4	= 8	= 4	= 8	= 4	= 8
QA	2	x1	NA	/2	/4	/2	/4	/2	/4
QA	4	NA	x1	x1	/2	x1	/2	x1	/2
QB	4	x2	x1	x1	NA	x1	/2	x1	/2
QB	8	x4	x2	NA	x1	x2	x1	x2	x1
QC	4	x2	x1	x1	/2	x1	NA	x1	/2
QC	8	x4	x2	x2	x1	NA	x1	x2	x1
QD	4	x2	x1	x1	/2	x1	/2	x1	NA
QD	8	x4	x2	x2	x1	x2	x1	NA	x1

Table 4. W42B972/973 Multiplication Possibilities

FSELFB0:2	D_{FB}	QA0:3, D_{OUT} =				QB0:3, D_{OUT} =				QC0:3, D_{OUT} =			
		4	6	8	12	4	6	8	10	2	4	6	8
000	4	x1	x2/3	/2	/3	x1	x2/3	/2	x2/5	x2	x1	x2/3	/2
001	6	x3/2	x1	x3/4	/2	x3/2	x1	x3/4	x3/5	x3	x3/2	x1	x3/4
010	8	x2	x4/3	x1	x2/3	x2	x4/3	x1	x4/5	x4	x2	x4/3	x1
011	10	x5/2	x5/3	x5/4	x5/6	x5/2	x5/3	x5/4	x1	x5	x5/2	x5/3	x5/4
100	8	x2	x4/3	x1	x2/3	x2	x4/3	x1	x4/5	x4	x2	x4/3	x1
101	12	x3	x2	x3/2	x1	x3	x2	x3/2	x6/5	x6	x3	x2	x3/2
110	16	x4	x8/3	x2	x4/3	x4	x8/3	x2	x8/5	x8	x4	x8/3	x2
111	20	x5	x10/3	x5/2	x5/3	x5	x10/3	x5/2	x2	x10	x5	x10/3	x5/2

Table 5. W42B974 Multiplication Possibilities

FSELFB0:1	D_{FB}	QA0:4, D_{OUT} =		QB0:4, D_{OUT} =		QC0:3, D_{OUT} =	
		2	4	2	4	4	6
00	4	x2	x1	x2	x1	x1	x2/3
01	8	x4	x2	x4	x2	x2	x4/3
10	6	x3	x3/2	x3	x3/2	x3/2	x1
11	12	x6	x3	x6	x3	x3	x2

Example

A 25-MHz signal is available and copies of 100 MHz, 50 MHz, and 33 MHz are needed to be generated from it. Hence, a x4, a x2, and a x4/3 is required. Scanning the above tables, three possibilities can be found:

- W42B931 with internal feedback, which could provide two copies of each frequency.
- W42B972/3 with feedback selectors of 010, 100, or 110 would provide four copies of each.
- W42B974 with feedback selector 01 would provide five copies each of 100 and 50, and four copies of 33.

Conclusion

Even though on some of the chips above, there are outputs specifically referred to as the feedback output, ANY of the outputs can be selected to be used as a feedback. This opens the door to a wider range of possible divider schemes than are explored in these tables. If you cannot find a solution from these tables, please contact Cypress directly so we may help you find the optimal solution.