Spread Aware™, Eight Output Zero Delay Buffer

Features

- **Spread Aware™—designed to work with SSFTG reference signals**
- **Eight LVCMOS/LVTTL outputs**
- **5.0V power supply**
- **Available in 24-pin SOIC (300 mil) package**

Key Specifications

Operating Voltage: .....5.0V±10%

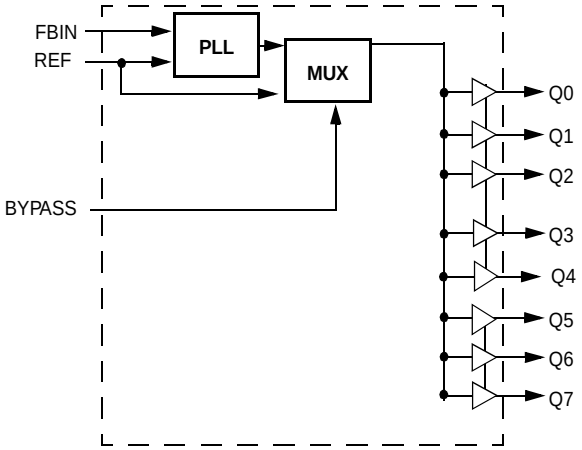
Operating Range: .....30 MHz < f_{OUT} < 35 MHz

Cycle-to-Cycle Jitter: .....<200 ps

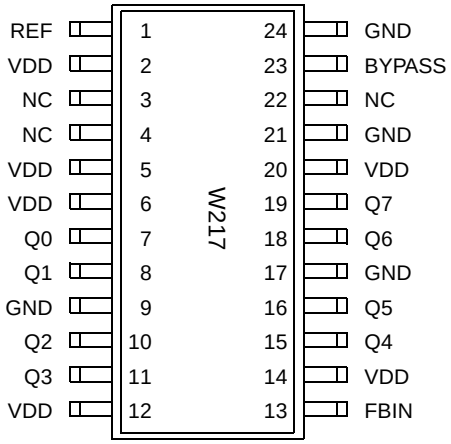
Output to Output Skew: .....<250 ps

PLL Lock Time:.....<25 µs

Block Diagram



Pin Configurations



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
REF	1	I	***Reference Input:*** Output signals Q0:7 will be synchronized to this signal.
FBIN	13	I	***Feedback Input:*** This input must be fed by one of the outputs to ensure proper functionality. If the trace between FBIN and output is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the CLK signal input.
Q0:7	7, 8, 10,11, 15, 16, 18, 19	O	***Integrated Series Resistor Outputs:*** The frequency and phase of the signals provided by these pins will be equal to the reference signal if properly laid out.
VDD	2, 5, 6, 12, 14, 20	P	***Power Connections:*** Connect to 5.0V. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	9, 17, 21, 24	G	***Ground Connections:*** Connect to common system ground plane.
BYPASS	23	I	***PLL Bypass:*** Tie to GND (LOW,0) for normal operation, when brought to V_{DD} (HIGH, 1) the onboard PLL is bypassed, eliminating the 'zero delay' feature.
NC	3, 4, 22	I	***No Connect:*** Leave these pins floating for normal operation.

Overview

The W217 is a PLL-based clock driver designed for use in RAID systems. External feedback allows users to lay out their systems so that the devices being driven by the outputs are accurately synchronized to the clock signal provided as a reference to the W217.

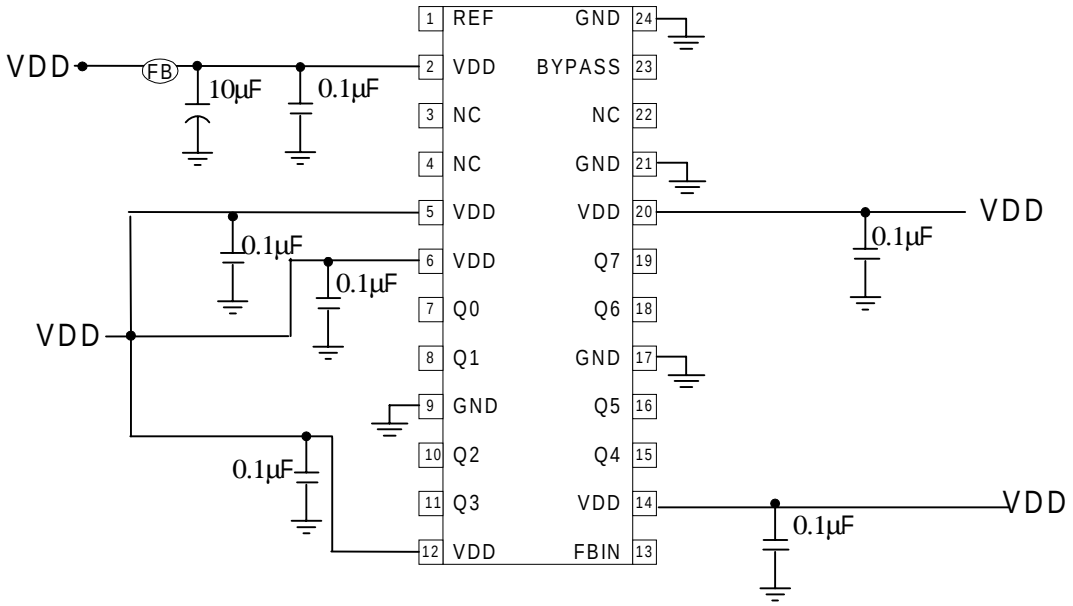


Figure 1. Schematic

Spread Aware™

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.”

How to Implement Zero Delay

Typically, zero delay buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going high at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described below.

External feedback is the trait that allows for this compensation. The PLL on the ZDB will cause the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feed back and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may be affected by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

AC Test Load

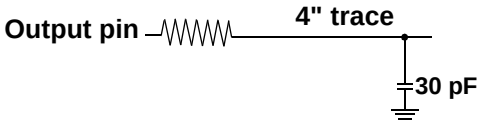


Figure 2. Test Load Schematic

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Exceeding maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
P_D	Power Dissipation	0.75	W

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 5.0V±10%

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current 5.0V	Unloaded, 33 MHz		110	130	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 46 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –16 mA	2.4			V
I_{IL}	Input Low Current - REF/FB	V_{IN} = 0V			500	µA
	Input Low Current - BYPASS				200	µA
I_{IH}	Input High Current - REF/FB BYPASS	V_{IN} = V_{DD}			500 200	µA
C_{IN}	Input Capacitance			10		pF
R_{Out}	Output Driver Impedance			55		Ω

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 5.0V±10%

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{OUT}	Output Frequency	30-pF load	30		35	MHz
t_R	Output Rise Time	0.8V to 2.0V, 30-pF load		1.0	1.5	ns
t_F	Output Fall Time	2.0V to 0.8V, 30-pF load		1.0	1.5	ns
t_{ICLKR}	Input Clock Rise Time[1]				4.5	ns
t_{ICLKF}	Input Clock Fall Time[1]				4.5	ns
t_{PE}	CLK to FBIN Skew[2]	Measured at 1.5V	–250	0	250	ps
t_{SK}	Output to output Skew	All outputs loaded equally	–250	0	250	ps
t_D	Duty Cycle[3]	30-pF load	45	50	55	%
t_{LOCK}	PLL lock time	Power supply stable		7	25	µs
t_{JC}	Jitter, Cycle-to-cycle				200	ps

Notes:

1. Longer input rise and fall time will degrade skew and jitter performance.
2. Skew is measured at 1.5V on rising edges.
3. Duty Cycle measured at 1.5V.

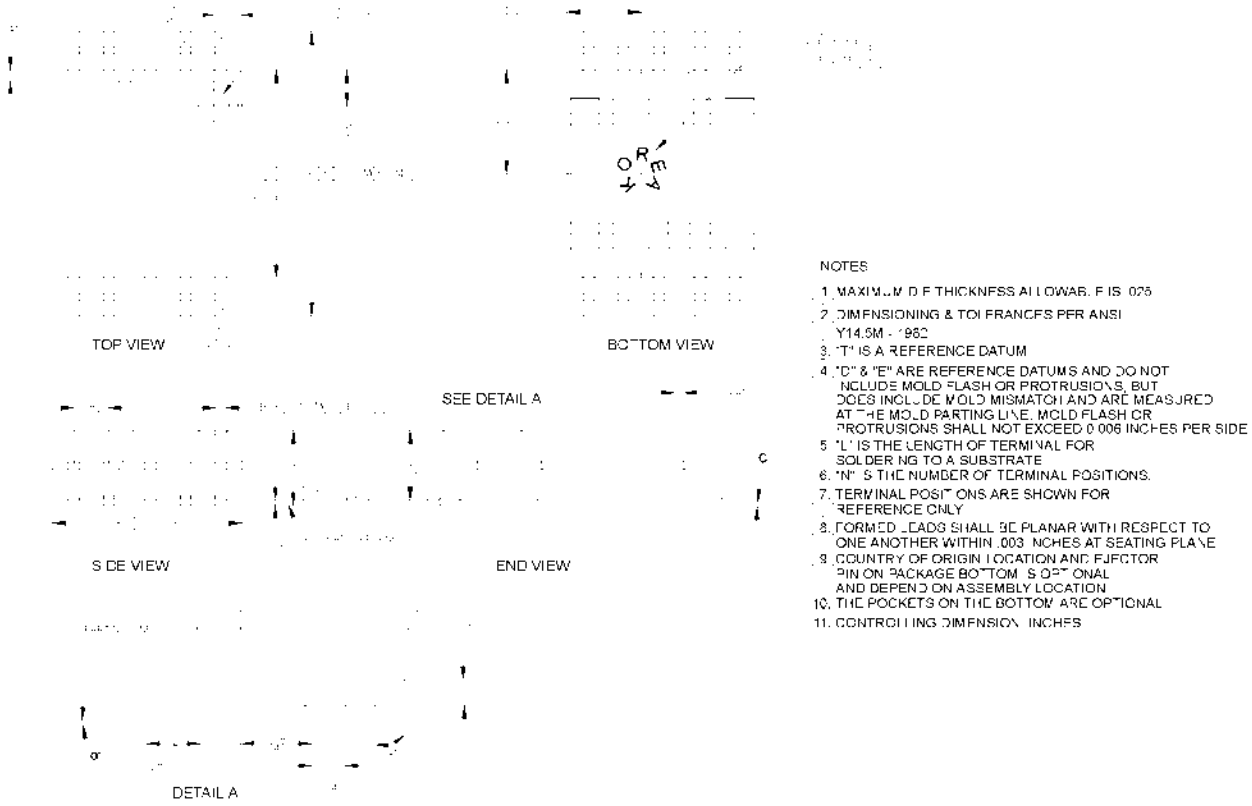
Ordering Information

Ordering Code	Package Name	Package Type
W217	G	24-pin SOIC

Document #38-00828-*A

Package Diagram

24-Pin Small Outline Integrated Circuit Package (SOIC)



NOTES

1. MAXIMUM D F THICKNESS AI LOWAB. F IS .025
2. DIMENSIONING & TOI FRANCES PER ANSI Y14.5M - 1982
3. "T" IS A REFERENCE DATUM
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT NCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDER NG TO A SUBSTRATE
6. "N" S THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSIT ONS ARE SHOWN FOR REFERENCE ONLY
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 NCHES AT SEATING PLANE
9. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM S OPT ONAL AND DEPEND ON ASSEMBLY LOCATION
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL
11. CONTROLLING DIMENSION INCHES

THIS TABLE IN INCHES

	COMMON DIMENSIONS				NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN	NOM	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A1	.0050	.009	.0115		AB	.451	.456	.461	18
A2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

	COMMON DIMENSIONS				NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
	0°	5°	8°						
X	2.16	2.36	2.54						