W223

SDRAM Buffer -2 DIMM

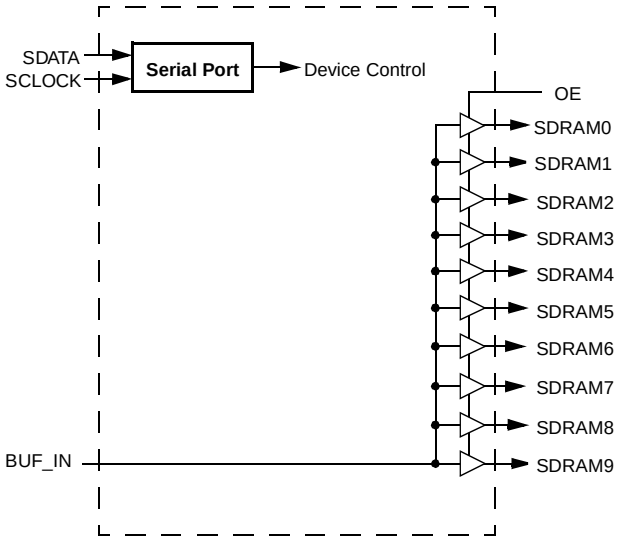
Features

- **Ten skew-controlled CMOS outputs (SDRAM0:9)**
- **Supports two SDRAM DIMMs**
- **Ideal for high performance systems designed around Intel's latest Mobile chip set**
- **I^2C Serial configuration interface**
- **Skew between any two outputs is less than 250 ps**
- **1 to 5ns propagation delay**
- **DC to 133 MHz operation**
- **Single 3.3V supply voltage**
- **Low power CMOS design packaged in a 28-pin, 0.209-inch SSOP (Shrink Small Outline Package)**

Key Specification

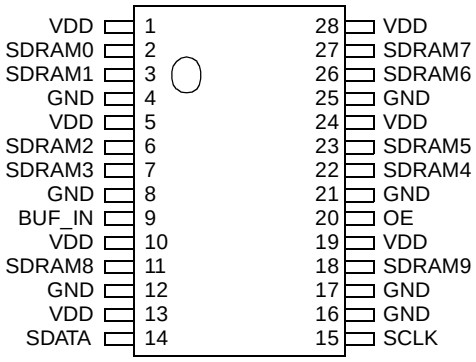
Supply Voltages: ..... V_{DD} = 3.3V±5%
Operating Temperature: ..... 0°C to +70°C
Input Threshold: ..... 1.5V typical
Maximum Input Voltage: ..... V_{DD} + 0.5V
Input Frequency: ..... 0 to 133 MHz
BUF_IN to SDRAM0:9 Propagation Delay: ..... 1.0 to 5.0 ns
Output Edge Rate: ..... ≥1.5 V/ns
Output Skew: ..... ±250 ps
Output Duty Cycle: ..... 45/55% worst case
Output Impedance: ..... 15Ω typical
Output Type: ..... CMOS rail-to-rail

Simplified Block Diagram



Pin Configuration [1]

SSOP



Note:

1. Internal pull-up resistor of 250K on SDATA, SCLK and OE inputs (should not be relied upon for pulling up to V_{DD}).

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Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
SDRAM0:9	2, 3, 6, 7, 22, 23, 26, 27, 11, 18	O	***SDRAM Outputs:*** Provides buffered copy of BUF_IN. The propagation delay from a rising input edge to a rising output edge is 1 to 5 ns. All outputs are skew controlled to within ± 250 ps of each other.
BUF_IN	9	I	***Clock Input:*** This clock input has an input threshold voltage of 1.5V (typ).
SDATA	14	I/O	***I^2C Data Input:*** Data should be presented to this input as described in the I^2C section of this data sheet. Internal 250-kΩ pull-up resistor.
SCLOCK	15	I	***I^2C Clock Input:*** The I^2C Data clock should be presented to this input as described in the I^2C section of this data sheet. Internal 250-kΩ pull-up resistor.
V_{DD}	1, 5, 10, 13, 19, 24, 28	P	***Power Connection:*** Power supply for core logic and output buffers, connected to 3.3V supply.
GND	4, 8, 12,16, 17, 21, 25	G	***Ground Connection:*** Connect all ground pins to the common system ground plane.

Overview

The Cypress W223 is a low-voltage, ten-output clock buffer. Output buffer impedance is approximately 15Ω which is ideal for driving SDRAM DIMMs.

Functional Description

Output Control Pins

Outputs three-stated when OE = 0, and toggle when OE = 1. Outputs are in phase with BUF_IN but are phase delayed by 3 to 7 ns. Outputs can also be controlled via the I^2C interface.

Output Drivers

The W223 output buffers are CMOS type which deliver a rail-to-rail (GND to V_{DD}) output voltage swing into a nominal capacitive load. Thus, output signaling is both TTL and CMOS level compatible. Nominal output buffer impedance is 15Ω.

Operation

Data is written to the W223 in eleven bytes of eight bits each. Bytes are written in the order shown in *Table 1*.

Table 1. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W223 to accept the bits in Data Bytes 0–7 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W223 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	“Don’t Care”	Unused by the W223, therefore bit values are ignored (“Don’t Care”). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	“Don’t Care”	Unused by the W223, therefore bit values are ignored (“Don’t Care”). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	“Don’t Care”	Refer to Cypress clock drivers.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5	Refer to *Table 2*	The data bits in these bytes set internal W223 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 2*, Data Byte Serial Configuration Map.
10	Data Byte 6		
11	Data Byte 7		

Writing Data Bytes

Each bit in the data bytes control a particular device function. Bits are written MSB (most significant bit) first, which is bit 7.

Table 2 gives the bit formats for registers located in Data Bytes 5-7.

Table 2. Data Bytes 5–7 Serial Configuration Map[2]

Bit(s)	Affected Pin		Control Function	Bit Control	
	Pin No.	Pin Name		0	1
Data Byte 5 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	N/A	Reserved	(Reserved)	--	--
6	N/A	Reserved	(Reserved)	--	--
5	N/A	Reserved	(Reserved)	--	--
4	N/A	Reserved	(Reserved)	--	--
3	7	SDRAM3	Clock Output Disable	Low	Active
2	6	SDRAM2	Clock Output Disable	Low	Active
1	3	SDRAM1	Clock Output Disable	Low	Active
0	2	SDRAM0	Clock Output Disable	Low	Active
Data Byte 6 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	27	SDRAM7	Clock Output Disable	Low	Active
6	26	SDRAM6	Clock Output Disable	Low	Active
5	23	SDRAM5	Clock Output Disable	Low	Active
4	22	SDRAM4	Clock Output Disable	Low	Active
3	N/A	Reserved	(Reserved)	--	--
2	N/A	Reserved	(Reserved)	--	--
1	N/A	Reserved	(Reserved)	--	--
0	N/A	Reserved	(Reserved)	--	--
Data Byte 7 SDRAM Active/Inactive Register (1 = Enable, 0 = Disable)					
7	18	SDRAM9	Clock Output Disable	Low	Active
6	11	SDRAM8	Clock Output Disable	Low	Active
5	N/A	Reserved	(Reserved)	--	--
4	N/A	Reserved	(Reserved)	--	--
3	N/A	Reserved	(Reserved)	--	--
2	N/A	Reserved	(Reserved)	--	--
1	N/A	Reserved	(Reserved)	--	--
0	N/A	Reserved	(Reserved)	--	--

Note:

2. At power up all SDRAM outputs are enabled and active. It is recommended to program Bits 4–7 of Byte 5 and Bits 0–3 of Byte 6 to a “0” to save power and reduce noise.

How To Use the Serial Data Interface

Electrical Requirements

illustrates electrical characteristics for the serial interface bus used with the W223. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistor on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W223 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

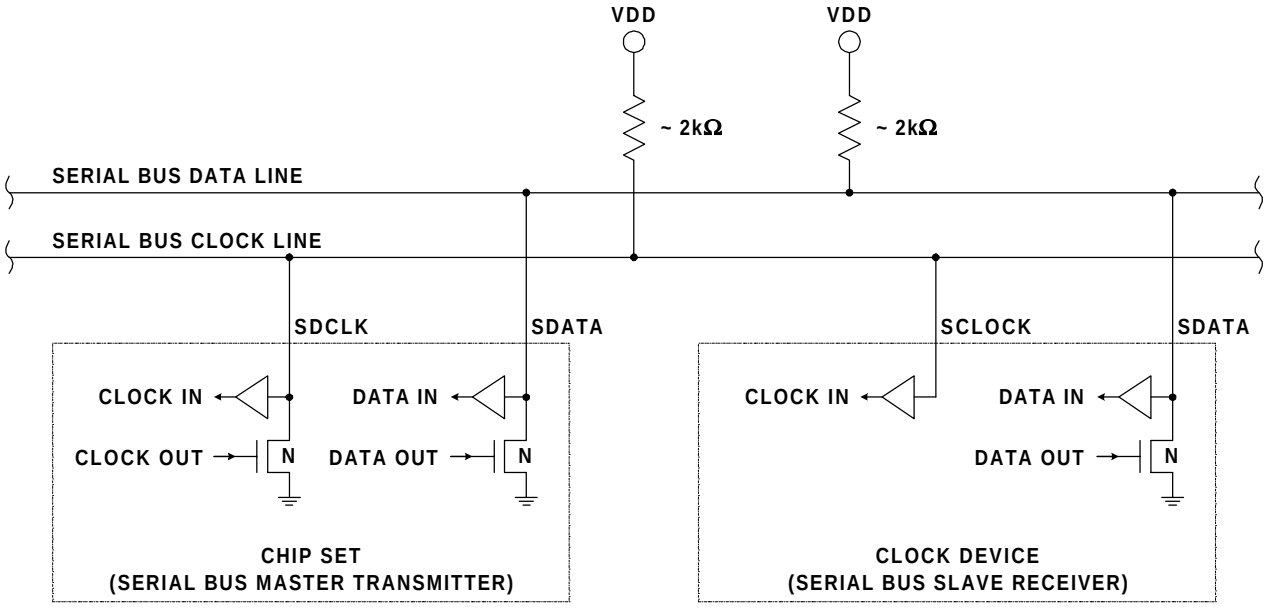


Figure 1. Serial Interface Bus Electrical Characteristics

Signaling Requirements

As shown in *Figure 2*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 3*. A “stop bit” signifies that a transmission has ended.

As stated previously, the W223 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 4*.

Sending Data to the W223

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).

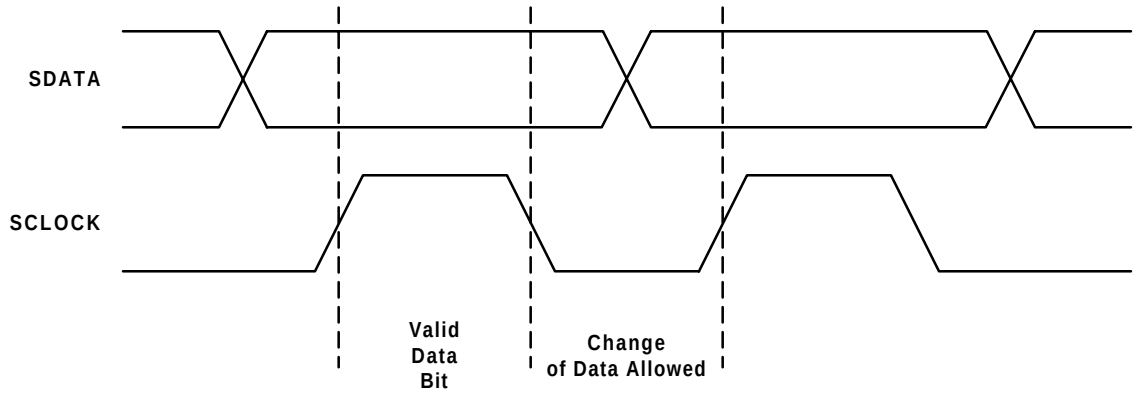


Figure 2. Serial Data Bus Valid Data Bit

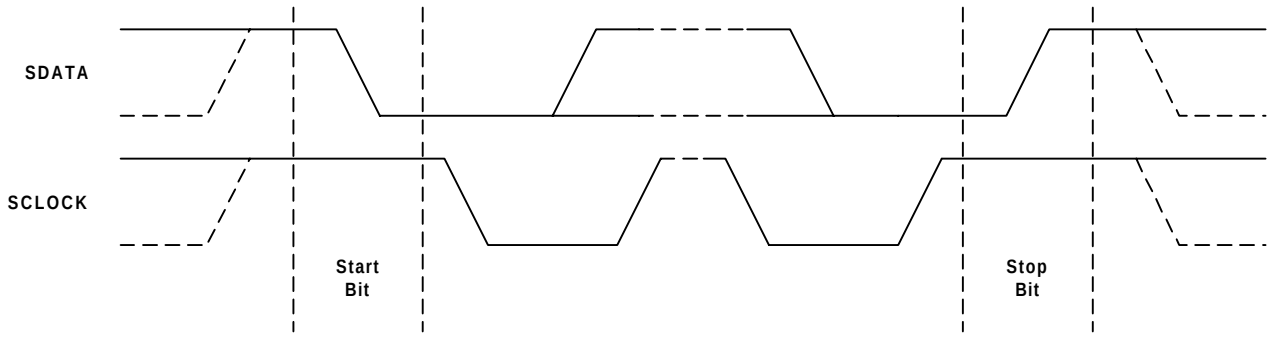


Figure 3. Serial Data Bus Start and Stop Bit

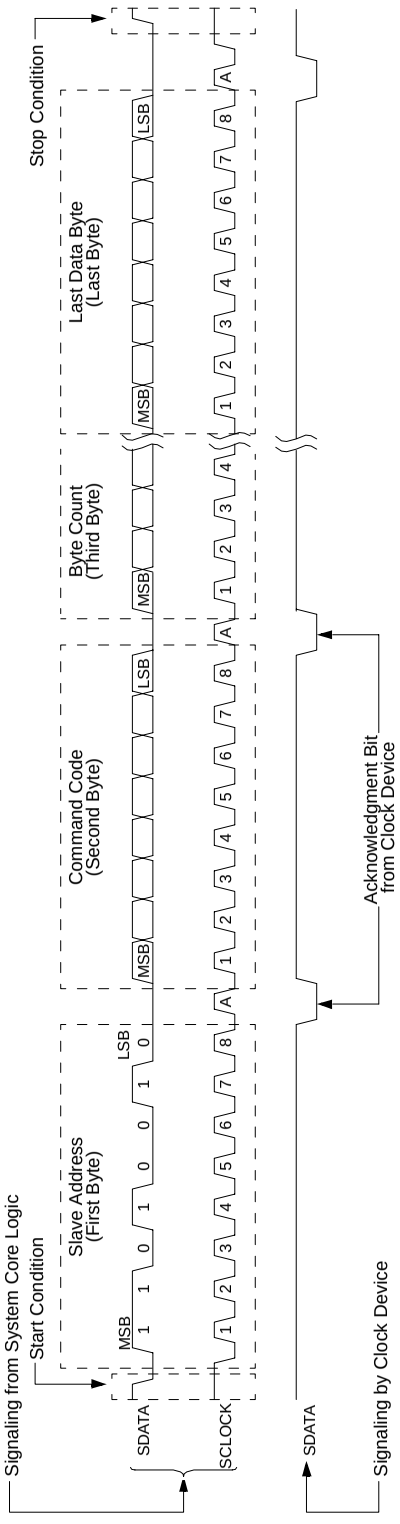


Figure 4. Serial Data Bus Write Sequence

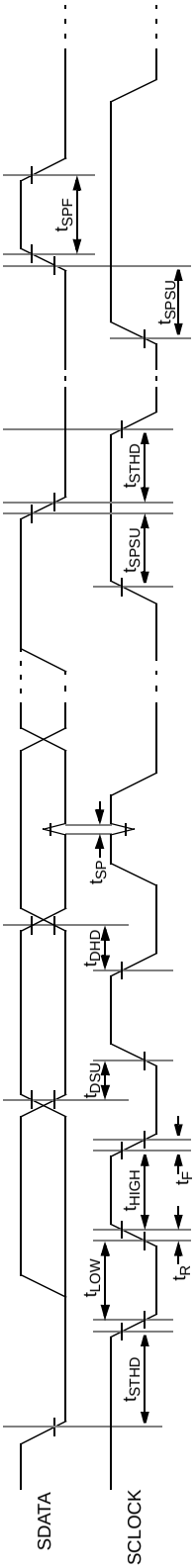


Figure 5. Serial Data Bus Timing Diagram

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V±5%

Parameter	Description	Test Condition/ Notes	Min.	Typ.	Max.	Unit
I_{DD}	3.3V Supply Current[4]	at 66 MHz[3]		120	160	mA
I_{DD}	3.3V Supply Current[4]	at 100 MHz[3]		185	220	mA
$I_{DD\ Tristate}$	3.3V Supply Current in Three-State			5	10	mA
Logic Inputs						
V_{IL}	Input Low Voltage		V_{SS} – 0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}+0.5	V
I_{ILEAK}	Input Leakage Current, BUF_IN		–5		+5	µA
I_{ILEAK}	Input Leakage Current		–20		+5	µA
Logic Outputs (SDRAM0:9)						
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	V_{OL} = 1.5V	70	110	185	mA
I_{OH}	Output High Current	V_{OH} = 1.5V	65	100	160	mA
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance (Except BUF_IN)				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Notes:

3. OE, SDATA, and SCLOCK logic pins have a 250-kΩ internal pull-up resistor (V_{DD} – 0.8V).
4. All SDRAM outputs loaded by 6" transmission lines with 22-pF capacitors on ends.

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V±5% (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency		0		133	MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
t_{SR}	Output Skew, Rising Edges				250	ps
t_{SF}	Output Skew, Falling Edges				250	ps
t_{EN}	Output Enable Time		1.0		8.0	ns
t_{DIS}	Output Disable Time		1.0		8.0	ns
t_{PR}	Rising Edge Propagation Delay		TBD		TBD	ns
t_{PF}	Falling Edge Propagation Delay		TBD		TBD	ns
t_D	Duty Cycle	Measured at 1.5V	45		55	%
Z_o	AC Output Impedance			15		Ω

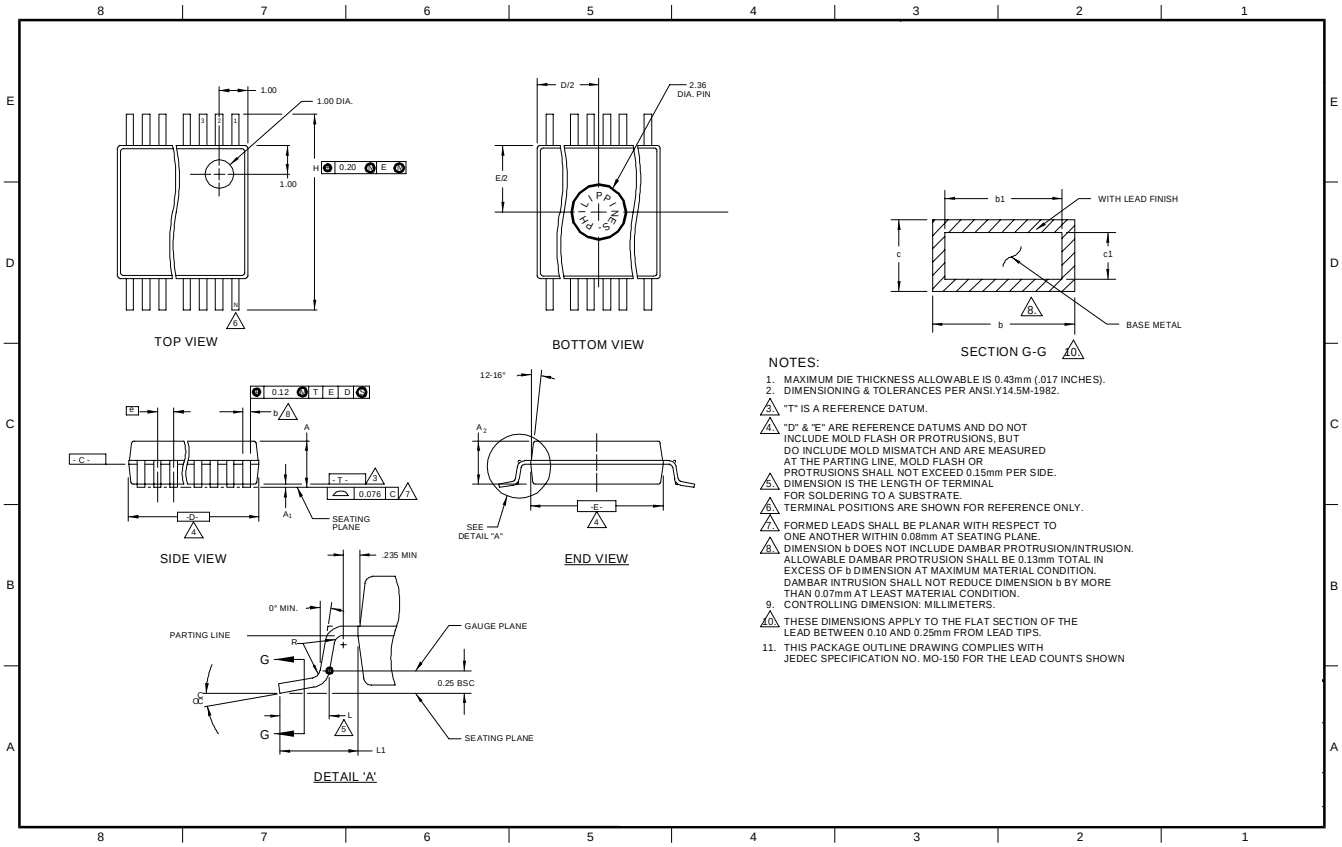
Ordering Information

Ordering Code	Package Name	Package Type
W223	H	28-Pin Plastic SSOP (209-mil)

Document #: 38-01007-**

Package Diagram

28-Pin Shrink Small Outline Package (SSOP, 209-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4 VARIATIONS	D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A_1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A_2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
α	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4 VARIATIONS	D			6 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.068	.073	.078		AA	.239	.244	.249	14
A_1	.002	.005	.008		AB	.239	.244	.249	16
A_2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
α	0°	4°	8°						
R	.004	.006							

TITLE: PACKAGE OUTLINE, 5.30mm (.209") BODY, SSOP

SIZE A1 | DWG. NO. 32289 | REV. 05

SCALE 8/1 | SHEET 2 of 2