Spread Spectrum FTG for SiS730S Chipset

Features

- **Maximized EMI Suppression using Cypress's Spread Spectrum technology**
- **Single-chip system frequency synthesizer for SiS730S core logic chip sets**
- **One pair of differential outputs for CPU**
- **Six copies of PCI output**
- **One 48-MHz output for USB**
- **One 24-/48-MHz selectable output for SIO**
- **Two buffered reference outputs**
- **13 SDRAM outputs provide support for 3 DIMMs I²C™ interface for programming**

Key Specifications

CPU Cycle-to-Cycle Jitter: ..... 250 ps

PCI Output Skew: ..... 500 ps

CPU to PCI Output Skew (CPU leads): ..... 1 to 4 ns

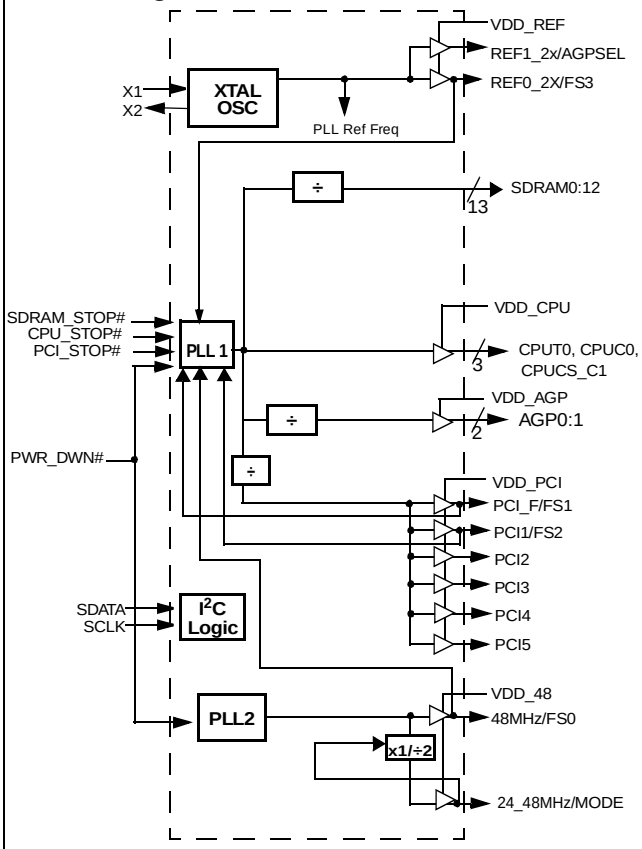
CPU to SDRAM Output Skew: ..... 500 ps

VDD_CPU, VDD_SDRAM, VDD_PCI, VDD_48, VDD_REF: .....3.3V±5%

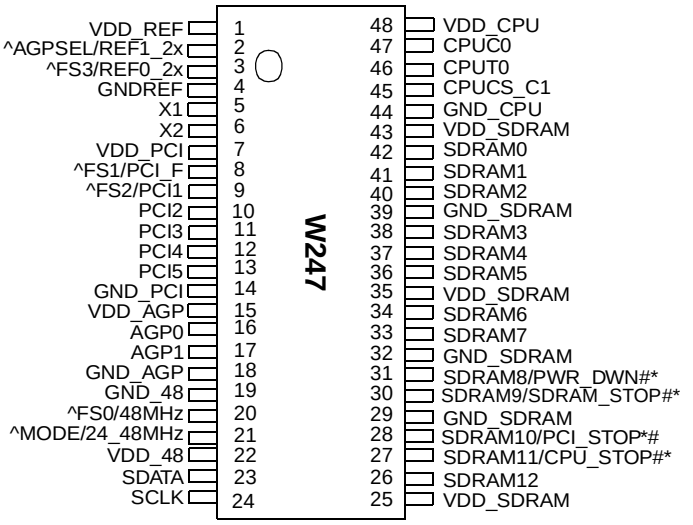
Table 1. Pin Selectable Frequency

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGP (MHz)		SS
							0	1	
0	0	0	0	100.0	100.0	33.3	66.6	57.1	–0.6%
0	0	0	1	100.0	133.3	33.3	66.6	57.1	–0.6%
0	0	1	0	105.0	140.0	30.0	60.0	52.5	OFF
0	0	1	1	100.0	66.6	33.3	66.6	57.1	–0.6%
0	1	0	0	112.0	112.0	33.6	67.2	56.0	OFF
0	1	0	1	110.0	110.0	33.0	66.0	55.0	OFF
0	1	1	0	124.0	124.0	31.0	62.0	53.1	OFF
0	1	1	1	133.3	100.0	33.3	66.6	57.1	–0.6%
1	0	0	0	133.3	133.3	33.3	66.6	57.1	–0.6%
1	0	0	1	103.0	137.3	34.3	68.6	58.9	OFF
1	0	1	0	108.8	145.0	31.1	62.2	54.4	OFF
1	0	1	1	143.0	107.3	30.6	61.2	53.6	OFF
1	1	0	0	143.0	143.0	30.6	61.2	53.6	OFF
1	1	0	1	90.0	90.0	30.0	60.0	51.4	OFF
1	1	1	0	103.0	103.0	34.3	68.6	58.9	OFF
1	1	1	1	105.0	105.0	30.0	60.0	52.5	OFF

Block Diagram



Pin Configuration [1]



Note:

1. Internal 100-kΩ pull-up and pull-down resistors present on inputs marked with * and ^ respectively. Design should not rely solely on internal pull-up or pull-down resistors to set I/O pins HIGH or LOW.

I²C is a trademark of Philips Corporation.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPUT0, CPUC0, CPUCS_C1	46, 47, 45	O (open-drain)	***CPU Clock Outputs:*** CPUT0 and CPUC0 are the differential CPU clock outputs for K7 processor. CPUCS_C1 is the open-drain clock output for the chipset. It has the same phase relationship as CPUT0.
PCI_F/FS1	8	I/O	***PCI Clock Output /Frequency Selection 1:*** Free-running PCI clock outputs. Output voltage swing is controlled by voltage applied to VDD_PCI. Shortly after initial power-up the pin is sampled as an input to determine CPU, SDRAM, and PCI operating frequencies.
PCI1/FS2	9	I/O	***PCI Clock Output /Frequency Selection 2:*** PCI clock output. Output voltage swing is controlled by voltage applied to VDD_PCI. Shortly after initial power-up the pin is sampled as an input to determine CPU, SDRAM, and PCI operating frequencies.
PCI2:5	10, 11, 12, 13	O	***PCI Clock Outputs 2 through 5:*** PCI clock outputs. Output voltage swing is controlled by voltage applied to VDD_PCI.
48MHz/FS0	20	I/O	***48-MHz Output/Frequency Select 0:*** 48 MHz is provided in normal operation. In standard PC systems, this output can be used as the reference for the Universal Serial Bus host controller. This pin also serves as a power on strap option to determine device operating frequency as described in *Table 1*
24_48MHz/MODE	21	I/O	***24_48-MHz Output/MODE:*** In standard PC systems, this output can be used as the clock input for a Super I/O chip. The output frequency is controlled by Configuration Byte 1 bit[1]. The default output frequency is 48 MHz. This pin also serves as a power on strap option to determine the operation mode of pin 27, 28, 30, and 31.
AGPSEL/ REF1_2x	2	I/O	***Reference Clock Output 1/AGPSEL:*** 3.3V 14.318-MHz output clock. This pin also serves as a power on strap option to determine device operating frequency as described in Table 3.Upon power-up, AGPSEL input will be latched which will set the AGP clock frequencies as described in *Table 1*.
FS3/REF0_2X	3	I/O	***Reference Clock Output 1/Frequency Select 3:*** 3.3V 14.318-MHz output clock. This pin also serves as a power on strap option to determine device operating frequency as described in *Table 3*.Upon power-up, FS0 input will be latched which will set clock frequencies as described in *Table 1*.
AGP0:1	16, 17	O	***Synchronous APIC Clock Outputs:*** Clock outputs running synchronous with the PCI clock outputs (33 MHz). Voltage swing set by VDD_AGP.
SDRAM0:7 SDRAM12	42, 41, 40, 38, 37, 36, 34, 33, 26	O	**SDRAM Clock Outputs:** These dedicated outputs provide the SDRAM clocks for memory DIMM. The swing is set by VDD_SDRAM.
SDRAM8/ PWR_DWN#	31	I/O	**SDRAM Clock Output /Power Down:** If the MODE pin is strapped LOW, this pin serves as SDRAM output. If MODE pin is strapped HIGH, this pin serves as PWR_DWN input.
SDRAM9/ SDRAM_STOP#	30	I/O	**SDRAM Clock Output/SDRAM_STOP:** If the MODE pin is strapped LOW, this pin serves as SDRAM output. If MODE pin is strapped HIGH, this pin serves as SDRAM_STOP input.
SDRAM10/ PCI_STOP#	28	I/O	**SDRAM Clock Output /PCI _STOP:** If the MODE pin is strapped LOW, this pin serves as SDRAM output. If MODE pin is strapped HIGH, this pin serves as PCI_STOP input.
SDRAM11/ CPU_STOP#	27	I/O	**SDRAM Clock Output/CPU_STOP:** If the MODE pin is strapped LOW, this pin serves as SDRAM output. If MODE pin is strapped HIGH, this pin serves as CPU_STOP input.
SCLK	24	I	Clock pin for I^2C circuitry.
SDATA	23	I/O	Data pin for I^2C circuitry.

Pin Definitions (continued)

Pin Name	Pin No.	Pin Type	Pin Description
X1	5	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	6	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDD_REF, VDD_PCI, VDD_AGP, VDD_48, VDD_SDRAM, VDD_CPU	1,7, 16, 22, 25, 35, 43, 48	P	***Power Connection:*** Power supply for core logic, PLL circuitry, CPU, SDRAM outputs, PCI outputs, reference outputs and 48-MHz output. Connect to 3.3V supply.
GND_REF, GND_PCI, GND_AGP, GND_48 GND_SDRAM, GND_CPU	4, 14, 18, 19, 29, 32, 39, 44	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Serial Data Interface

The device features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W247 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLK. In motherboard applications, SDATA and SCLK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

Operation

Data is written to the device in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the options that are provided by the frequency selection pin power-on default selection. Frequency is changed in a smooth and controlled fashion.	For alternate CPU devices, and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Three-state	Puts all clock outputs into a high-impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation with X1 input, internal PLL is bypassed. Refer to *Table 4*.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the device to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the device is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	“Don’t Care”	Unused by the device, therefore bit values are ignored (“Don’t Care”). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	“Don’t Care”	Unused by the device, therefore bit values are ignored (“Don’t Care”). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 4*	The data bits in these bytes set internal W247 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes controls a particular device function except for the “reserved” bits, which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 4* gives the bit formats for registers located in Data Bytes 0–6. *Table 5* details additional frequency selections that are available through the serial data interface.

Table 4. Data Bytes 0–6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	BYTE0_SEL3	Refer to *Table 5*		0
6	--	--	BYTE0 _SEL2	Refer to *Table 5*		0
5	--	--	BYTE0 _SEL1	Refer to *Table 5*		0
4	--	--	BYTE0 _SEL0	Refer to *Table 5*		0
3	--	--	FS0:3 override	Select operating frequency by FS 3:0	Select operating frequency by BYTE0_SEL (4:0)	0
2	--	--	BYTE0_SEL4	Refer to *Table 5*		0
1	--	--	(Reserved)	--	--	1
0	--	--	Test Mode	Normal	Three-state all outputs	0
Data Byte 1						
7	--	--	SI0_SEL	48 MHz	24 MHz	1
6	45	--	CPUCS_C1 Control	Free-running	Disabled by CPU_STP#	1
5	--	--	(Reserved)	--	--	1
4	--	--	(Reserved)	--	--	1
3	45	CPUCS_C1	Clock Output Disable	Low	Active	1
2	--	--	(Reserved)	--	--	1
1	46, 47	CPUT0, CPUC0	Clock Output Disable	Low	Active	1
0	--	--	(Reserved)	--	--	1
Data Byte 2						
7	--	--	(Reserved)	--	--	1
6	--	--	(Reserved)	--	--	1
5	13	PCI5	Clock Output Disable	Low	Active	1
4	12	PCI4	Clock Output Disable	Low	Active	1
3	11	PCI3	Clock Output Disable	Low	Active	1
2	10	PCI2	Clock Output Disable	Low	Active	1
1	9	PCI1	Clock Output Disable	Low	Active	1
0	8	PCI_F	Clock Output Disable	Low	Active	1
Data Byte 3						
7	33	SDRAM7	Clock Output Disable	Low	Active	1
6	34	SDRAM6	Clock Output Disable	Low	Active	1
5	36	SDRAM5	Clock Output Disable	Low	Active	1
4	37	SDRAM4	Clock Output Disable	Low	Active	1
3	38	SDRAM3	Clock Output Disable	Low	Active	1
2	40	SDRAM2	Clock Output Disable	Low	Active	1
1	41	SDRAM1	Clock Output Disable	Low	Active	1

Table 4. Data Bytes 0–6 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
0	42	SDRAM0	Clock Output Disable	Low	Active	1
Data Byte 4						
7	21	24_48MHz	Clock Output Disable	Low	Active	1
6	20	48MHz	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	1
4	26	SDRAM12	Clock Output Disable	Low	Active	1
3	27	SDRAM11	Clock Output Disable	Low	Active	1
2	28	SDRAM10	Clock Output Disable	Low	Active	1
1	30	SDRAM9	Clock Output Disable	Low	Active	1
0	31	SDRAM8	Clock Output Disable	Low	Active	1
Data Byte 5						
7	17	AGP1	Clock Output Disable	Low	Active	1
6	16	AGP0	Clock Output Disable	Low	Active	1
5	--	--	(Reserved)	--	--	1
4	--	--	(Reserved)	--	--	1
3	--	--	(Reserved)	--	--	1
2	--	--	(Reserved)	--	--	1
1	2	REF1	Clock Output Disable	Low	Active	1
0	3	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions					Output Frequency					
Data Byte 0 Bit 3 = 1								AGP		
Bit 2 SEL_4	Bit 7 SEL_3	Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU	SDRAM	PCI	AGPSEL=0	AGPSEL=1	Spread Spectrum
0	0	0	0	0	100.0	100.0	33.3	66.6	57.1	–0.6%
0	0	0	0	1	100.0	133.3	33.3	66.6	57.1	–0.6%
0	0	0	1	0	105.0	140.0	30.0	60.0	52.5	OFF
0	0	0	1	1	100.0	66.6	33.3	66.6	57.1	–0.6%
0	0	1	0	0	112.0	112.0	33.6	67.2	56.0	OFF
0	0	1	0	1	110.0	110.0	33.0	66.0	55.0	OFF
0	0	1	1	0	124.0	124.0	31.0	62.0	53.1	OFF
0	1	0	0	1	133.3	100.0	33.3	66.6	57.1	–0.6%
0	1	0	0	0	133.3	133.3	33.3	66.6	57.1	–0.6%
0	1	0	1	1	103.0	137.3	34.3	68.6	58.9	OFF
0	1	0	1	0	108.8	145.0	31.1	62.2	54.4	OFF
0	1	1	0	1	143.0	107.3	30.6	61.2	53.6	OFF
0	1	1	0	0	143.0	143.0	30.6	61.2	53.6	OFF
0	1	1	1	1	90.0	90.0	30.0	60.0	51.4	OFF
0	1	1	1	0	103.0	103.0	34.3	68.6	58.9	OFF
0	0	1	1	1	105.0	105.0	30.0	60.0	52.5	OFF
1	0	0	0	0	100.2	100.2	33.4	66.8	57.1	±0.5%
1	0	0	0	1	100.2	133.6	33.4	66.8	57.1	±0.5%
1	0	0	1	0	107.0	107.0	30.6	61.2	53.5	OFF
1	0	0	1	1	100.2	66.8	33.4	66.8	57.1	±0.5%
1	0	1	0	0	120.0	120.0	30.0	60.0	51.4	OFF
1	0	1	0	1	129.0	129.0	32.3	64.6	55.3	OFF
1	0	1	1	0	137.0	102.8	34.3	68.6	58.7	OFF
1	0	1	1	1	133.6	100.2	33.4	66.8	57.1	±0.5%
1	1	0	0	0	133.6	133.6	33.4	66.8	57.1	±0.5%
1	1	0	0	1	122.0	122.0	30.5	61.0	52.3	OFF
1	1	0	1	0	117.0	117.0	33.4	66.8	58.5	OFF
1	1	0	1	1	140.0	140.0	30.0	60.0	52.5	OFF
1	1	1	0	0	112.5	150.0	32.1	64.2	56.3	OFF
1	1	1	0	1	115.0	115.0	34.5	69.0	57.5	OFF
1	1	1	1	0	137.0	137.0	34.25	68.6	58.7	OFF
1	1	1	1	1	140.0	105.0	30.0	60.0	52.5	OFF

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

3.3V DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = 3.3V±5% (3.135–3.465V)

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD}	Combined 3.3V Supply Current				350		mA
Logic Inputs (All referenced to V_{DD} = 3.3V)							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current[3]					10	µA
I_{IH}	Input High Current[3]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
I_{OL}	Output Low Current	SDRAM0:12	V_{OL} = 1.5V	80	110	155	mA
		PCI1:5, PCI_F		55	75	105	
		REF0,1		60	75	90	
		48/24 MHZ		55	75	105	
I_{OH}	Output High Current	SDRAM0:12	V_{OH} = 1.5V	80	120	175	mA
		PCI1:5, PCI_F		55	85	125	
		REF0,1		60	75	90	
		48/24 MHz		55	85	125	
Crystal Oscillator							
V_{TH}	X1 Input Threshold Voltage[4]				1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[5]				18		pF
$C_{IN,X1}$	X1 Input Capacitance[6]		Pin X2 unconnected		28		pF

Notes:

2. All clock outputs loaded with 6" 60Ω transmission lines with 22-pF capacitors.
3. W247 logic inputs have internal pull-up devices (pull-ups not full CMOS level).
4. X1 input threshold voltage (typical) is $V_{DDQ3}/2$.
5. The W247 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
6. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

3.3V DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = 3.3V±5% (3.135–3.465V) (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH
Serial Input Port						
V_{IL}	Input Low Voltage				$0.3V_{DD}$	V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V
I_{IL}	Input Low Current	No internal pull-up/ down on SCLK.			10	µA
I_{IH}	Input High Current	No internal pull-up/ down on SCLK.			10	µA
I_{OL}	Sink Current into SDATA or SCLK, Open Drain N-Channel Device On	$I_{OL} = 0.3V_{DD}$	6			mA
C_{IN}	Input Capacitance of SDATA and SCLK				10	pF
C_{SDATA}	Total Capacitance of SDATA Bus				400	pF
C_{SCLOCK}	Total Capacitance of SCLK Bus				400	pF

3.3V AC Electrical Characteristics (CPU3.3#_2.5 Input = 0)

T_A = 0°C to +70°C, V_{DDQ3} = V_{DDQ2} = 3.3V±5% (3.135–3.465V), f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

CPU Clock Outputs, (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/ Comments	CPU = 100 MHz			CPU = 133 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	10.0			7.5			ns
f	Frequency, Actual	Determined by PLL divider ratio	TBD			TBD			MHz
t_H	High Time	Duration of clock cycle above 2.4V	3.0			1.87			ns
t_L	Low Time	Duration of clock cycle below 0.4V	2.8			1.67			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	15	20	30	15	20	30	Ω

SDRAM Clock Outputs, (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/ Comments	SDRAM = 100 MHz			SDRAM = 133 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V.	10.0			7.5			ns
f	Frequency, Actual	Determined by PLL divider ratio.		TBD			TBD		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V.	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V.	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V.	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V.		175			175		ps
t_{SK}	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.			500			500	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	10	15	20	10	15	20	Ω

PCI Clock Outputs, PCI0:6 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	PCI = 33.3 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V.	30			ns
f	Frequency, Actual	Determined by PLL divider ratio.		33.3		MHz
t_H	High Time	Duration of clock cycle above 2.4V.	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V.	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V.	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V.	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V.	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V.			500	ps
t_O	CPU to PCI Clock Skew	Covers all 3V66/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1	2	4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	15	20	30	Ω

REF0_2X, REF1_2X Clock Output (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator.		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V.	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V.	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V.	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	17	20	25	Ω

SIO Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008/24.004		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17, 57/34		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	40		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	15	20	30	Ω

Serial Input Port

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f_{SCLOCK}	SCLOCK Frequency	Normal Mode.	0		100	kHz
t_{STHD}	Start Hold Time		4.0			µs
t_{LOW}	SCLOCK Low Time		4.7			µs
t_{HIGH}	SCLOCK High Time		4.0			µs
t_{DSU}	Data Set-up Time		250			ns
t_{DHD}	Data Hold Time	(Transmitter should provide a 300-ns hold time to ensure proper timing at the receiver.)	0			ns
t_R	Rise Time, SDATA and SCLOCK	From $0.3V_{DD}$ to $0.7V_{DD}$			1000	ns
t_F	Fall Time, SDATA and SCLOCK	From $0.7V_{DD}$ to $0.3V_{DD}$			300	ns
t_{STSU}	Stop Set-up Time		4.0			µs
t_{SPF}	Bus Free Time between Stop and Start Condition		4.7			µs
t_{SP}	Allowable Noise Spike Pulse Width				50	ns

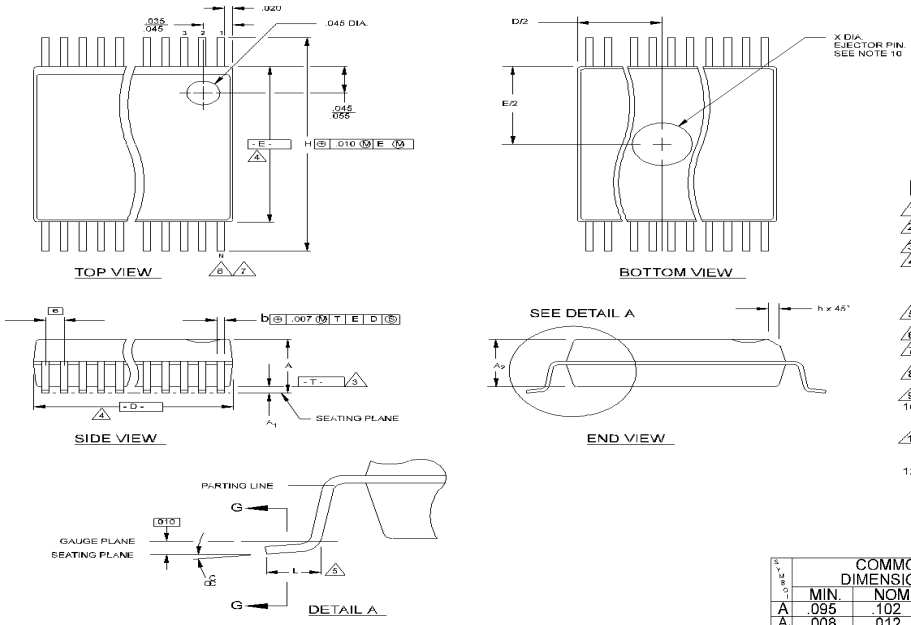
Ordering Information

Ordering Code	Package Name	Package Type
W247	H	48-pin SSOP (300 mils)

Document #: 38-00928-**

Package Diagram

48-Pin Small Shrink Outline Package (SSOP, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS				NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS				NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

THIS TABLE IN MILLIMETERS