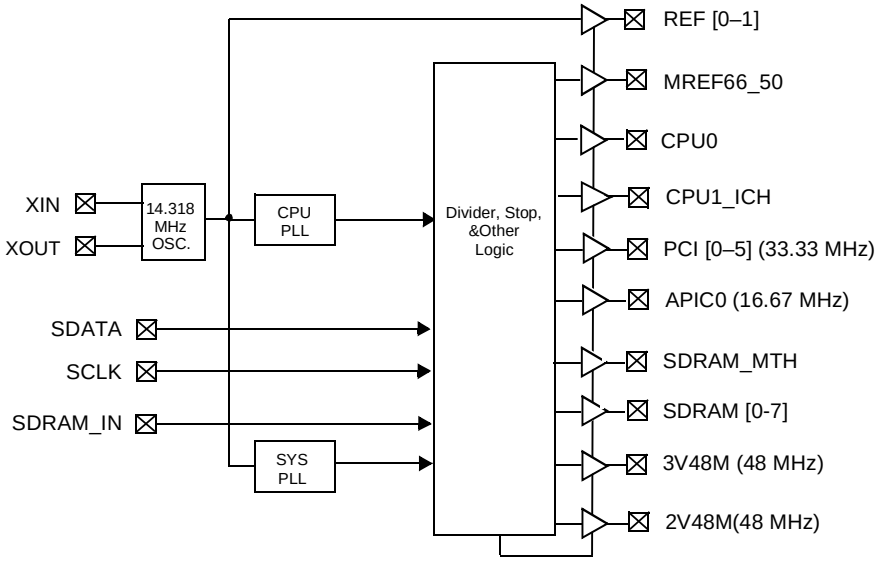
PRELIMINARY

W281

Spread Spectrum Frequency Timing Generator for Integrated CPU

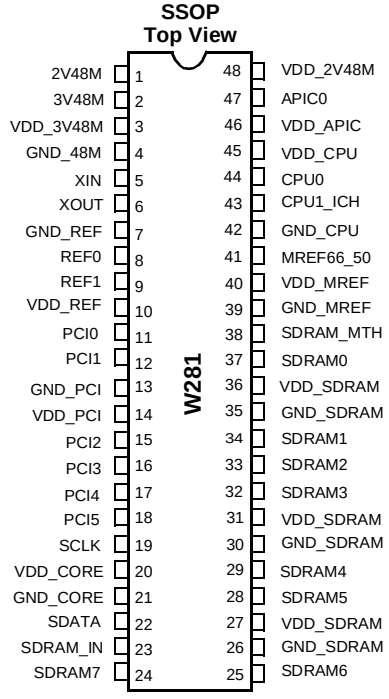
Features	Benefits
• **Mixed 2.5V and 3.3V operation** — **Integrated CY2219 (main Clock) and CY2310 (SDRAM buffer) into a single chip**	Supports Intel Timna processors with integrated graphics and memory controllers — Combined with W134S, W281 offers an optimized and cost reduced solution for Timna platform
• **Multiple output clocks at different frequencies** — **Two CPU clocks at 66 MHz** — **Six PCI clocks at 33 MHz, 1 free-running** — **One DRCG reference clock at 66 MHz or 50 MHz** — **One synchronous APIC clock at 16.67 MHz** — **One 3.3V and one 2.5V clock at 48 MHz** — **Two reference clocks at 14.318 MHz** — **Nine SDRAM output clocks**	Single-chip main motherboard clock generator — Support for CPU and chipset — Support for multiple PCI slots and chipset — Drives one main memory clock generator, including DRCG (W134S) — Supports USB frequencies and I/O chip
• **Non-linear Spread Spectrum implementation**	Maximize EMI reduction
• **Two Frequency Select inputs**	Supports up to four CPU clock frequencies
• **Low-skew and low-jitter outputs**	Meets tight system timing requirements at high frequency
• **OE and Test Mode support**	Enables ATE and “bed of nails” testing
• **48-pin SSOP package**	Widely available, standard package enables lower cost

Logic Block Diagram



Pin Configuration[1]

SSOP
Top View



Note:

1. Pins denoted by * have internal pull-up resistor. Designer should not solely rely on internal resistor to set I/O pins HIGH,

Pin Summary

Name	Pins	Description
CPU0, CPU1_ICH,	44, 43	2.5V 66-MHz Host bus clock outputs
MREF66_50	41	2.5V Memory Reference clock output. Output frequency is determined by I^2C control Byte [5]
PCI [0-5]	11, 12, 15, 16, 17, 18,	3.3V PCI clock outputs
APIC0	47	2.5V 33-MHz IOAPIC clock outputs
REF [0-1]	8, 9	3.3V Fixed (non SSC) 14.318-MHz clock output
XIN	5	14.318-MHz Crystal input
XOUT	6	14.318-MHz Crystal output
3V48M (USB)	2	3.3V Fixed (non-SSC) 48-MHz clock output
2V48M (DOT)	1	2.5V Fixed (non-SSC) 48-MHz clock output
SDRAM _IN	23	3.3V LVTTL-compatible SDRAM input for driving SDRAM output drivers
SDRAM [0-7] SDRAM_MTH	37, 34, 33, 32, 29, 28, 25, 24 38	3.3V output driver. All SDRAM outputs can be turned off through I^2C except SDRAM_MTH
SDATA	22	I^2C compatible SDATA
SCLK	19	I^2C compatible SCLOCK
VDD_CORE VDD_3V48M, VDD_REF, VDD_PCI, VDD_SDRAM, VDD_MREF,	20, 3, 10, 14, 27, 31, 36, 40	3.3V power supply
GND_CORE, GND_48M, GND_REF, GND_PCI, GND_SDRAM, GND_MREF. GND_CPU	21 4, 7, 13, 26, 30, 35, 39, 42	Ground
VDD_CPU, VDD_APIC, VDD_2V48M	45, 46, 48	2.5V power

Clock Driver Impedances

Buffer Name	V_{DD} Range	Buffer Type	Minimum (Ω)	Typical (Ω)	Maximum (Ω)
CPU MREF66_50, APIC, 2V48M	2.375–2.625	Type 1	13.5	28	45
REF, 3V48M	3.135–3.465	Type 3	20	25	60
PCI	3.135–3.465	Type 5	12	34	55
SDRAM	3.135–3.465	Type 4	10	25	24

W281 Serial Data Interface

1. The serial bits will be read by the clock driver in the following order:

   Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

   Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

2. All unused register bits (reserved and N/A) should be written to a “0” level.
3. All register bits labeled “Initialize to 0" must be written to zero during initialization. Failure to do so may result in higher than normal operating current.

Byte 0: Control Register (1 = Enable, 0 = Disable)[2]

Bit	Pin#	Name	Pin Description	Default
Bit 7	-	Reserved Drive to ‘0’	(Active/Inactive)	0
Bit 6	-	Reserved Drive to ‘0’	(Active/Inactive)	0
Bit 5	-	Reserved Drive to ‘0’	(Active/Inactive)	0
Bit 4	-	Reserved Drive to ‘0’	(Active/Inactive)	0
Bit 3	-	Reserved Drive to ‘0’	(Active/Inactive)	0
Bit 2	1	2v48M DOT	(Active/Inactive)	1
Bit 1	2	3V48M USB	(Active/Inactive)	1
Bit 0	--	Reserved Drive to ‘0’	(Active/Inactive)	0

Byte 1: Control Register (1 = Enable, 0 = Disable)[2]

Bit	Pin#	Name	Pin Description	Default
Bit 7	24	SDRAM7	(Active/Inactive)	1
Bit 6	25	SDRAM6	(Active/Inactive)	1
Bit 5	28	SDRAM5	(Active/Inactive)	1
Bit 4	29	SDRAM4	(Active/Inactive)	1
Bit 3	32	SDRAM3	(Active/Inactive)	1
Bit 2	33	SDRAM2	(Active/Inactive)	1
Bit 1	34	SDRAM1	(Active/Inactive)	1
Bit 0	37	SDRAM0	(Active/Inactive)	1

Byte 2: Control Register (1 = Enable, 0 = Disable)[2]

Bit	Pin#	Name	Pin Description	Default
Bit 7	--	Reserved Drive to ‘0’	(Active/Inactive)	1
Bit 6	--	Reserved Drive to ‘0’	(Active/Inactive)	1
Bit 5	18	PCI5	(Active/Inactive)	1
Bit 4	17	PCI4	(Active/Inactive)	1
Bit 3	16	PCI3	(Active/Inactive)	1
Bit 2	15	PCI2	(Active/Inactive)	1
Bit 1	12	PCI1	(Active/Inactive)	1
Bit 0	11	PCI0	Reserved	1

Note:

2. Inactive mean outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 3: Reserved Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description	Default
Bit 7	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 6	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 5	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 4	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 3	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 2	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 1		Reserved Drive to '0'	(Active/Inactive)	0
Bit 0	-	Reserved Drive to '0'	(Active/Inactive)	0

Byte 4: Reserved Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description	Default
Bit 7	-	SDRAM Buffer Delay [1]	Bit[7:6] Delay '00' - 5.5 to 7.5 ns '01' - 5.0 to 7.0 ns '10' - 6.0 to 8.0 ns '11' - 6.5 to 8.5 ns	0
Bit 6	-	SDRAM Buffer Delay [0]		0
Bit 5	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 4	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 3	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 2	-	Reserved Drive to '0'	(Active/Inactive)	0
Bit 1		Reserved Drive to '0'	(Active/Inactive)	0
Bit 0	-	Reserved Drive to '0'	(Active/Inactive)	0

Byte 5: I^2C SEL Frequency Table

Bit	Pin#	Name	0	1	Default
Bit 7	-	Test Mode	Normal	Three-State	0
Bit 6	-	MREF SEL	66 MHz	50 MHz	0
Bit 5	-	Frequency Select Override	HW	SW	0
Bit 4	-	SEL4	Refer to Frequency *Table 1*		0
Bit 3	-	SEL3	Refer to Frequency *Table 1*		0
Bit 2	-	SEL2	Refer to Frequency *Table 1*		0
Bit 1		SEL1	Refer to Frequency *Table 1*		0
Bit 0	-	SEL0	Refer to Frequency *Table 1*		0

Table 1. Frequency Table.

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPU	MREF		PCI	APIC	SS%
						0	1			
0	0	0	0	0	66.66	66.66	50	33.33	33.33	OFF
0	0	0	0	1	66.66	66.66	50	33.3	33.3	–0.5
0	0	0	1	0	66.8	66.8	50.1	33.4	33.4	±0.5
0	0	0	1	1	66.8	66.8	50.1	33.4	33.4	±0.25
0	0	1	0	0	66.8	66.8	50.1	33.4	33.4	OFF
0	0	1	0	1	67.33	67.33	50.5	33.67	33.67	OFF
0	0	1	1	0	68	68	51	34	34	OFF
0	0	1	1	1	69	69	51.75	34.5	34.5	OFF
0	1	0	0	0	70	70	52.5	35	35	OFF
0	1	0	0	1	71	71	53.25	35.5	35.5	OFF
0	1	0	1	0	72	72	54	36	36	OFF
0	1	0	1	1	73	73	54.75	36.5	36.5	OFF
0	1	1	0	0	74	74	55.5	37	37	OFF
0	1	1	0	1	75	75	56.25	37.5	37.5	OFF
0	1	1	1	0	76	76	57	38	38	OFF
0	1	1	1	1	77	77	57.75	38.5	38.5	OFF
1	0	0	0	0	78	78	58.5	39	39	OFF
1	0	0	0	1	79	79	59.25	39.5	39.5	OFF
1	0	0	1	0	80	80	60	40	40	OFF
1	0	0	1	1	81	81	60.75	40.5	40.5	OFF
1	0	1	0	0	83.33	83.33	62.5	27.78	27.78	OFF
1	0	1	0	1	85	85	63.75	28.33	28.33	OFF
1	0	1	1	0	87.5	87.5	65.63	29.17	29.17	OFF
1	0	1	1	1	90	90	67.5	30	30	OFF
1	1	0	0	0	92.5	92.5	69.38	30.83	30.83	OFF
1	1	0	0	1	95	95	71.25	31.67	31.67	OFF
1	1	0	1	0	97.5	97.5	73.13	32.5	32.5	OFF
1	1	0	1	1	100.2	100.2	75.15	33.4	33.4	OFF
1	1	1	0	0	100	100	75	33.33	33.33	OFF
1	1	1	0	1	100	100	75	33.33	33.33	–0.5
1	1	1	1	0	100.2	100.2	75.15	33.4	33.4	±0.5
1	1	1	1	1	100.2	100.2	75.15	33.4	33.4	±0.25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ..... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions Over which Electrical Parameters are Guaranteed

Parameter	Description	Min.	Max.	Unit
V_{DD_REF}, V_{DD_PCI}, V_{DD_Core}, V_{DD_3V48M}, V_{DD_USB}	3.3V Supply Voltages	3.135	3.465	V
V_{DD_CPU}, V_{DD_MREF66}, V_{DD_APIC}, V_{DD_2V48}	2.5V Supply Voltages	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on: CPU, MREF66_50, APIC, 3V48, REF PCI SDRAM 2V48	 10 10 20 10	 20 30 30 15	 pF pF pF pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except XIN and SEL0. Threshold voltage for XIN = $V_{DD}/2$		2.0		V
V_{IL}	Low-level Input Voltage	Except XIN and SEL0. Threshold voltage for XIN = $V_{DD}/2$			0.8	V
V_{IHCPU2_EN}	High-level Input Voltage			70%		V_{DD}
V_{ILCPU2_EN}	Low-level Input Voltage				30%	V_{DD}
V_{OH}	High-level Output Voltage	CPU, MREF66_50, APIC, 2V48	I_{OH} = –1 mA	2.0		V
		PCI, 3V48, REF, SDRAM	I_{OH} = –1 mA	2.4		
V_{OL}	Low-level Output Voltage	CPU, MREF66,_50 APIC, 2V48	I_{OL} = 1 mA		0.4	V
		PCI, 3V48, REF, SDRAM	I_{OL} = 1 mA		0.4	
I_{IH}	Input High Current	$0 \le V_{IN} \le V_{DD}$			10	µA
I_{IL}	Input Low Current	$0 \le V_{IN} \le V_{DD}$			10	µA
I_{OH}	High-level Output Current	CPU, MREF66_50, APIC, 2V48	V_{OH} = 1.5V	–12	–59	mA
		3V48, 3V66/48, REF	V_{OH} = 1.5V	–16	–63	
		PCI	V_{OH} = 1.5V	–15	–100	
		SDRAM	V_{OH} = 1.5V	–15	–100	
I_{OL}	Low-level Output Current	CPU, MREF66_50, APIC, 2V48	V_{OL} = 1.5V	12	40	mA
		3V48, 3V66/48, REF	V_{OL} = 1.5V	9	27	
		PCI	V_{OL} = 1.5V	10	38	
		SDRAM	V_{OH} = 1.5V	–15	–100	
I_{OZ}	Output Leakage Current	Three-state			10	µA
I_{DD2}	2.5V Power Supply Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V			100	mA
I_{DD3}	3.3V Power Supply Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V			280	mA
I_{DDPD2}	2.5V Shutdown Current	AV_{DD}/V_{DD33} = 3.465V, V_{DD25} = 2.625V			100	µA
I_{DDPD3}	3.3V Shutdown Current	AV_{DD}/V_{DDQ3} = 3.465V, V_{DD25} = 2.625V			200	µA

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2}= 2.5V±5%
f_{XTL} = 14.31818 MHz
Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

AC Electrical Characteristics

Parameter	Description	Min.	Max.	Unit	Notes
T_{Period}	Host/CPUCLK Period	15.0	15.3	ns	
T_{HIGH}	Host/CPUCLK High Time	5.2	N/A	ns	3
T_{LOW}	Host/CPUCLK Low Time	5.0	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
T_{RISE}	Host/CPUCLK Rise Time	0.4	1.6	ns	5, 6
T_{FALL}	Host/CPUCLK Fall Time	0.4	1.6	ns	5, 6
T_{Period}	MREF66 Period	15.0	15.3	ns	7, 8
T_{HIGH}	MREF66 CLK High Time	5.2	N/A	ns	3
T_{LOW}	MREF66 CLK Low Time	5.0	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
T_{RISE}	MREF66 CLK Rise Time	0.4	1.6	ns	5, 6
T_{FALL}	MREF66 CLK Fall Time	0.4	1.6	ns	5, 6
T_{Period}	APIC 33-MHz CLK Period	30.0	N/A	ns	9, 10
T_{HIGH}	APIC 33-MHz CLK High Time	12.0	N/A	ns	3
T_{LOW}	APIC 33-MHz CLK Low Time	12.0	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
T_{RISE}	APIC 33-MHz CLK Rise Time	0.4	1.6	ns	5, 6
T_{FALL}	APIC 33-MHz CLK Fall Time	0.4	1.6	ns	5, 6

Notes:

3. T_{LOW} is measured at 0.4V for all outputs.
4. The time specified is measured from when V_{DDQ3} achieves its nominal operating level (typical condition V_{DDQ3} = 3.3V) until the frequency output is stable and operating within specification.
5. Period, jitter, offset, and skew measured on rising edge at 1.25 for 2.5V clocks and at 1.5V for 3.3V clocks.
6. The average period over any 1-µs period of time must be greater than the minimum specified period.
7. T_{HIGH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
8. Measured with duty cycle of input clock (SDRAM_IN) at 50%.
9. Output drivers must have monotonic rise/fall times through the specified V_{OL}/V_{OH} levels.
10. T_{RISE} and T_{FALL} are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.0V (1 mA) JEDEC specification for 2.5V outputs, and V_{OL} = 0.4V and V_{OH} = 2.4V for 3.3V.

AC Electrical Characteristics (continued)

Parameter	Description	Min.	Max.	Unit	Notes
T_{Period}	PCI CLK Period	30.0	N/A	ns	7, 8
T_{HIGH}	PCI CLK High Time	12.0	N/A	ns	3
T_{LOW}	PCI CLK Low Time	12.0	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	V/ns	
T_{RISE}	PCI CLK Rise Time	0.5	2.0	ns	5, 6
T_{FALL}	PCI CLK Fall Time	0.5	2.0	ns	5, 6
T_{Period}	3V48M CLK Period				
Edge Rate	Rising Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	V/ns	
T_{RISE}	3V48M CLK Rise Time	0.5	2.0	ns	
T_{FALL}	3V48M CLK Fall Time	0.5	2.0	ns	
T_{Period}	2V48M (DOT) CLK Period				
Edge Rate	Rising Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	V/ns	
T_{RISE}	2V48M CLK Rise Time	0.4	1.6	ns	5, 6
T_{FALL}	2V48M CLK Fall Time	0.4	1.6	ns	5, 6
T_PZL, T_PZH	Output Enable Delay (All outputs)	1.0	10.0	ns	
T_PLZ, T_PZH	Output Disable Delay (All outputs)	1.0	10.0	ns	
T_{STABLE}	All Clock Stabilization from Power-up		3.0	ms	8

SDRAM Driver AC Timing Requirements

Parameter	Description	Min.	Max.	Units	Notes
F_{MAX}	Maximum Operating Frequency		133	MHz	
T_PLH	LH Propagation Delay	5.5	7.5	ns	
T_PHL	HL Propagation Delay	5.5	7.5	ns	
Edge Rate	Rise Edge Rate (Type 4 Buffer 3.3V)	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 4 Buffer 3.3V)	1.0	4.0	V/ns	
T Rise	SDRAM CLK Rise Time	0.4	1.6	ns	5, 7
T Fall	SDRAM CLK Fall Time	0.4	1.6	ns	5, 7
T_PLZ, T_PZH	Output Disable Delay (All outputs	1.0	10.0	ns	
T_PLZ, T_PZH	Output Disable Delay (All outputs)	1.0	10.0	ns	

Table 2. Inter Group Skew and Jitter Limits

Output Group	Pin-pin Skew Max.	Cycle-Cycle Jitter Max.	Duty Cycle	Nom V_{DD}	Skew, Jitter measure point
CPU	175 ps	250 ps	45/55	2.5V	1.25V
APIC	250 ps	500 ps	45/55	2.5V	1.25V
MREF66_50	N/A	250 ps	45/55	2.5V	1.25V
2V48M	N/A	250 ps	45/55	2.5V	1.25V
3V48M	N/A	500 ps	45/55	3.3V	1.5V
PCI	500 ps	500 ps	45/55	3.3V	1.5V
REF	N/A	1000 ps	45/55	3.3V	1.5V
SDRAM	250 ps	N/A	45/55	3.3V	1.5V

Table 3. Group Offset Limits

Group	Offset	Measurement loads (lumped)	Measure Points	Notes
CPU to PCI	1.5–3.5 ns, CPU leads	CPU@20 pF, PCI@ 30 pF	CPU@1.5V, PCI@1.5V	11
CPU to IOAPIC	1.5–3.5 ns, CPU leads	CPU@20 pF, IOAPIC@20 pF	CPU@1.25V, IOAPIC@1.25V	11

Note:
11. All offsets are to be measured at rising edges.

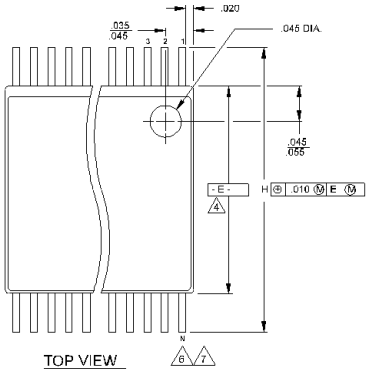
Ordering Information

Ordering Code	Package Name	Package Type
W281	H	48-pin SSOP

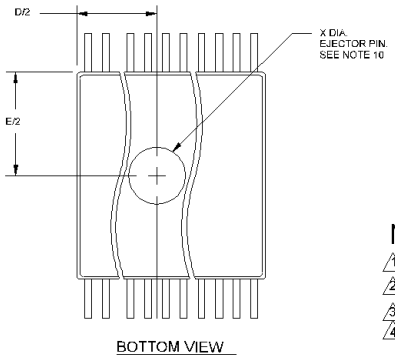
Document #: 38-00968-**

Package Diagram

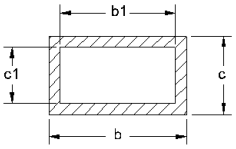
48-Pin Shrink Small Outline Package (SSOP, 300 mils)



TOP VIEW

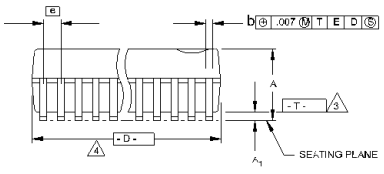


BOTTOM VIEW

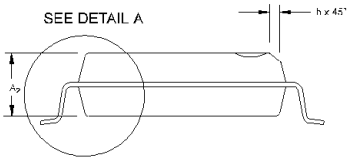


SECTION G-G 11

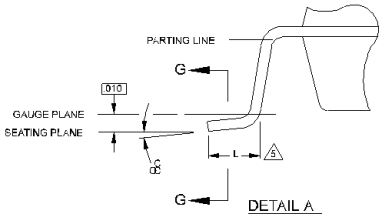
SCALE: NONE



SIDE VIEW



END VIEW



DETAIL A

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS			h/2 L	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			h/2 L	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

THIS TABLE IN MILLIMETERS