CY7C53150

Neuron® Chip Network Processor Errata List

Summary

Rev. B is the current revision of Cypress Neuron Chip. All known errata are fixed in the next revision of silicon (Rev. B+) which is due out at the end of July 2001.

Address Hold Time Violation

Description

Rev.B Neuron Chip does not meet the current Address Hold Time after E HIGH (t_{AH}) specification of 10 ns.

Implication

Device characterization at worst case temperature of –40°C is showing address hold times in the range of 8-9 ns (as measured from E at 2.0V to rising edge of address signal at 0.8V). It is possible that this errata will not effect most users at most temperature because the hold time as measured from 2.0V E to 0.8V Address is very close to 9 ns.

Workaround

Add delay/capacitance load to address path to be able to run the current device at worst case conditions (i.e., cold temperatures –40°C).

Status

The solution to the problem has been identified. It will be incorporated in the next revision of the device.

R/W Hold Time Violation

Description:

Rev.B Neuron Chip does not meet the current R/W Hold Time after E HIGH (tAH) specification of 5 ns.

Implication:

Device characterization at worst case temperature of –40°C is showing R hold times in the range of 2-3 ns and W hold times in the range of 4-5 ns (as measured from E at 2.0V to rising edge of address signal at 0.8V). It is possible that this errata will not effect most users at most temperature because the hold time as measured from 2.0V E to 0.8V R/W is very close to 4 ns.

Workaround:

Add delay/capacitance load to R/W path to be able to run the current device at worst case conditions (i.e., cold temperatures –40°C).

Status:

The solution to the problem has been identified. It will be in corporated in the next revision of the device.

Integrated 3 KB EEPROM support

Description:

Rev.B Neuron Chip features 3 KB of integrated EEPROM memory. However, only 512 bytes of this memory is supported by developement tools (NodeBuilder™ and LonBuilder™).

Implication:

Support for 3 KB of EEPROM is unavailable from Echelon's developement tools. It is possible that this errate will not affect most users because they may need only 512 bytes of memory which is currently supported by the development tools.

Workaround:

None

Status:

Cypress is working with Echelon to incorporate this support in the tool set. It will be implemented shortly.

Endurance Specification

Description:

The Rev.B Neuron Chip does not guaranty 100,000 write cycles.

Implication:

The Rev.B Neuron Chip has been tested for only 1000 write cycles under worst case conditions. Therefore, only 1000 write cycles are guaranteed. It is possible that this errata will not affect most users because mostlikely the design and debug phase of a product will not require more than 1000 writes.

Workaround:

None

Status:

The Rev.B Neuron Chip is undergoing the qualification tests for 100,000 write cycles under typical conditions. The results will be notified to the users when they are complete.

Document Title: Neuron® Chip Network Processor Errata List			
REV.	**Date Changed**	**Orig. of Change**	**Description of Change**
1.0	July 18, 2001	ALP	First release of the document