CPLD POWER CONSUMPTION COMPARISON

ALTERA, CYPRESS, LATTICE, VANTIS AND XILINX

TECHNICAL BRIEF **APRIL 1999**

INTRODUCTION

An important consideration in any system design is power consumption. Programmable logic in general, and CPLDs in particular, are becoming central components in today's systems. As such, CPLD power consumption is becoming a key factor when deciding which component to use. To aid in that decision making process, this document provides a comparison of CPLD power consumption for multiple vendors.

SCOPE

This power consumption comparison looks at CPLDs offered by Altera, Cypress, Lattice, Vantis and Xilinx. This includes devices that operate at both 5V and 3.3V. To achieve the comparison, this document provides an estimation of power versus operating frequency at room temperature and nominal voltage. The devices compared are listed in Table 1.

TABLE 1: DEVICES ANALYZED

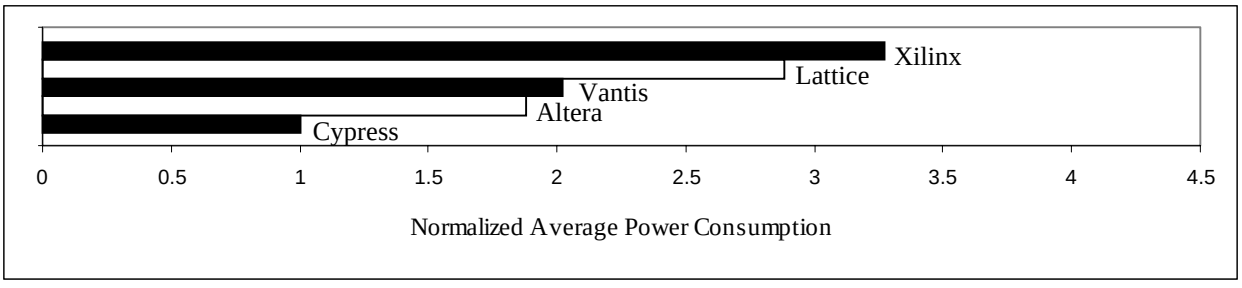
Company	Altera	Cypress	Lattice	Vantis	Xilinx
5V devices	MAX7000S	Ultra37000	ispLSI3000E	MACH4	XC9500
3.3V devices	MAX7000A	Ultra37000V	ispLSI5000V	MACH4LV	XC9500XL

Power consumption is plotted for the settings shown in Table 2. The data was obtained from each vendors' data sheets posted on their websites. To view references, please refer to the last section of this paper.

TABLE 2: SETTINGS ANALYSED

	High Power	Low Power[1]
Vcc = 3.3 [V]	X	X
Vcc = 5.0 [V]	X	X

SUMMARY OF RESULTS[2]



Notes:

1. Almost every CPLD in this comparison has the ability to operate in a lower power setting. This study compares CPLDs operating in the lowest power mode, as well as full power mode.
2. Power consumption for all devices, in all settings, from 0 to 50 MHz, was averaged and then normalized.

VCC = 5V AND HIGH POWER MODE

The following graph shows power versus frequency for 256 macrocell devices. The devices are operating in high power mode at a V_{cc} of 5V.

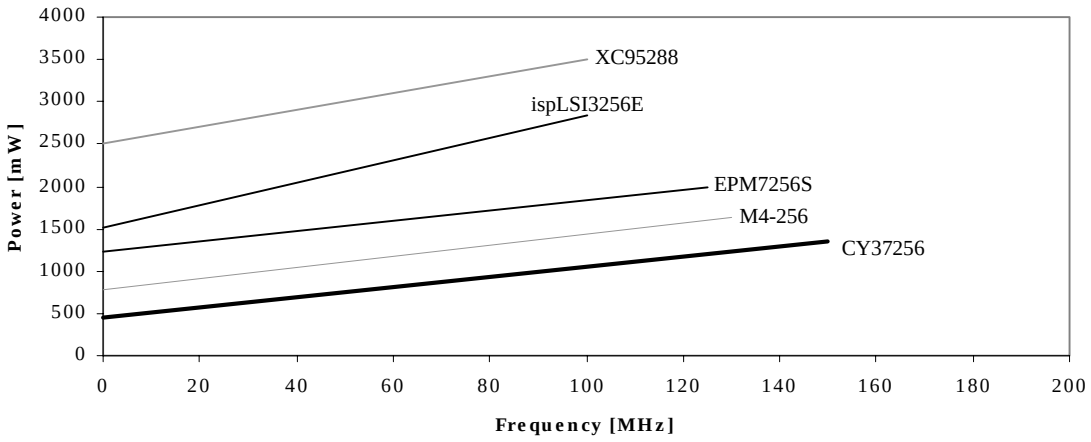


FIGURE 1: 256/288 MACROCELL DEVICES, VCC = 5V, HIGH POWER MODE

VCC = 5V AND LOW POWER MODE

The following graph shows power versus frequency for 256 macrocell devices. The devices are operating in low power mode at a V_{cc} of 5V.

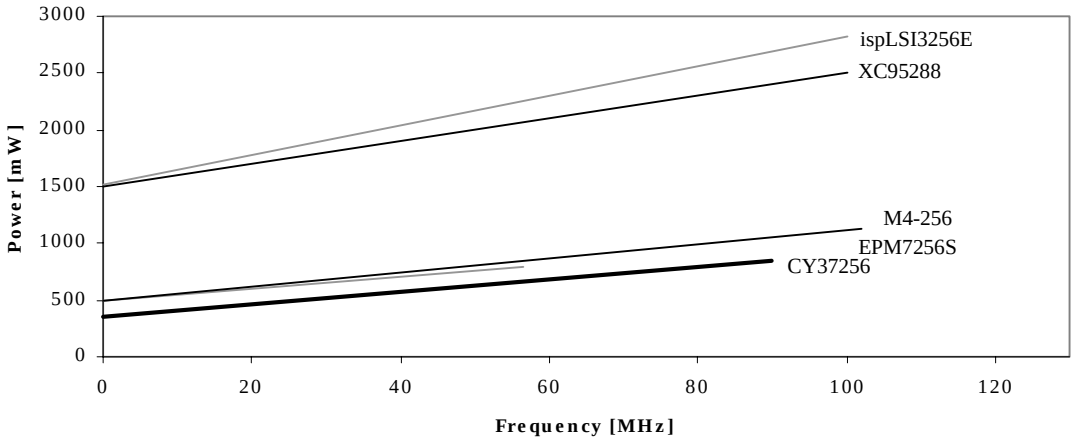


FIGURE 2: 256/288 MACROCELL DEVICES, VCC = 5V, LOW POWER MODE

VCC = 3.3V AND HIGH POWER MODE

The following graph shows power versus frequency for 256 macrocell devices. The devices are operating in high power mode at a V_{cc} of 3.3V.

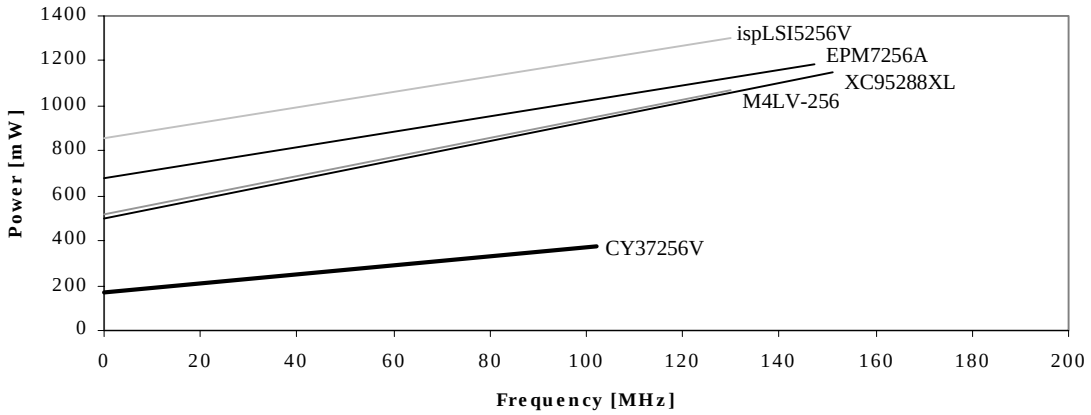


FIGURE 3: 256/288 MACROCELL DEVICES, VCC = 3.3V, HIGH POWER MODE

VCC = 3.3V AND LOW POWER MODE

The following graph shows power versus frequency for 256 macrocell devices. The devices are operating in low power mode at a V_{cc} of 3.3V.

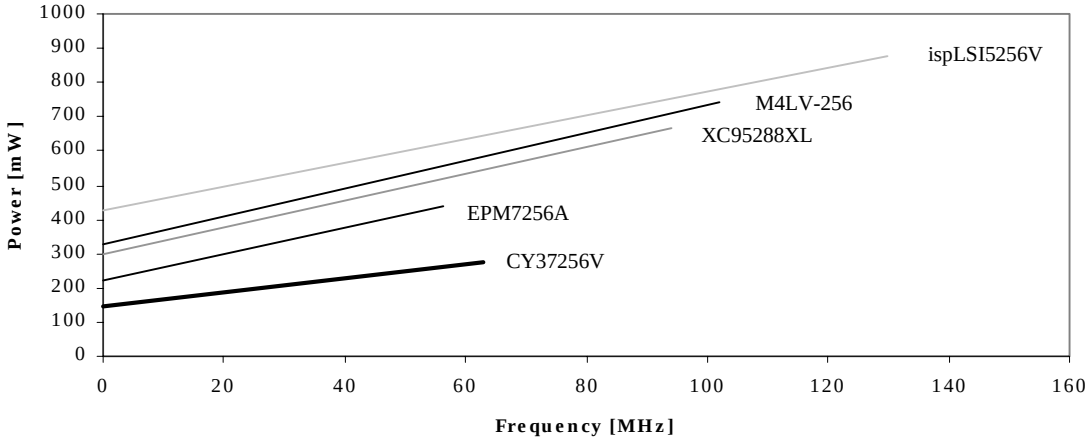


FIGURE 4: 256/288 MACROCELL DEVICES, VCC = 3.3V, LOW POWER MODE

REFERENCES

Company	Device	Source	Date
Altera	MAX7000S MAX7000A	www.altera.com	July 1998 January 1999
Cypress	Ultra37000 Ultra37000V	www.cypress.com	January, 1999 January, 1999
Lattice	ispLSI3000E ispLSI5000V	www.latticesemi.com	October 1998 February 1999
Vantis	MACH4(LV)	www.vantis.com	December 1998
Xilinx	XC9500 XC9500XL	www.xilinx.com	December 4 1998 September 28 1998