PRELIMINARY

Delta39K™ and Quantum38K™ I/O Standards and Configurations

Introduction

As Delta39K™ and Quantum38K™ approach the densities previously found only in FPGAs, the potential for applications using high-density CPLDs has increased dramatically. In order to support a wide variety of applications from general purpose standard applications to high performance memory and backplane interfaces, Delta39K and Quantum38K have architectures to support the new features of programmable I/Os and the AnyVolt™ interface. Quantum38K supports a subset of the I/O standards that Delta39K supports. This document will refer to Delta39K and the observations will be applicable to Quantum38K if the I/O Standard is supported by Quantum38K. All of the supported I/O standards are listed in *Table 1*.

On any Delta39K device, I/Os are grouped into I/O blocks. Each I/O block has a maximum of 21 I/O cells, an Output Control Channel (OCC), and a configuration block. The number of I/O cells bonded out from an I/O block is determined by the number of I/Os offered in each package configuration. Each I/O cell drives a pin output of the device and supplies an input to the device that connects to a dedicated track in the associated outing channel. The I/O blocks are grouped to form eight programmable I/O banks. Each device in the Delta39K CPLD family has eight I/O banks and a varying number of I/O blocks depending on the device density. Each individual input and output pin on these programmable I/O banks can be configured to conform to the one of the 15 industry I/O standards in simple steps, using *Warp*® Release 6.0 software tools.

In a modern bus application, a new I/O standard is often introduced by the influential digital electronics companies that tailor to their specific application needs. Each I/O standard is unique in its own requirements, such as voltage, current, I/O buffering and termination techniques. Therefore, the capability to provide highly configurable and easy-to-use I/Os to support a variety of I/O standards is in ever-increasing demand.

The Delta39K supports a variety of I/O standards, such as the basic I/O standards of LVCMOS18, LVCMOS2, LVCMOS3, LVCMOS, LVTTL, and 3.3V PCI standards as well as the high performance memory and backplane interfaces including SSTL2, SSTL3, HSTL and GTL+.

The Delta39K family also offers the AnyVolt™ interface. The logic core operates at 1.8V, and Cypress uses an on-chip voltage regulator to support 2.5V and 3.3V power supplies as well. Therefore, the I/Os can interface at 1.8V, 2.5V or 3.3V regardless of the supply voltage.

Table 1. Delta39K Supported I/O Standards

I/O Standards	V_{CCIO}	V_{REF}	V_{TT}
LVTTL (24 mA, 16 mA, 12 mA, 8 mA, 6 mA, 4 mA, 2 mA)[1]	3.3V	N/A	N/A
LVCMOS[1]	3.3V	N/A	N/A
LVCMOS3[1]	3.0V	N/A	N/A
LVCMOS2[1]	2.5V	N/A	N/A
LVCMOS18[1]	1.8V	N/A	N/A
3.3V PCI[1]	3.3V	N/A	N/A
GTL+	N/A	1.0V	1.5V
SSTL3 Class I & II	3.3V	1.5V	1.5V
SSTL2 Class I & II	2.5V	1.25V	1.125V
HSTL Class I & II	1.5V	0.75V	0.75V
HSTL Class III & IV	1.5V	0.9V	1.5V

Outline of I/O Standard Specifications

While most of the I/O standards specify a range of constraints, this document only summarizes the typical voltage values and sample termination circuit of the Delta39K supported I/O standards. Detailed information can be obtained from the individual specifications as necessary.

The specifics discussed below include the typical termination circuit, the supply voltage (V_{CCIO}), the sink and source signal voltage levels (V_{IL},V_{IH},V_{OL},V_{OH}), the reference voltage level (V_{REF}) and the termination voltage level (V_{TT}) where it applies.

Note:
1. This I/O Standard is supported by Quantum38K.

HSTL — High Speed Transceiver Logic

The High Speed Transceiver Logic (HSTL) standard is a high-speed general-purpose bus standard created by IBM, with four classes of variations. This standard uses a differential amplifier input buffer and a push-pull output buffer. This standard requires a 1.5V supply voltage (V_{CCIO}), the use of a reference voltage (V_{REF}) of 0.75V and an on-board termination voltage (V_{TT}) of 0.75V for Class I & II and V_{TT} of 0.9V for Class III and IV. The DC voltage specifications for all four classes of HSTL standard are listed in *Table 2* through *Table 5*.

Table 2. HSTL Class I DC Parameters[2]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	1.4	1.5	1.6
V_{REF}	0.68	0.75	0.9
$V_{TT} = V_{CCIO}/2$	0.7	0.75	0.8
V_{IH}	V_{REF}+0.1		V_{CCIO} + 0.3
V_{IL}	–0.3	-	V_{REF}–0.1
V_{OH} (I_{OH}= –8 mA)	V_{CCIO}–0.4	-	-
V_{OL} (I_{OL}= 8 mA)	-	-	0.4

A sample termination circuit for HSTL Class I is shown in *Figure 1*. A sample termination circuit for HSTL Class II is shown in *Figure 2*. A sample termination circuit for HSTL Class III is shown in *Figure 3*. A sample termination circuit for HSTL Class IV is shown in *Figure 4*.

Table 3. HSTL Class II DC Parameters[2]

DC Parameters	Min	Typ	Max
V_{CCIO}	1.4	1.5	1.6
V_{REF}	0.68	0.75	0.9
V_{TT}	0.7	0.75	0.8
V_{IH}	V_{REF}+0.1	-	V_{CCIO}+0.3
V_{IL}	–0.3	-	V_{REF}–0.1
V_{OH} (I_{OH} = –16 mA)	V_{CCIO}–0.4	-	-
V_{OL} (I_{OL} = 16 mA)	-	-	0.4

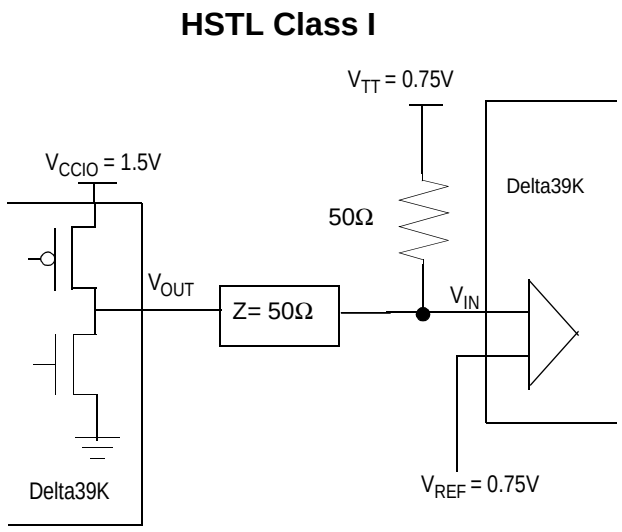

Figure 1. Sample HSTL Class I Termination Circuit

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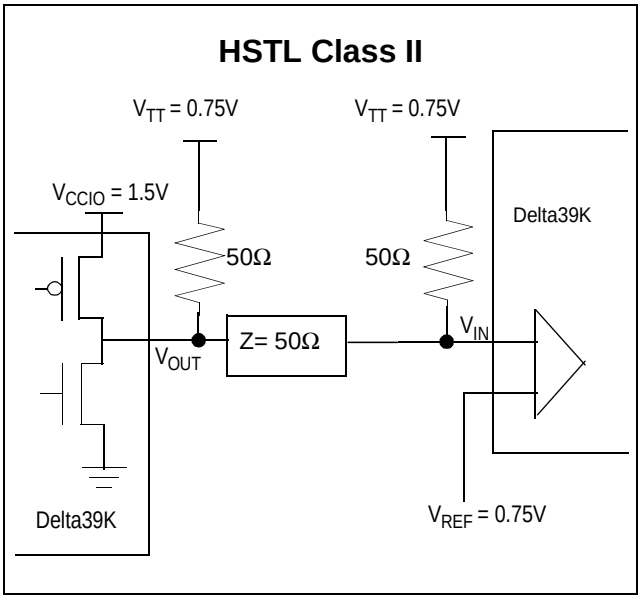

Figure 2. Sample HSTL Class II Termination Circuit

Note:
2. See HSTL specification JESD8-6 from www.jedec.org for reference.

Table 4. HSTL Class III DC Parameters[2]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	1.4	1.5	1.6
V_{REF}	0.68	0.9	0.9
$V_{TT} = V_{CCIO}$	1.4	1.5	1.6
V_{IH}	V_{REF}+0.1	-	V_{CCIO}+0.3
V_{IL}	–0.3	-	V_{REF}–0.1
V_{OH} (I_{OH} = –8 mA)	V_{CCIO}–0.4	-	-
V_{OL} (I_{OL} = 24 mA)	-	-	0.4

Table 5. HSTL Class IV DC Parameters[2]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	1.4	1.5	1.6
V_{REF}	0.68	0.9	0.9
$V_{TT} = V_{CCIO}$	1.4	1.5	1.6
V_{IH}	V_{REF} + 0.1	-	V_{CCIO} + 0.3
V_{IL}	–0.3	-	V_{REF} – 0.1
V_{OH} (I_{OH} = –8 mA)	V_{CCIO}–0.4	-	-
V_{OL} (I_{OL} = 48 mA)	-	-	0.4

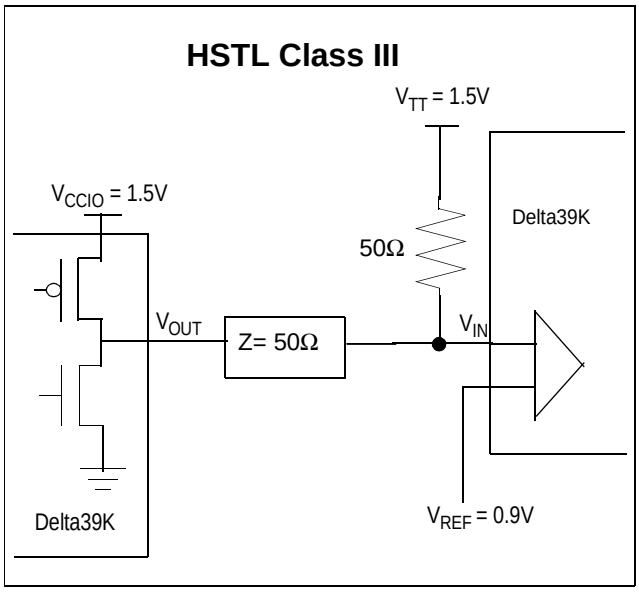

Figure 3. A Sample HSTL Class III Termination Circuit

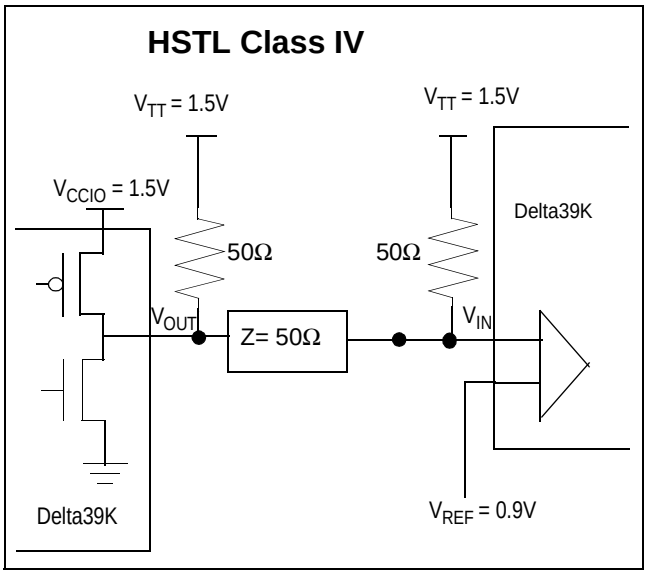

Figure 4. Sample HSTL Class IV Termination Circuit.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V (SSTL2) standard is a high-speed, general-purpose memory bus standard for 2.5V applications, created by Hitachi and IBM, with 2 classes of variations. This standard uses a differential amplifier input buffer and a push-pull output buffer. This standard requires a 2.5V supply voltage (V_{CCIO}), the use of a reference voltage (V_{REF}) of 1.25V and an on-board termination voltage (V_{TT}) of 1.25V.

Table 6 lists the DC voltage specifications for the SSTL2 standard.

A sample termination circuit for SSTL Class I is shown in *Figure 5*. A sample termination circuit for SSTL2 Class II is shown in *Figure 6*.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3, standard is a high speed, general purpose memory bus standard for 3.3V applications, created by Hitachi and IBM, with 2 classes of variations. This standard uses a differential amplifiers input buffer and a push-pull output buffer setup. This standard requires a 3.3V supply voltage (V_{CCIO}), the use of a reference voltage (V_{REF}) of 1.5V and an on-board termination voltage (V_{TT}) of 1.5V.

Table 6. SSTL2 DC Parameters Class I & II[3]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	2.3	2.5	2.7
V_{REF}	1.15	1.25	1.35
V_{TT}	V_{REF}–0.04	V_{REF}	V_{REF}+0.04
V_{IH}	V_{REF}+0.18	-	V_{CCIO}+0.3
V_{IL}	–0.3	-	V_{REF}–0.18
Class I V_{OH}[4] (I_{OH} = –7.6 mA)	-	-	-
Class II V_{OH}[4] (I_{OH} = –15.2 mA)	-	-	-
Class I V_{OL}[4] (I_{OL} = 7.6 mA)	-	-	-
Class II V_{OL}[4] (I_{OL} = 15.2 mA)	-	-	-

Table 7 lists the DC voltage specifications for the SSTL3 standard..

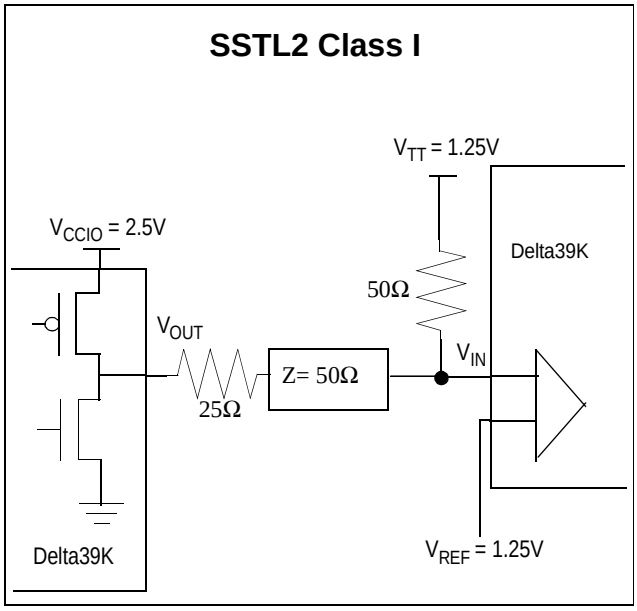

Figure 5. Sample SSTL2 Class I Termination Circuit

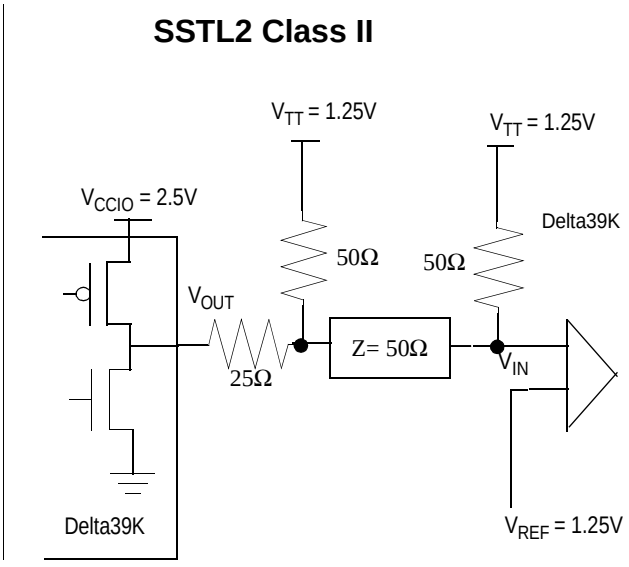

Figure 6. Sample SSTL2 Class II Termination Circuit

Notes:
3. See SSTL2 specification, JESD8-9 from www.jedec.org for reference.
4. VOH, VIH are not specified under DC test conditions. See section 3 of the SSTL2 specification, JESD8-9 from www.jedec.org for reference.

Table 7. SSTL3 DC Parameters Class I & II

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	3.0	3.3	3.6
V_{REF}	1.3	1.5	1.7
V_{TT}	V_{REF}-0.05	V_{REF}	V_{REF}+0.05
V_{IH}	V_{REF}+0.2	-	V_{CCIO}+0.3
V_{IL}	–0.3	-	V_{REF}-0.2
Class I V_{OH}[6] (I_{OH} = –8 mA)	-	-	-
Class II V_{OH}[6] (I_{OH} = –16 mA)	-	-	-
Class I V_{OL}[6] (I_{OL} = 8 mA)	-	-	-
Class II V_{OL}[6] (I_{OL} = 16 mA)	-	-	-

A sample termination circuit for SSTL3 Class I is shown in *Figure 7*. A sample termination circuit for SSTL3 Class I is shown in *Figure* .

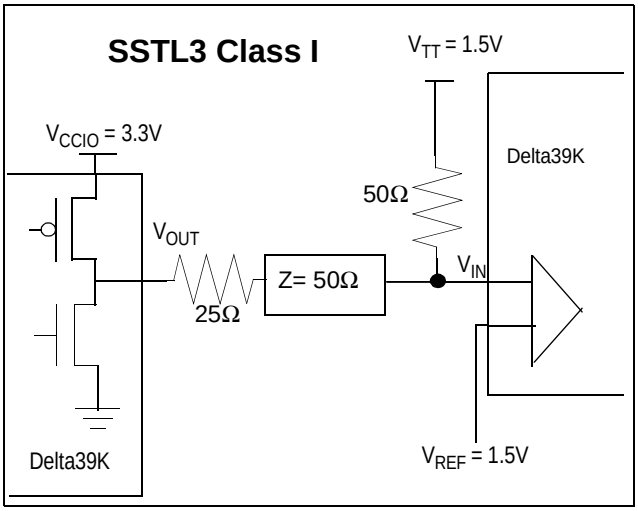

Figure 7. Sample SSTL3 Class I Termination Circuit

GTL+ - Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus (GTL+) is a high speed standard used by the Pentium Pro processor. It is an extension to the original GTL standard, enhanced to connect up to 8 devices operating at 66.6MHz and higher with better noise margin and reduced ringing than the GTL standard. This standard requires a differential amplifier input buffer and an open drain output buffer. This standard does not require a specific supply voltage (V_{CCIO}). However, it requires the use of a reference voltage (V_{REF}) of 1.0V and an on-board termination voltage (V_{TT}) of 1.5V. In addition, the I/O drivers should be characterized to specifications, using an Intel specified load network, REF8N. For more details, refer to the detailed Intel specifications.*Table 8* lists the DC voltage specifications for the GTL+ standard.

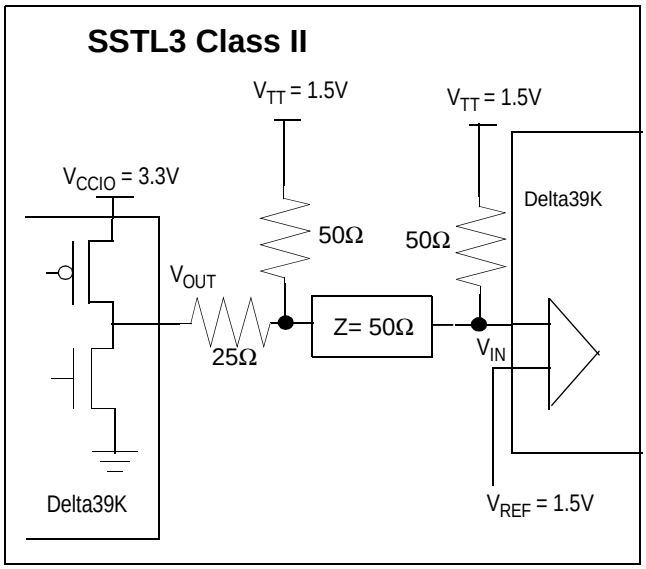

Figure 8. Sample SSTL3 Class II Termination Circuit

Table 8. GTL+ DC Parameters

DC Parameters	Min	Typ	Max
V_{CCIO}[7]	N/A	N/A	N/A
V_{REF}	2/3 * V_{TT} – 2%	2/3 * V_{TT}	2/3 * V_{TT} +2%
V_{TT}	1.35	1.5	1.65
V_{IH}	V_{REF}+0.2	-	V_{CCIO}
V_{IL}	–0.3[8]	-	V_{REF}-0.2
V_{OH}	-	-	1.65 (V_{TT} max)
V_{OL} (I_{OL} = 36mA)	0.3	-	0.6

Notes:
5. See SSTL3 specification, JESD8-8 from www.jedec.org for reference.
6. VOH, VIH are not specified under DC test conditions. See section 3 of the SSTL3 specification, JESD8-8 from www.jedec.org for reference
7. V_{CCIO} is not specified in the GTL+ specification. See the GTL+ data sheet, http://developer.intel.com/design/pro/datashts/reference.htm
8. V_{IL} minimum does not conform to formula $V_{IL} = V_{REF} – 0.2V$. See GTL+ data sheet, http://developer.intel.com/design/pro/datashts/reference.htm

A sample termination circuit for GTL+ is shown in *Figure 9*.

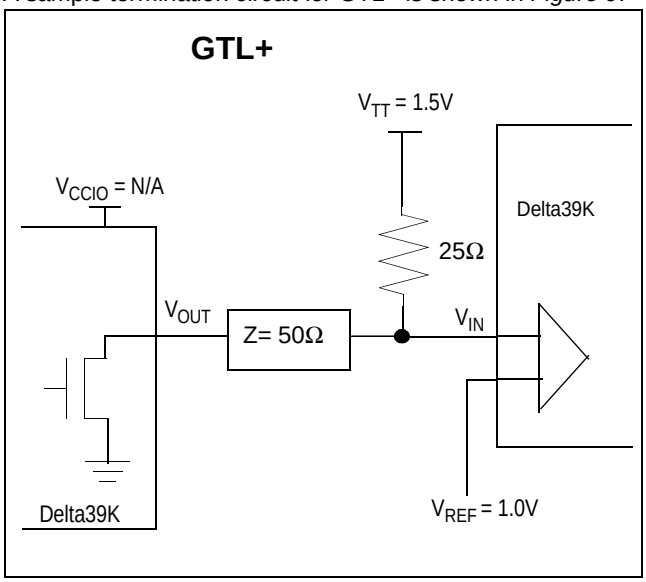

Figure 9. GTL+ Termination Circuit

3.3V PCI — Peripheral Component Interface

The Peripheral Component Interface (PCI) standard, originated by Intel's PCI Group, supports both 33-MHz and 66-MHz PCI local bus application. Delta39K and Quantum38K support the 3.3V PCI standard. They use a PCI input buffer and a push-pull output buffer. This standard requires a 3.3V supply voltage (V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or an on-board termination voltage (V_{TT}). It also requires no special termination circuit.

* Note that to support the PCI bus standard, AC parameters also must be met by the user's design. Refer to the PCI Specification 2.2, www.pcisig.com. PCI also has a capacitance requirement for CLK, data, and IDSEL pins. Refer to the Delta 39K data sheet for details regarding the pins that support the capacitance requirements outlined in Table 4-3 of the PCI Specification 2.2.

Table 9 lists the DC voltage specifications for the PCI standard.

Table 9. 3.3V PCI DC Parameters[9]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	3.0	3.3	3.6
V_{IH}	$0.5V_{CCIO}$	-	V_{CCO}+0.5
V_{IL}	–0.5	-	$0.3V_{CCIO}$
V_{OH}	$0.9V_{CCIO}$	-	-
V_{OL}	-	-	$0.1V_{CCIO}$

LVCMOS3 & LVCMOS

The Low-Voltage CMOS (LVCMOS) standard is a general-purpose standard. LVCMOS3 is defined by a 3.0V supply voltage (V_{CCIO}) and LVCMOS by a 3.3V supply voltage (V_{CCIO}). The 3.0V is associated It does not require the use of a reference voltage (V_{REF}) or an on-board termination voltage (V_{TT}). It has no special termination circuit requirement. A Delta39K device can be driven by a LVCMOS3 or LVCMOS device that is powered by 3.3V, however it will never see 5V. Refer to the application note, "Interfacing the Delta39K to 5V Devices" for further details.

Table 10 and *Table 11* list the DC voltage specifications of LVCMOS3 and LVCMOS standards.

Table 10. LVCMOS3 DC Parameters[10]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	2.7	3.0	3.6
$V_{IH} = V_{CCIO} + 0.3$	2.0	-	V_{CCIO}+0.3
V_{IL}	–0.3	-	0.8
V_{OH} (I_{OH} = – 0.1 mA)	V_{CCIO} – 0.2	-	-
V_{OL} (I_{OL} = 0.1 mA)	-	-	0.2

Table 11. LVCMOS DC Parameters[10]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	3.0	3.3	3.6
V_{IH}	2.0	-	V_{CCIO}+0.3
V_{IL}	–0.3	-	0.8
V_{OH} (I_{OH} = –0.1 mA)	V_{CCIO}-0.2	-	-
V_{OL} (I_{OL} = 0.1 mA)	-	-	0.2

LVTTL

The Low-Voltage TTL (LVTTL) standard is a general-purpose standard for 3.3V applications. This standard requires a 3.3V supply voltage (V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or an on-board termination voltage (V_{TT}). It has no special termination circuit requirement. A Delta39K device can be driven by a LVTTL device that is powered by 3.3V; however it should never be driven by a 5V signal. Refer to the application note, "Interfacing the Delta39K to 5V devices" and the Delta39K datasheet for further details. *Table 12* lists the DC voltage specifications for the LVTTL standard.

Notes:
9.Refer to PCI specification 2.2, www.pcisig.com.
10. See LVCMOS3 specification, JESD8-B from www.jedec.org, for reference.

Table 12. LVTTL DC Parameters[11]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	3.0	3.3	3.6
V_{IH}	2.0	-	3.9
V_{IL}	–0.3	-	0.8
V_{OH} = (I_{OH} = –2.0 mA)	2.4	-	-
V_{OL} (I_{OL} = 2.0 mA)	-	-	0.4

LVCMOS2

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is used for general purpose 2.5V applications. This standard requires a 2.5V supply voltage, but does not require the use of a reference voltage (V_{REF}) or an on-board termination voltage (V_{TT}). It has no special termination circuit requirement.

Table 13 lists the DC voltage specifications for the LVCMOS2 standard.

Table 13. LVCMOS2 DC Parameters[11]

DC Parameters		Min.	Typ.	Max.
V_{CCIO}		2.3	2.5	2.7
V_{IH}		1.7	-	V_{CCIO}+0.3
V_{IL}		–0.3	-	0.7
V_{OH}	(I_{OH} = –0.1 mA)	2.1	-	-
	(I_{OH} = –1.0 mA)	2.0	-	-
	(I_{OH} = –2.0 mA)	1.7	-	-
V_{OL}	(I_{OL} = 0.1 mA)	-	-	0.2
	(I_{OL}= 1.0 mA)	-	-	0.4
	(I_{OL}= 2.0 mA)	-	-	0.7

LVCMOS18

LVCMOS18 is a general purpose standard for 1.8V applications that uses a push-pull output buffer, but no particular input buffer is required. This standard requires a 1.8V supply voltage (V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or an on-board termination voltage (V_{TT}). It has no special termination circuit requirement.

Table 14 lists the DC voltage specifications for the 1.8V interference standard.

Table 14. LVCMOS18 DC Parameters[13]

DC Parameters	Min.	Typ.	Max.
V_{CCIO}	1.65	1.8	1.95
V_{IH}	0.65V_{CCIO}	-	V_{CCIO}+0.3
V_{IL}	–0.3	-	0.35V_{CCIO}
V_{OH} (I_{OH} = –2.0 mA)	1.2	-	-
V_{OL} (I_{OL}= 2.0 mA)	-	-	0.45

I/O Bank Compatibility

As stated in the previous section, the I/O blocks are grouped to form programmable I/O banks. Each I/O block has a common routing channel. Each I/O bank has a common V_{CCIO} supply voltage. For example, the CY39100 has 14 I/O blocks, 3 each on the left and right side and 4 each on the top and bottom of the die. The I/O blocks are combined in a fashion as shown in *Figure 10* to form I/O banks.

There are eight I/O banks in each Delta39K device. Note that I/O block 1 and I/O block 8 are split I/O blocks which resides on 2 different I/O banks. In the Delta39K device, the configuration of the I/O standard is defined in groups called I/O banks.

Each I/O bank has its own dedicated I/O power supply (V_{CCIO}). The V_{CCIO} between the different I/O banks are not connected together, resulting in eight separate I/O power supplies on the chip. The I/O bank on the Delta39K family device allow for having multiple I/O standards on the device at the same time.

Due to the difference in the voltage requirements for each I/O standard, in order to have more than one I/O standard to co-exist on the same I/O bank, the I/O set-up should comply with the following rules:

1. I/O standards not requiring a V_{REF} input can be used in the same I/ O bank as any other I/O standard with the same V_{CCIO} supply.
2. I/O standards having a V_{REF} input must reside in an I/O bank with an I/O that uses the same V_{CCIO} supply and the same V_{REF}.

Compatibility of the I/O standards on the same I/O bank must be observed in order for the I/Os to function correctly. The compatibility of the supported I/O standards are listed in *Table 15*.

Notes:
11. See LVTTL specification, JESD8-B from www.jedec.org, for reference.
12. See LVCMOS2 specification, JESD8-5 from www.jedec.org, for reference.
13. See LVCMOS18 specification, JESD8-7 from www.jedec.org, for reference.

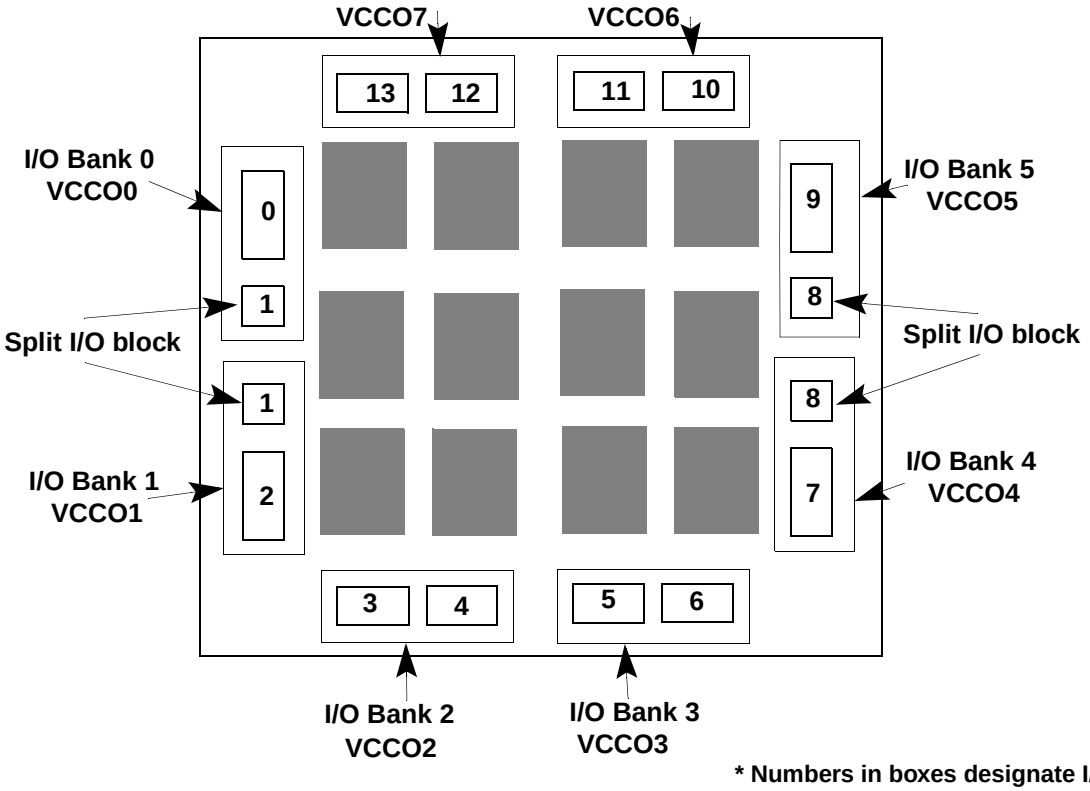

Figure 10. CY39100 I/O Bank Configuration

Table 15. Compatibility of Supported I/O Standards

I/O Standards	LVCMOS18	LVCMOS2	LVCMOS3	LVCMOS	LVTTL	3.3V PCI	GTL+	STTL2 Class I & II	STTL3 Class I & II	HSTL Class I & II	HSTL Class III & IV
LVCMOS18	Y	N		N	N	N	Y	N	N	N	N
LVCMOS2	N	Y		N	N	N	Y	Y	N	N	N
LVCMOS3			Y				Y				
LVCMOS	N	N		Y	Y	Y	Y	N	Y	N	N
LVTTL	N	N		Y	Y	Y	Y	N	Y	N	N
PCI	N	N		Y	Y	Y	Y	N	Y	N	N
GTL+	Y	Y	Y	Y	Y	Y	Y	Y**	Y**	Y**	Y**
SSTL2 Class I & II	N	Y		N	N	N	Y**	Y	N	N	N
SSTL3 Class I & II	N	N		Y	Y	Y	Y**	N	Y	N	N
HSTL Class I & II	N	N		N	N	N	Y**	N	N	Y	Y**
HSTL Class III & IV	N	N		N	N	N	Y**	N	N	Y**	Y

Y denotes that the I/O standards are fully compatible

Y** denotes that only input/output or output/output combination of I/O standards are compatible

N denotes that the I/O standards are not compatible

I/O Constraints with Density Migration

As you migrate to different densities with Delta39K, a given I/O pin retains its bank assignment. This allows for simple implementation of multiple I/O standards during the design and proto-typing phase, before a final density has been determined. This feature is known as True Vertical Migration.™

I/O Limit per I/O Bank

The maximum number of I/Os allowed per bank is based on the corresponding I/O standard and the characteristics of the device. This is due to the high current requirements of some of the I/O Standards. See *Table 16* for a listing of the I_{OH}/I_{OL} requirements of the I/O Standards supported by Delta39K/Quantum38K.

The design procedure to be used to determine if the device current limits are being violated follows:

First, refer to the device data sheet to determine the maximum source and sink current limits per V_{CCIO}/GND_{IO} pin. For example, CY39100 has a maximum source current limit of 165 mA per V_{CCIO} and a maximum sink current limit of 230 mA per GND_{IO} pin (Delta39K data sheet, section on DC Characteristics (IO)).

Second, determine the design requirements. The example design has the following requirements:

CY39100V676

20 HSTL III I/Os in Bank 3

22 HSTL I I/Os in Bank 3

The next step is determining the I_{OH} required for each of the I/O Standards used. For our example, the total source current required is 20 * 8 + 22 * 8 = 336 mA. The total sink current requirement is 20 * 24 + 22 * 8 = 656 mA. Reviewing the Delta39K pin tables reveals that the there are four V_{CCIO}s for bank 3. Note that the number of GND_{IO}s is equal to the number of V_{CCIO}s (although GND_{IO}s are labeled GND in the datasheet). Therefore, the V_{CCIO}s for bank 3 can source a total of 165*4 = 660 mA and the GND_{IO}s can sink a total of 230*4 = 920 mA. Since neither the source limit or the sink limit is exceeded, the I/O distribution for bank 3 falls within the design parameters of the CY39100V676.

Table 16. I/O Standard I_{OH}/I_{OL} Limits

I/O Standard	I_{OH} (mA)	I_{OL} (mA)
LVTTL24mA	24	24
LVTTL16mA	16	16
LVTTL12mA	12	12
LVTTL8mA	8	8
LVTTL6mA	6	6
LVTTL4mA	4	4
LVTTL2mA	2	2
LVCMOS	0.1	0.1
LVCMOS3	0.1	0.1
LVCMOS2	2	2
LVCMOS18	2	2
3.3V PCI	N/A[14]	N/A[14]
GTL+	N/A[15]	36
SSTL3 I	8	8
SSTL3 II	16	16
SSTL2 I	7.6	7.6
SSTL2 II	15.2	15.2
HSTL I	8	8
HSTL II	16	16
HSTL III	8	24
HSTL IV	8	48

As another example, consider the following case:

CY39100V676

42 LVTTL24 mA I/Os in Bank 3

In this case, the total source current restriction stays the same (660 mA source), except now our design requirement is 42 * 24 = 1008 mA, which is outside the limits of the CY39100 device. If a design were to use LVTTL24mA for all 42 I/Os in bank 3, and the design had loads such that it required the full 24 mA source/sink capability of the I/O standard for every one of the 42 I/Os, the design would violate the current limits of the CY39100.

Non-I/O Pins

Besides programmable I/O banks, Delta39K also features non-I/O pins which are isolated from the I/O bank partitioning process and are used for global signals, configuration and testing purposes. These non-I/O pins includes Global Clock pins (GCLK), Global Control pins (GCTL), a Configuration port, and a JTAG port. All non-I/O pins are 3.3V tolerant. For more detailed information on the functions of these Non-I/O pins, please refer to the Delta39K Data Sheet.

Global Clock (GCLK) and Global Control (GCTL) Pins

There is a total of four global clock (GCLK) pins and four global control (GCTL) pins on each Delta39K device. They are distributed in four I/O banks, and their input buffer is sourced by the V_{CCIO} of the I/O bank in which they reside. The GCLK and GCTL pins may co-exist in the same I/O bank with any of the 14 supported I/O standards. The GCLK and GCTL input buffers have configuration bits to choose between the various I/O standards. These configuration bits are part of the I/O bank configuration bits and get configured along with the I/O cell configuration.

The GCLK pins provide inputs for clock selections of the registers in the I/O cells and the Delta39K logic. The GCTL pins can be used as inputs for the control signals, such as output enable, register reset, or register enable of the I/O cells (they are not available to logic).

Configuration Port

The Configuration port has its own dedicated power supply (V_{CCNFG}) and is compatible with the following I/O standards: LVCMOS18, LVCMOS2, LVCMOS3, LVCMOS, and LVTTL. The configuration pins do not have their I/O standard set via the I/O standards GUI in *Warp*; the I/O standard is determined by V_{CCCNFG}. The most common configuration is LVTTL/LVCMOS, which is chosen by using a 3.3V supply voltage for V_{CCCNFG}. Refer to the application note “Configuring Delta39K/Quantum38K” for further details.

JTAG Pins

The JTAG port consists of four pins and its own dedicated power supply pin (V_{CCJTAG}) that allows the user to access the boundary scan cell elements. It complies with the *IEEE 1149.1* Standard Test Access Port standards. The JTAG port is used for boundary scan testing, ISR programming and non-volatile FLASH memory configuration. The C3ISR cable is recommended to interface to the JTAG pins of the Delta39K, but the UltraISR cable may be used with no problems if V_{CCJTAG} is 3.3V

Configuring I/O Properties using *Warp* Release 6.x software tools

The latest version of the Cypress *Warp* Release 6.x software tools is equipped with a GUI to support I/O standard configuration on Delta39K. The GUI is launched from the Galaxy menu Project-Configure IO Standards. Besides the configuration of the I/O type, the user can configure other signal parameters, such as slew clock and bus hold enable, with in the same dialog box.

When signals are assigned to I/O pins, the pin assignment information will be written to a text file (*.pin). The I/O Properties interface reads from this assignment file, and display all I/O signals on the dialog box for the user to define individually the I/O properties of each signal.

Note:
14. PCI does not define DC I_{OH}/I_{OL} parameters. Refer to the PCI 2.2 specification at www.pcisig.com for details.
15. GTL+ is open-drain; hence their is no I_{OH} requirement.Refer to the GTL+ specification, http://developer.intel.com/design/pro/datashts/reference.htm

When finished, the I/O properties dialog will store the information into a text-based control file (*.ctl). The control file is automatically generated after the first I/O configuration or can be created by the user. The I/O properties are specified in the control file as attributes.

When launching the I/O properties function from Galaxy, a three-tab dialogue box will show up on the screen. Within this dialogue box, the user is allowed to set the default I/O property, the I/O bank type, and the I/O property for each individual I/O signal.

Setting the Default I/O Properties

In many case, a user's design will consist primarily of one I/O type. *Warp*'s default I/O standard for Delta39K devices is LVCMOS. Therefore, *Warp* will initially set every I/O, clock and global control to LVCMOS and will allow the user to change the I/O standard to any I/O type the user chooses. To set the I/O standard, the user will:

1. Launch the I/O Properties dialog box and select the *"Default I/O Properties"* tab (*Figure 11*).
2. Set each of the properties in the *"Properties"* section at the top of the tab to the desired values.
3. Press the *"Set Defaults"* button, then *"Reset All"* button.

Pressing *"Set Defaults"* button will set the chosen properties on every I/O signal ***that is set to the current default***. I/O signals that are not set to the current default will remain unchanged and the I/O bank settings will also remain unchanged.

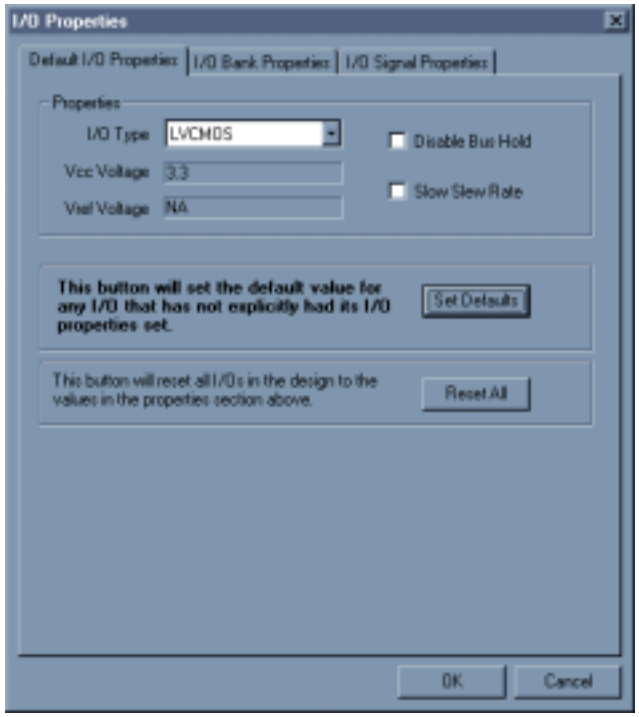

Figure 11. Default I/O Properties Dialog Box

When the *"Reset All"* button is pressed, the user will be issued a warning that states that every I/O is about to be changed in the GUI display (*Figure 12*). The dialog will ask for the user confirmation. If *"OK"* is chosen, then every I/O signal will be changed to the chosen properties and every I/O Bank will be set to the chosen V_{CC} and V_{REF} voltages.

Figure 12. Reset All Warning Dialog Box

Selecting I/O Bank Properties

The I/O Bank V_{CC} and V_{REF} voltages are set via the *"I/O Bank Properties"* tab, as shown in *Figure 13*. The V_{CC} and V_{REF} voltages are simply selected via the drop-down list boxes supplied for each of the eight I/O banks. In general, the I/O bank settings will never be restricted, meaning that the user can always change the V_{CC} and V_{REF} voltages to any valid value regardless of any other settings, such as existing I/O signal properties.

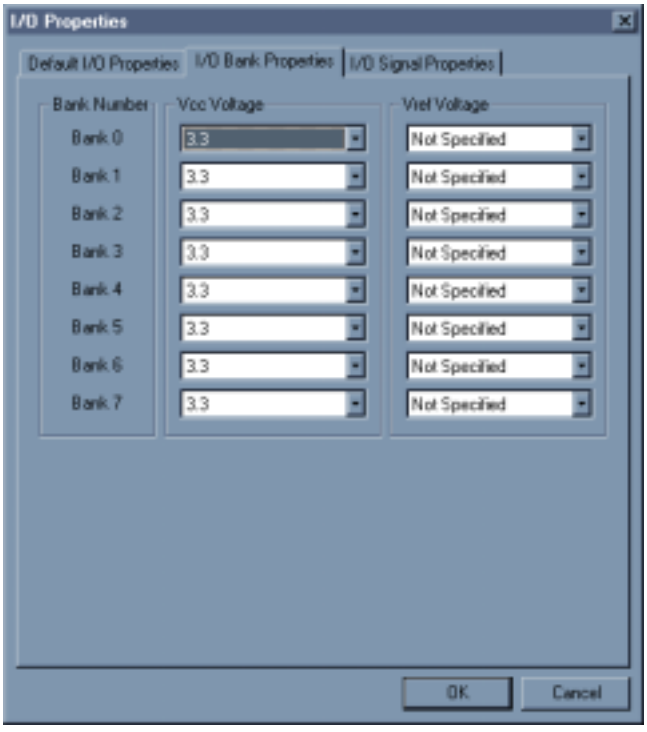

Figure 13. Default I/O Properties Dialog Box

Setting I/O Signal Properties

The user can set the I/O properties for each of the signals listed individually using the third tab in the I/O Signal Properties Dialog, as shown in *Figure 14*.

1. Highlight the signal(s) to be modified.
2. Select the desired properties in the "*Properties*" section of the tab.
3. Press the "*Update Signals*" button.

Selecting Signal(s)

There are several ways in which signals shown in the Signal List can be selected. Individual signals can be selected with a left mouse click. Multiple signals can be selected using the standard Shift or Ctrl-left-mouse-click.

In addition, the *"Signal Name Filter"* edit box allows the user to input a filter string. This string is initially set to * so that all signals are listed. The user can enter a new filter string into the box and when the *"Enter"* key is pressed, the Signal List will display only the signal names which contain the filter string. The user can also press the *"Select All"* button to select all signals currently displayed in the Signal List.

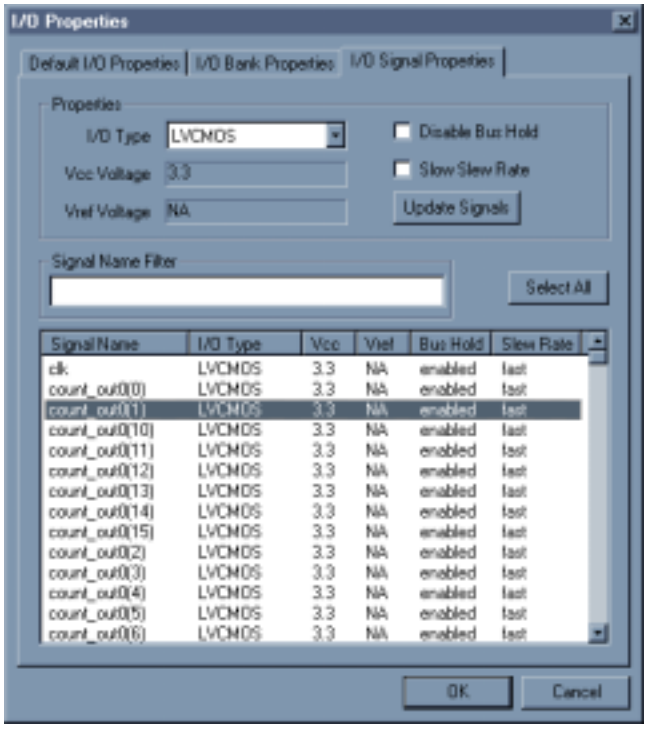

Figure 14. I/O Signal Properties Dialog Box

Selecting Properties

The I/O Type, V_{CC} voltage and V_{REF} voltage properties are selected via a drop down list box. In the list box, all available settings will be listed and the user can simply left click on the desired selection. The available selections will be limited to valid selections based on I/O Bank settings. The following will influence what property choices are greyed out:

1. When the I/O type is selected, only the valid V_{CC} and V_{REF} voltages can be selected. All other voltages will be greyed out.
2. When choosing a V_{CC} and V_{REF} value, only values that have been set using the *"I/O Bank Properties"* tab will be available.

The bus hold enable/disable is specified via a check box. If the box is checked, the bus hold will be Disabled, otherwise, the bus hold will be Enabled. The slew rate for each I/O is also specified via a check box. If the box is checked, the slew rate will be set to slow; otherwise, it will be set to fast.

Modifying I/O Attributes in the Control File

Within the control file, there are three attributes that define that I/O properties. User can change the attributes either via the I/O Property GUI or by changing the attribute values on the control file.

Default I/O Properties Attribute

The first attribute describes the default I/O properties for any I/Os that are not defined by I/O signal attribute. The attribute correspond to the "*Default I/O Property*" page on the I/O property dialogue box. This attribute only appears once, and will automatically assigned the I/O type to any unspecific I/Os. The attribute displays in the form of:

```
ATTRIBUTE IO_TYPE OF <ENTITY_NAME>: ENTITY IS
"<IO_TYPE, VCC_VALUE, VREF_VALUE>"
```

where

```
IO_TYPE:= LVCMOS2 | LVTTL_24mA | LVTTL_16mA
| LVTTL_12mA | LVTTL_8mA | LVTTL_6mA
| LVTTL_4mA | LVTTL_2mA | LVCMOS
| LVCMOS3_0 | PCI |GTL_PLUS | HSTL_CLASS_I
| HSTL_CLASS_II | HSTL_CLASS_III
| HSTL_CLASS_IV | SSTL2_CLASS_I
| SSTL3_CLASS_I | SSTL2_CLASS_II
| SSTL3_CLASS_II
VCC_VALUE:= 3.3, 3.0, 2.5, 1.8, 1.5, N/A
VREF_VALUE ::= 1.5, 1.25, 1.0, 0.9, 0.75, N/A
```

For example, in entity < DESIGN>, the default I/O type is LVCMOS, where V_{CCIO} = 3.3V and there is no V_{REF} requirement, then the attribute will display:

```
ATTRIBUTE IO_TYPE OF DESIGN: ENTITY IS
"<LVCMOS, 3.3, N/A>";
```

I/O Bank Properties Attribute

The second attribute describes the I/O property of the I/O bank. The attribute correspond to the "I/O Bank Property" page on the I/O property dialogue box. The attribute displays in the form of:

```
ATTRIBUTE IO_BANK OF <ENTITY-NAME> : ENTITY IS
"<BANK_NUMBER0, VCC_VALUE0, VREF_VALUE0>
<BANK_NUMBER1, VCC_VALUE1, VREF_VALUE1>..."
```

where

```
BANK_NUMBER ::= 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7
VCC_VALUE ::= 3.3, 3.0, 2.5, 1.8, 1.5, N/A
VREF_VALUE* ::= 1.5, 1.25, 1.0, 0.9, 0.75
```

*** Note that for VREF_VALUE of I/O bank attribute, where there is no V_{REF} requirement, the VREF_VALUE is displayed blank.**

For example, in entity < DESIGN>, if 2 out of the 8 banks are defined as follows:

Bank0 : has V_{CCIO} = 1.5V, V_{REF} = 0.9V (HSTL Class III & IV)

Bank3 : has V_{CCIO} = 3.3V, V_{REF} = N/A

The attribute will be :

```
ATTRIBUTE IO_BANK OF DESIGN : ENTITY IS
"<0, 1.5, 0.9><3, 3.3, >";
```

I/O Signal Properties Attribute

The third attribute describes the I/O property of a signal name. The attribute correspond to the "*I/O Signal Property*" page on the I/O property dialogue box. Each attribute statement defines property of one signal. The attribute displays in the form of:

```
ATTRIBUTE IO_TYPE OF SIGNAL <SIG_NAME> : SIGNAL
IS "<IO_TYPE, VCC_VALUE, VREF_VALUE>"
```

where

```
IO_TYPE ::= LVCMOS2 | LVTTL | LVCMOS | PCI |
    GTL_PLUS | HSTL_CLASS_I | HSTL_CLASS_II
    | HSTL_CLASS_III | HSTL_CLASS_IV |
    SSTL2_CLASS_I_II | SSTL3_CLASS_I_II
VCC_VALUE ::= 3.3, 3.0, 2.5, 1.8, 1.5, N/A
VREF_VALUE ::= 1.5, 1.25, 1.0, 0.9, 0.75, N/A
```

For example, if signal name PCI_IN is a PCI type signal, where V_{CCIO} = 3.3V and there is no V_{REF} requirement, the attribute will be:

```
ATTRIBUTE IO_TYPE OF SIGNAL PCI_IN: SIGNAL IS
"<PCI, 3.3, N/A>";
```

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