



CY7C371

UltraLogic™ 32-Macrocell Flash CPLD

Features

- 32 macrocells in two logic blocks
- 32 I/O pins
- 6 dedicated inputs including 2 clock pins
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
 - $f_{MAX} = 143 \text{ MHz}$
 - $t_{PD} = 8.5 \text{ ns}$
 - $t_S = 5 \text{ ns}$
 - $t_{CO} = 6 \text{ ns}$
- Electrically alterable FLASH technology
- Available in 44-pin PLCC, CLCC, and TQFP packages
- Pin compatible with the CY7C372

Functional Description

The CY7C371 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370 family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C371 is designed to bring the ease

of use and high performance of the 22V10 to high-density CPLDs.

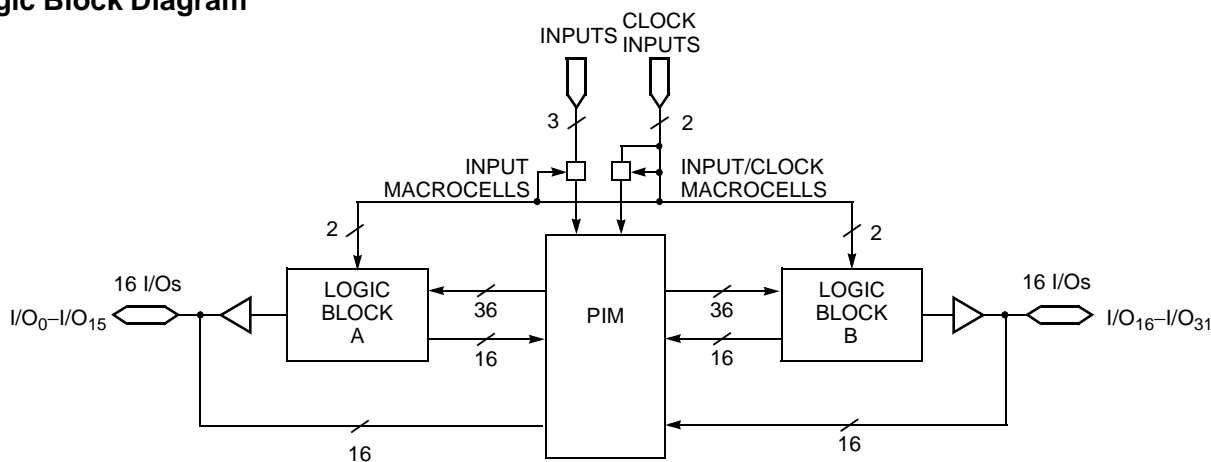
The 32 macrocells in the CY7C371 are divided between two logic blocks. Each logic block includes 16 macrocells, a 72×86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C371 is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C371 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C371 remain the same.

Logic Block Diagram



Selection Guide

		7C371-143	7C371-110	7C371-83	7C371L-83	7C371-66	7C371L-66
Maximum Propagation Delay, t_{PD} (ns)		8.5	10	12	12	15	15
Minimum Set-Up, t_S (ns)		5	6	10	10	12	12
Maximum Clock to Output, t_{CO} (ns)		6	6.5	10	10	12	12
Maximum Supply Current, I_{CC} (mA)	Commercial	220	175	175	90	175	90
	Military/Ind.			220	110	220	110

Shaded area contains preliminary information.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State -0.5V to +7.0V
 DC Input Voltage -0.5V to +7.0V
 DC Program Voltage 12.5V

Output Current into Outputs (LOW)..... 16 mA

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to ± 70°C	5V ± 5%
Military ^[1]	-55°C to ± 125°C	5V ± 10%
Industrial	-40°C to ± 85°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -3.2 mA (Com'l/Ind)	2.4		V
			I _{OH} = -2.0 mA (Mil)			V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 16 mA (Com'l/Ind)		0.5	V
			I _{OL} = 12 mA (Mil)			V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs ^[3]		2.0	7.0	V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs ^[3]		-0.5	0.8	V
I _{Ix}	Input Load Current	V _I = Internal GND, V _I = V _{CC}		-10	+10	μA
I _{OZ}	Output Leakage Current	V _O = Internal GND, V _O = V _{CC}		-50	+50	μA
I _{OS}	Output Short Circuit Current ^[4, 5]	V _{CC} = Max., V _{OUT} = 0.5V		-30	-160	mA
I _{CC}	Power Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = 1 MHz, V _{IN} = GND, V _{CC} ^[6]		Com'l	175	mA
				Com'l "L" -66, -83	90	mA
				Com'l -143,	220	mA
				Mil/Ind	220	mA
				Ind "L" -66, -83	110	mA

Shaded area contains preliminary information.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{I/O} ^[7, 8]	Input Capacitance	V _{IN} = 5.0V at f=1 MHz	10	pF

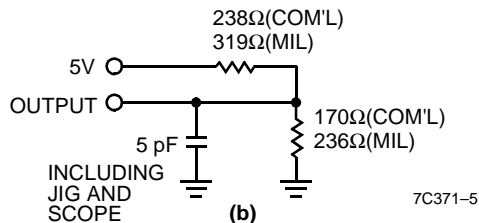
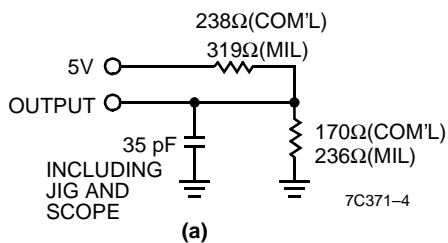
Endurance Characteristics^[5]

Parameter	Description	Test Conditions	Min.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100	Cycles

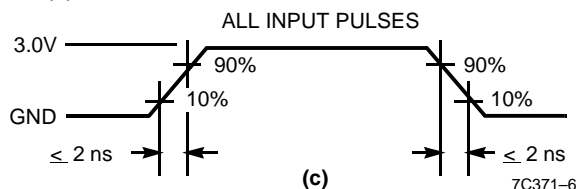
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Measured with 16-bit counter programmed into each logic block.
7. C_{I/O} for the CLCC package is 15 pF Max.
8. C_{I/O} for I₁ is 15 pF Max.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT
 99Ω (COM'L) 2.08V (COM'L)
 136Ω (MIL) 2.13V (MIL)



Parameter ^[9]	V _X	Output Waveform Measurement Level
t _{ER} (-)	1.5V	V _{OH} 0.5V V _X 7c371-7
t _{ER} (+)	2.6V	V _{OL} 0.5V V _X 7c371-8
t _{EA} (+)	1.5V	V _X 0.5V V _{OH} 7c371-9
t _{EA} (-)	V _{thc}	V _X 0.5V V _{OL} 7c371-10

(d) Test Waveforms

Switching Characteristics Over the Operating Range^[10]

Parameter	Description	7C371-143		7C371-110		7C371-83 7C371L-83		7C371-66 7C371L-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t _{PD}	Input to Combinatorial Output		8.5		10		12		15	ns
t _{PDL}	Input to Output Through Transparent Input or Output Latch		11.5		13		18		22	ns
t _{PDLL}	Input to Output Through Transparent Input and Output Latches		13.5		15		20		24	ns
t _{EA}	Input to Output Enable		13		14		19		24	ns
t _{ER}	Input to Output Disable		13		14		19		24	ns
Input Registered/Latched Mode Parameters										
t _{WL}	Clock or Latch Enable Input LOW Time ^[5]	2.5		3		4		5		ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[5]	2.5		3		4		5		ns
t _{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t _{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t _{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		12		14		19		24	ns
t _{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		14		16		21		26	ns

Notes:

- t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
- All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

Switching Characteristics Over the Operating Range^[10] (continued)

Parameter	Description	7C371-143		7C371-110		7C371-83 7C371L-83		7C371-66 7C371L-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Output Registered/Latched Mode Parameters										
t _{CO}	Clock or Latch Enable to Output		6		6.5		10		12	ns
t _S	Set-Up Time from Input to Clock or Latch Enable	5		6		10		12		ns
t _H	Register or Latch Data Hold Time	0		0		0		0		ns
t _{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		12		14		19		24	ns
t _{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	7		9		12		15		ns
t _{SCS2}	Output Clock Through Array to Output Clock (2-Pass Delay) ^[5]	13		16.5		21		27		ns
t _{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	9		10		12		15		ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f _{MAX1}	Maximum Frequency with Internal Feedback (Least of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) ^[5]	143		111		83.3		66.6		MHz
f _{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO}) ^[5]	166.7		153.8		100		83.3		MHz
f _{MAX3}	Maximum Frequency with external feedback (Lesser of 1/(t _{CO} + t _S) and 1/(t _{WL} + t _{WH})) ^[5]	91		80		50		41.6		MHz
t _{OH} -t _{IH} 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x ^[5, 11]	0		0		0		0		ns
Pipelined Mode Parameters										
t _{ICS}	Input Register Clock to Output Register Clock	7		9		12		15		ns
f _{MAX4}	Maximum Frequency in Pipelined Mode (Least of 1/(t _{CO} + t _{IS}), 1/t _{ICS} , 1/(t _{WL} + t _{WH}), 1/(t _{IS} + t _{IH}), or 1/t _{SCS})	125		111		76.9		62.5		MHz
Reset/Preset Parameters										
t _{RW}	Asynchronous Reset Width ^[5]	8		10		15		20		ns
t _{RR}	Asynchronous Reset Recovery Time ^[5]	10		12		17		22		ns
t _{RO}	Asynchronous Reset to Output		14		16		21		26	ns
t _{PW}	Asynchronous Preset Width ^[5]	8		10		15		20		ns
t _{PR}	Asynchronous Preset Recovery Time ^[5]	10		12		17		22		ns
t _{PO}	Asynchronous Preset to Output		14		16		21		26	ns

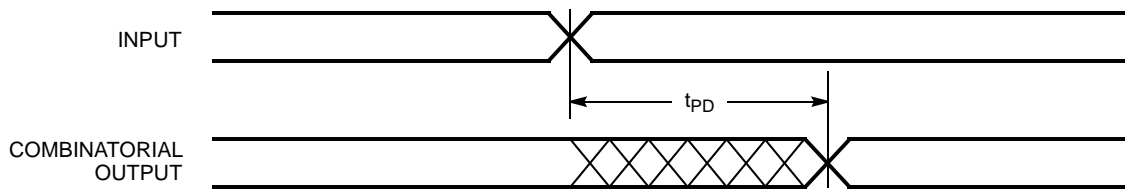
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Note:

11. This specification is intended to guarantee interface compatibility of the other members of the CY7C370 family with the CY7C371. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

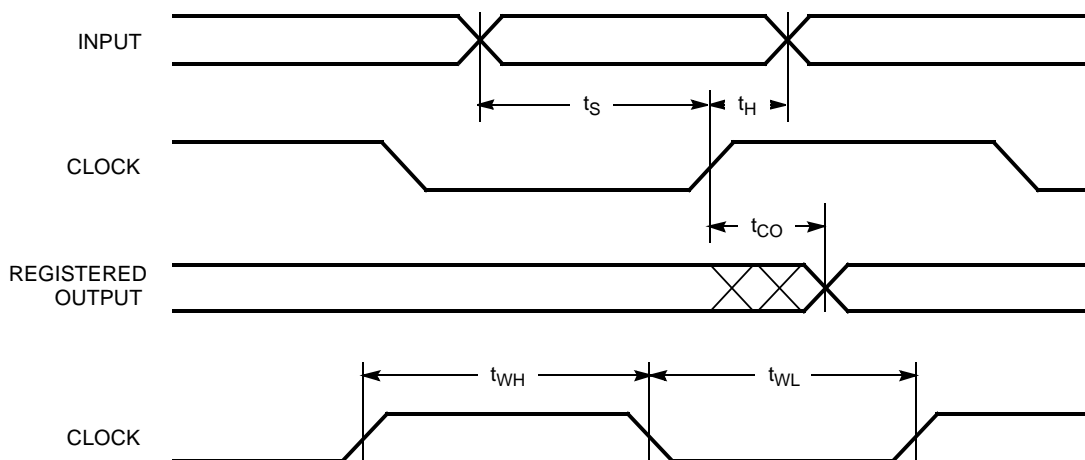
Switching Waveforms

Combinatorial Output



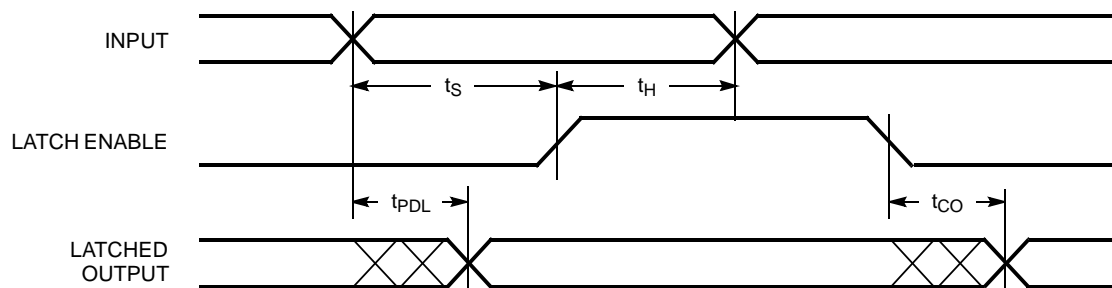
7c371-11

Registered Output

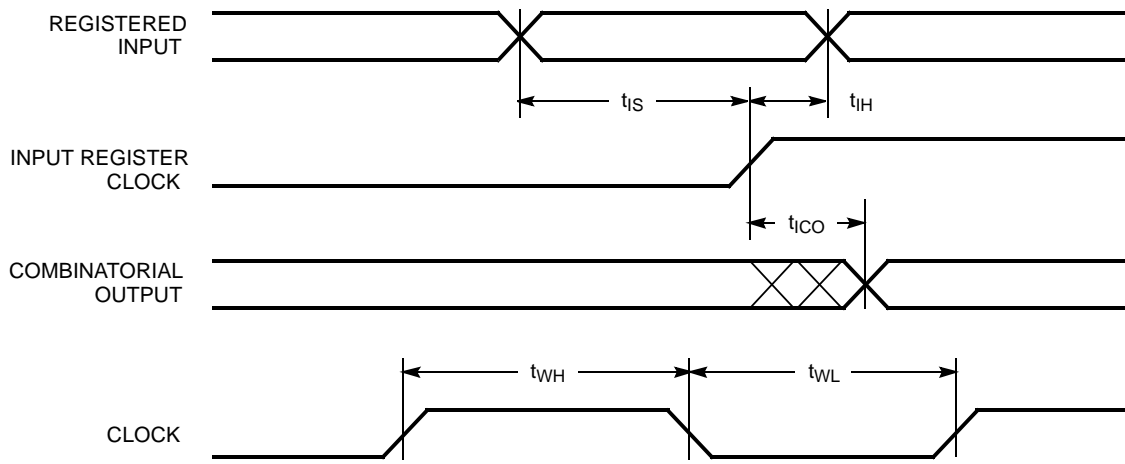


7c371-12

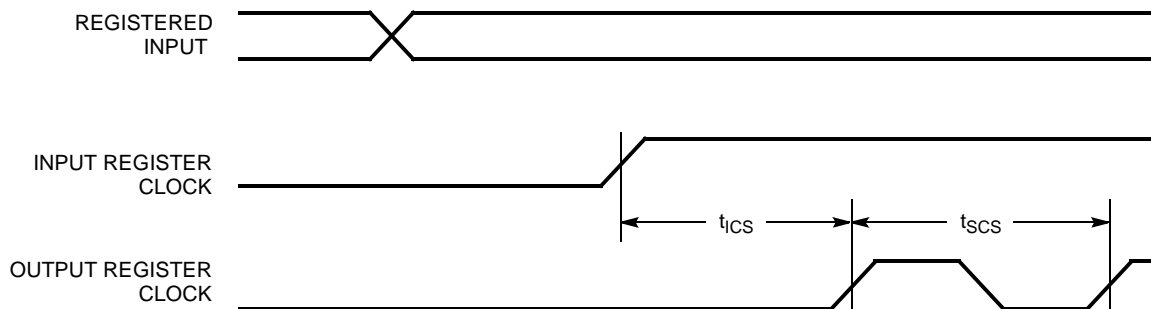
Latched Output



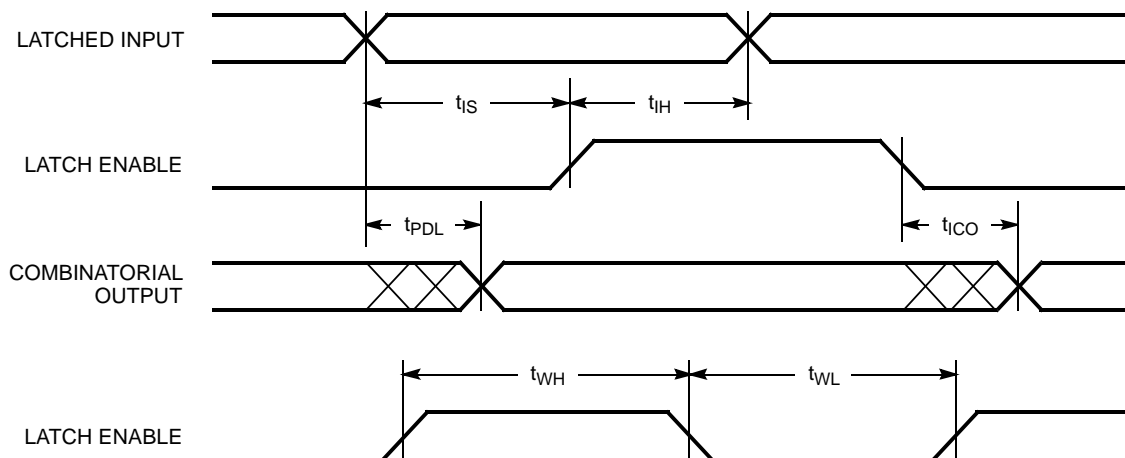
7c371-13

Switching Waveforms (continued)
Registered Input


7c371-14

Clock to Clock


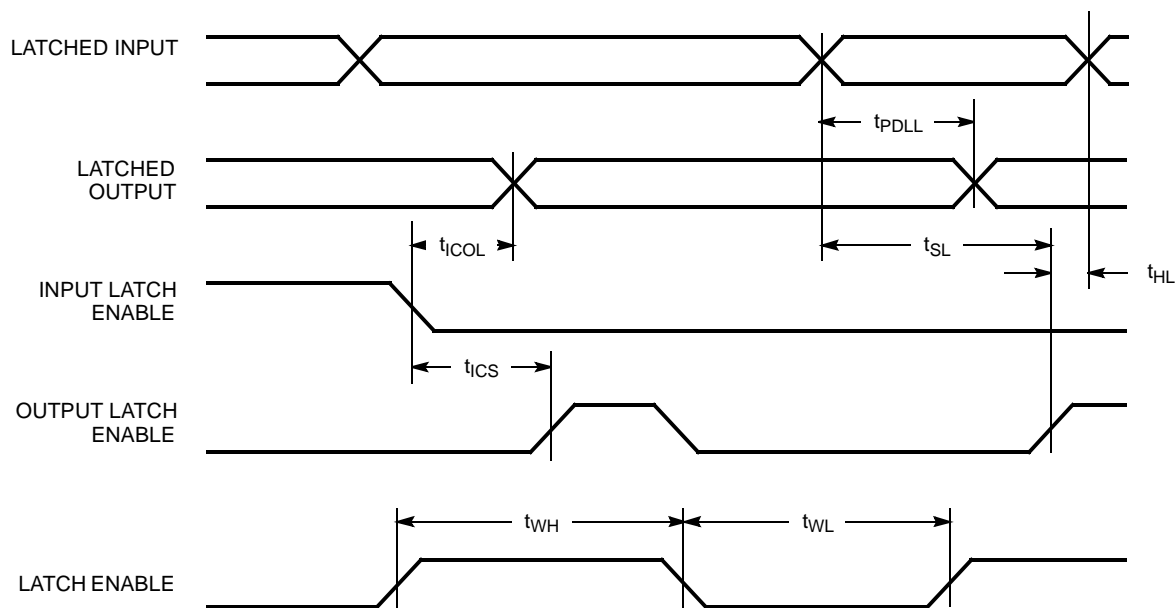
7c371-15

Latched Input


7c371-16

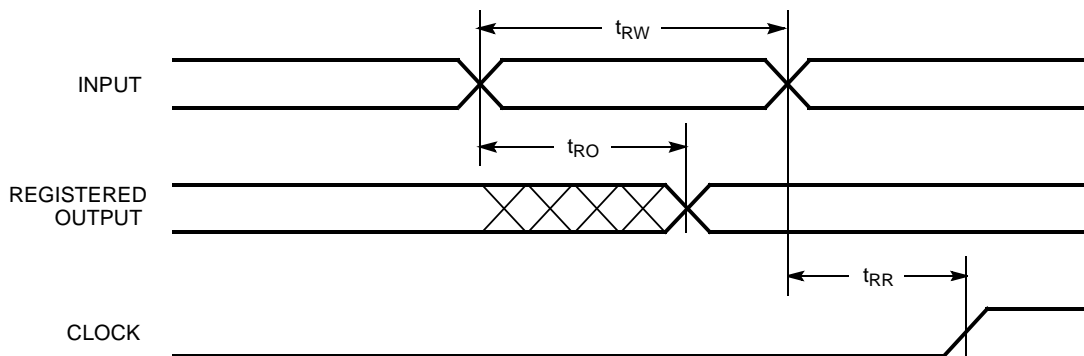
Switching Waveforms (continued)

Latched Input and Output



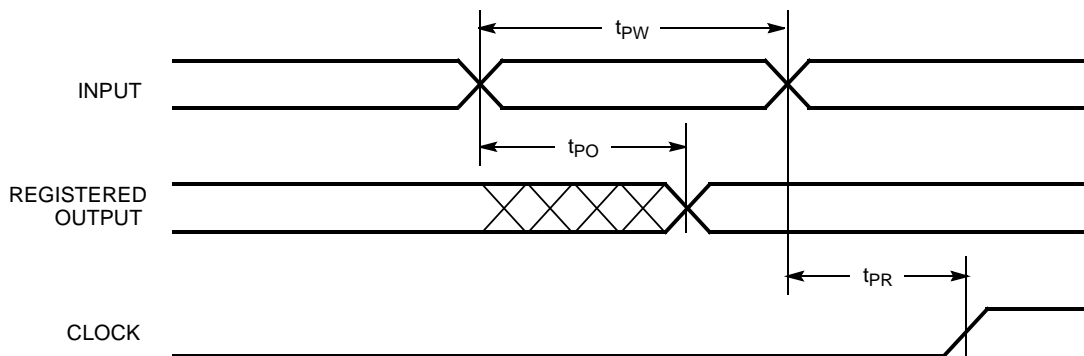
7c371-17

Asynchronous Reset



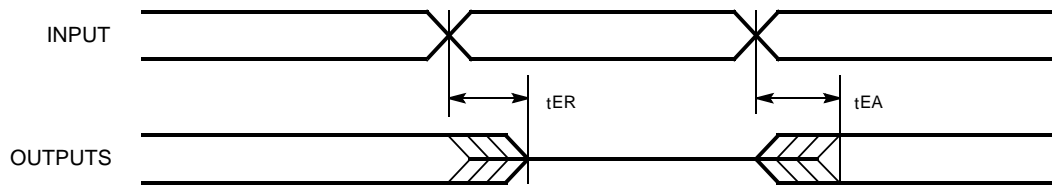
7c371-18

Asynchronous Preset



7c371-19

Switching Waveforms (continued)

Output Enable/Disable


7c371-21

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
143	CY7C371-143AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
110	CY7C371-110AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371-110JC	J67	44-Lead Plastic Leaded Chip Carrier	
83	CY7C371-83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371L-83AC	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371-83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L-83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371-83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371L-83AI	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371-83JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L-83JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371-83YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
66	CY7C371-66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371L-66AC	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371-66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L-66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371-66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371L-66AI	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371-66JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L-66JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371-66YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military

Shaded areas contain preliminary information.

MILITARY SPECIFICATIONS Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

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LOG/iC is a trademark of Isdata Corporation.

CUPL is a trademark of Logical Devices Incorporated.

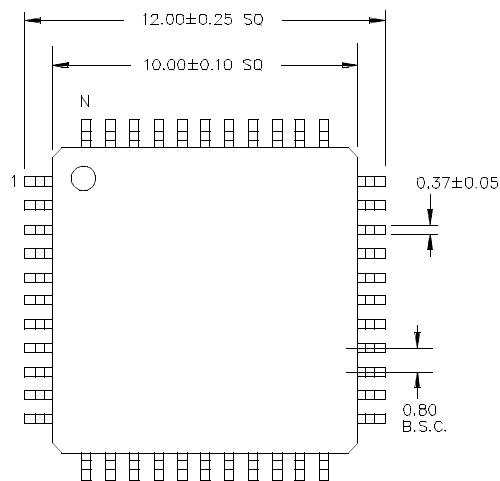
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Switching Characteristics

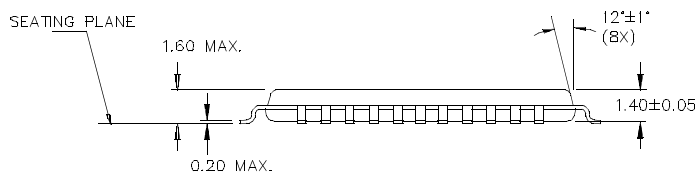
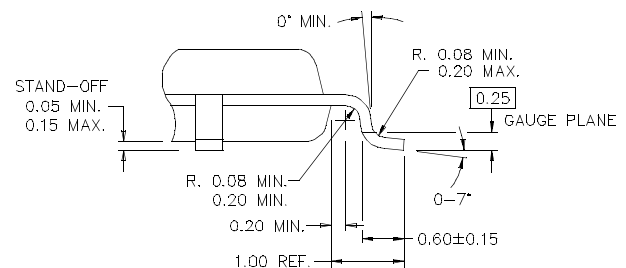
Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

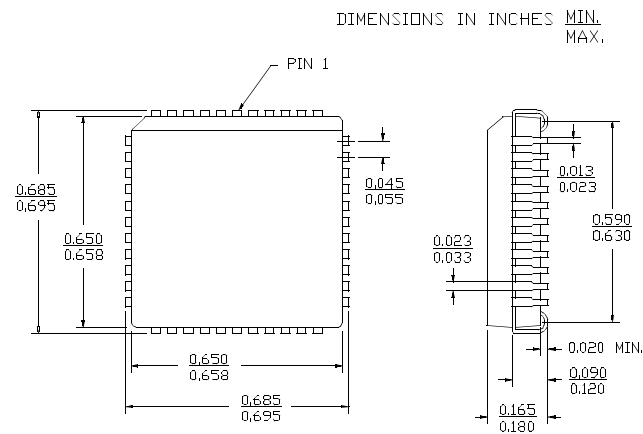
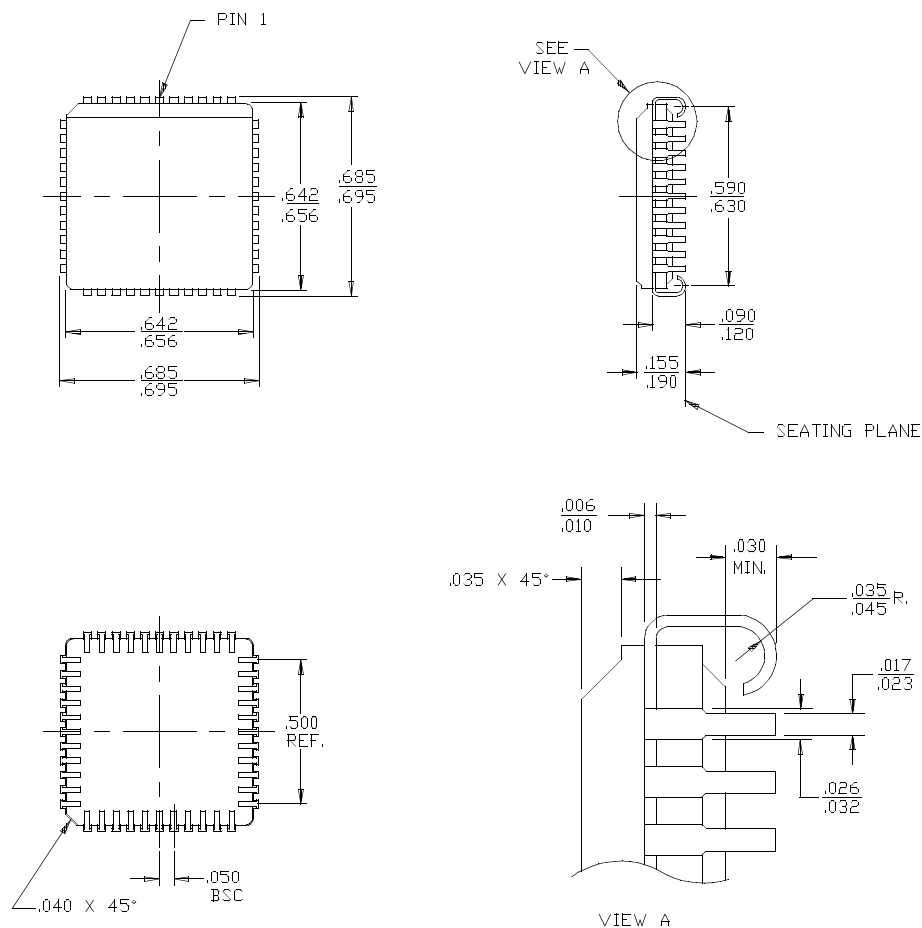
Package Diagrams

44-Lead Thin Plastic Quad Flat Pack A44



DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.



Package Diagrams (continued)
44-Lead Plastic Leaded Chip Carrier J67

44-Pin Ceramic Leaded Chip Carrier Y67


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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106319	04/27/01	SZV	Change from Spec number: 38-00212 to 38-03019