For new designs see CY7C373i

CY7C373

UltraLogic™ 64-Macrocell Flash CPLD

Features

- **64 macrocells in four logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - **—f_{MAX} = 125 MHz**
  - **—t_{PD} = 10 ns**
  - **—t_S = 5.5 ns**
  - **—t_{CO} = 6.5 ns**
- **Electrically alterable Flash technology**
- **Available in 84-pin PLCC and 100-pin TQFP packages**
- **Pin compatible with the CY7C374**

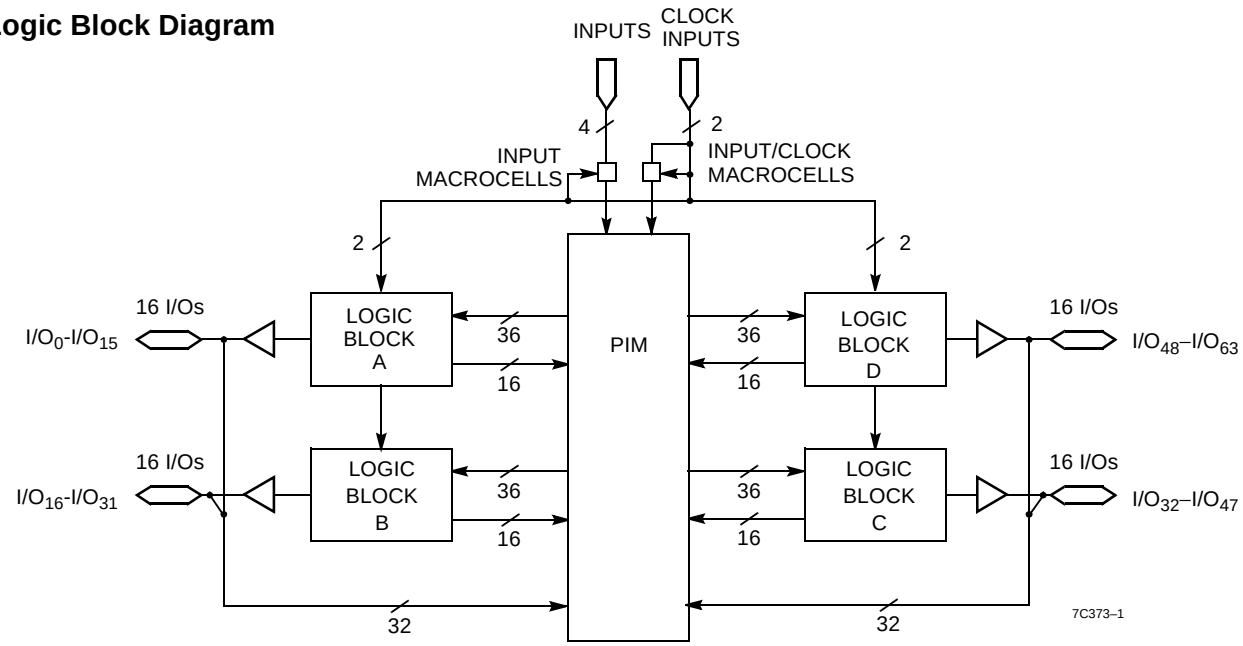
Functional Description

The CY7C373 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C373 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

The 64 macrocells in the CY7C373 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Logic Block Diagram



Selection Guide

		7C373-125	7C373-100	7C373-83	7C373-66	7C373L-66
Maximum Propagation Delay (ns)		10	12	15	20	20
Minimum Set-up, t_S (ns)		5.5	6	8	10	10
Maximum Clock to Output, t_{CO} (ns)		6.5	6.5	8	10	10
Maximum Supply Current, I_{CC} (mA)	Commercial	280	250	250	250	125
	Industrial			300	300	

Shaded area contains preliminary information.

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