CY7C375

UltraLogic™ 128-Macrocell Flash CPLD

Features

- **128 macrocells in eight logic blocks**
- **128 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - **—f_{MAX} = 100 MHz**
  - **—t_{PD} = 12 ns**
  - **—t_S = 6 ns**
  - **—t_{CO} = 7 ns**
- **Electrically alterable FLASH technology**
- **Available in 160-pin TQFP, CQFP, and PGA packages**

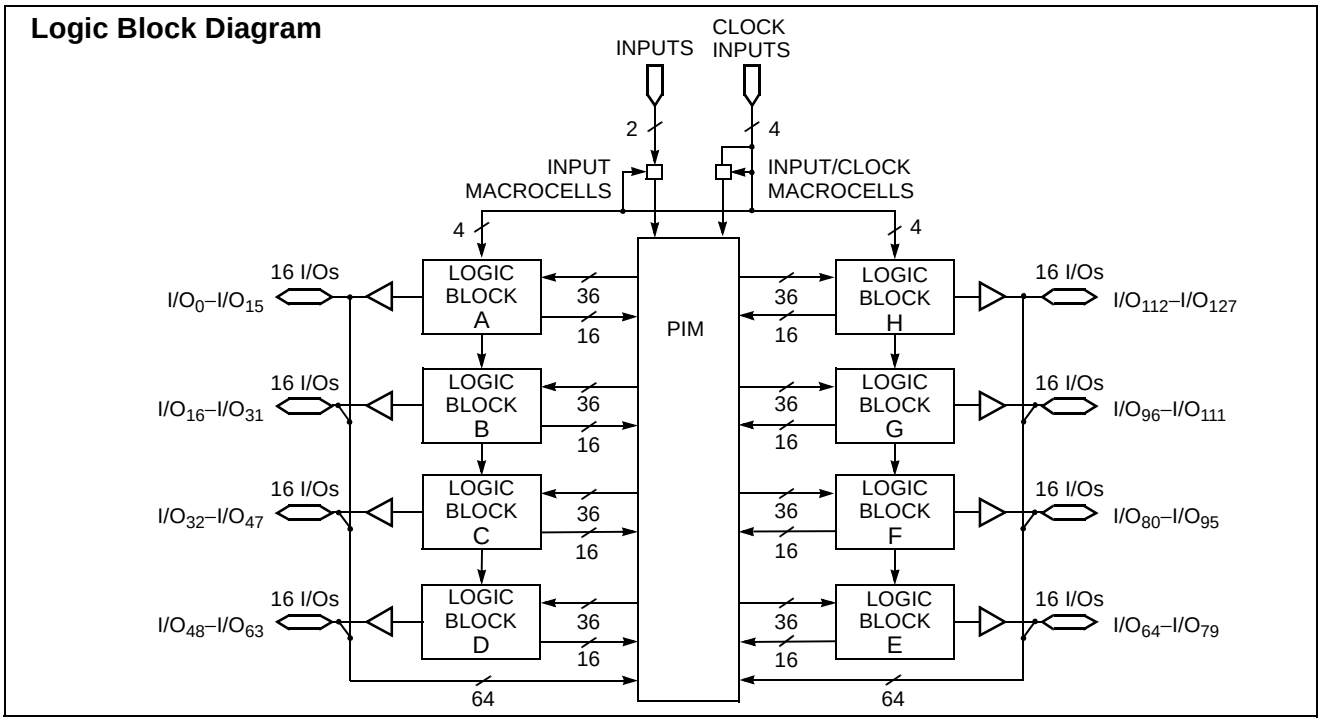
Functional Description

The CY7C375 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C375 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 128 macrocells in the CY7C375 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Logic Block Diagram



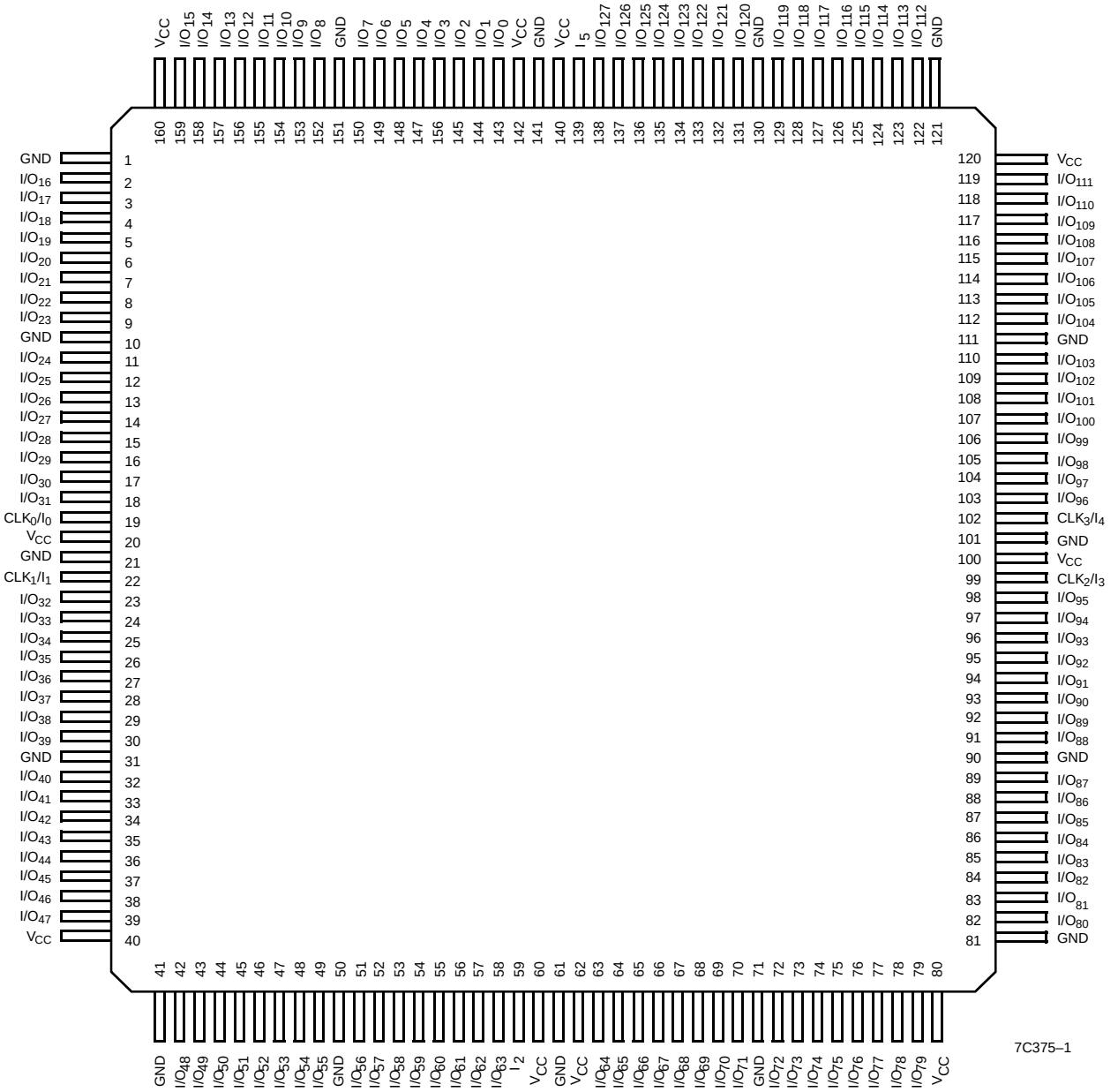
Selection Guide

		7C375-100	7C375-83	7C375-66	7C375L-66
Maximum Propagation Delay, t_{PD} (ns)		12	15	20	20
Minimum Set-Up, t_S (ns)		6	8	10	10
Maximum Clock to Output, $t_{CO\ (ns)}$		7	8	10	10
Maximum Supply Current, I_{CC} (mA)	Commercial	330	300	300	150
	Military/Industrial		370	370	

Pin Configurations

TQFP/CQFP

Top View



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Functional Description (continued)

Like all members of the FLASH370 family, the CY7C375 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 128 I/O pins on the CY7C375. In addition, there are two dedicated inputs and four input/clock pins.

Finally, the CY7C375 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C375 remain the same.

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C375 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the

Pin Configurations

PGA
BottomView

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	I/O_{109}	I/O_{112}	I/O_{115}	I/O_{118}	I/O_{121}	I/O_{123}	I/O_{126}	I/O_{127}	I/O_0	I/O_3	I/O_5	I/O_7	I/O_{10}	I/O_{11}	I/O_{14}
P	I/O_{106}	I/O_{110}	I/O_{113}	I/O_{116}	I/O_{119}	I/O_{122}	I/O_{125}	GND	I/O_1	I/O_4	I/O_6	I/O_9	I/O_{13}	I/O_{15}	I/O_{16}
N	I/O_{105}	I/O_{108}	I/O_{111}	I/O_{114}	I/O_{117}	I/O_{120}	I/O_{124}	I_5	I/O_2	GND	I/O_8	I/O_{12}	GND	I/O_{17}	I/O_{19}
M	I/O_{102}	I/O_{104}	I/O_{107}	V_{CC}			V_{CC}	GND	V_{CC}			GND	I/O_{18}	I/O_{20}	I/O_{22}
L	I/O_{100}	I/O_{101}	I/O_{103}										I/O_{21}	I/O_{23}	I/O_{25}
K	I/O_{98}	I/O_{99}	GND										I/O_{24}	I/O_{26}	I/O_{27}
J	I/O_{96}	I/O_{97}	CLK_3 /I_4	V_{CC}								V_{CC}	I/O_{28}	I/O_{29}	I/O_{30}
H	I/O_{95}	GND	CLK_2 /I_3	GND								GND	CLK_0 /I_0	GND	I/O_{31}
G	I/O_{94}	I/O_{93}	I/O_{92}	V_{CC}								V_{CC}	CLK_1 /I_1	I/O_{33}	I/O_{32}
F	I/O_{91}	I/O_{90}	I/O_{88}										GND	I/O_{35}	I/O_{34}
E	I/O_{89}	I/O_{87}	I/O_{85}										I/O_{39}	I/O_{37}	I/O_{36}
D	I/O_{86}	I/O_{84}	I/O_{82}	GND			V_{CC}	GND	V_{CC}			V_{CC}	I/O_{43}	I/O_{40}	I/O_{38}
C	I/O_{83}	I/O_{81}	GND	I/O_{76}	I/O_{72}	GND	I/O_{66}	I_2	I/O_{60}	I/O_{56}	I/O_{53}	I/O_{50}	I/O_{47}	I/O_{44}	I/O_{41}
B	I/O_{80}	I/O_{79}	I/O_{77}	I/O_{73}	I/O_{70}	I/O_{68}	I/O_{65}	GND	I/O_{61}	I/O_{58}	I/O_{55}	I/O_{52}	I/O_{49}	I/O_{46}	I/O_{42}
A	I/O_{78}	I/O_{75}	I/O_{74}	I/O_{71}	I/O_{69}	I/O_{67}	I/O_{64}	I/O_{63}	I/O_{62}	I/O_{59}	I/O_{57}	I/O_{54}	I/O_{51}	I/O_{48}	I/O_{45}

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product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows

Functional Description (continued)

for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C375 has a separate I/O pin associated with it. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and four global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C375 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

A feature called bus-hold has been added to all FLASH370 I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's per-

formance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Development Tools

Development software for the CY7C375 is available from Cypress's *Warp*™ software packages. Both of these products are based on IEEE standard 1076/1164 VHDL. Cypress is also supported by a number of third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please refer to the third-party tool support data sheets for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	–40°C to +85°C	5V ± 10%
Military[1]	–55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)		2.4		V
			I_{OH} = –2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[3]			2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[3]			–0.5	0.8	V
I_{IX}	Input Load Current	V_I = Internal GND, V_I = V_{CC}			–10	+10	µA
I_{OZ}	Output Leakage Current	V_o = Internal GND, V_o = V_{CC}			–50	+50	µA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = 0.5V			–30	–160	mA
I_{CC}	Power Supply Current[6]	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 mHz, V_{IN} = GND, V_{CC}		Com'l		330	mA
				Com'l "L" –66		150	mA
				Mil/Ind		370	mA

Shaded area contains preliminary information.

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$[7, 8]	Input Capacitance	V_{IN} = 5.0V at f=1 MHz	10	pF

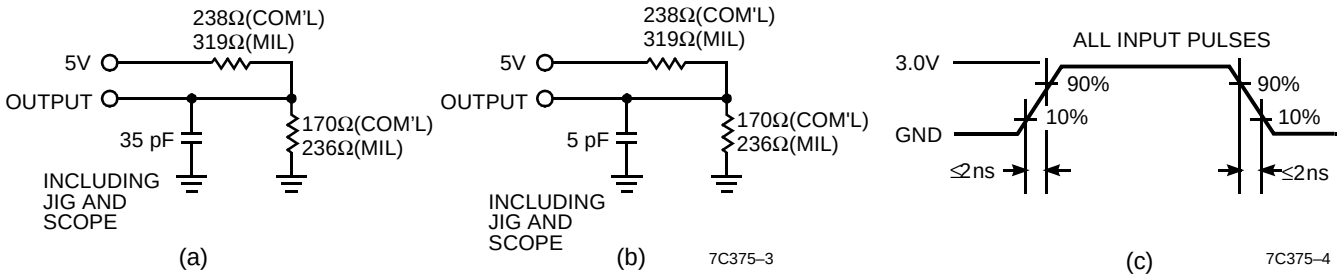
Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Measured with 16-bit counter programmed into each logic block.
7. $C_{I/O}$ for the CPGA and CQFP package is 15 pF Max.
8. $C_{I/O}$ for I_5 is 15 pF Max.

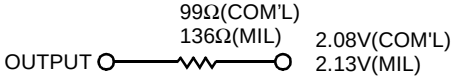
Endurance Characteristics[5]

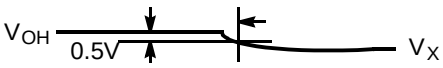
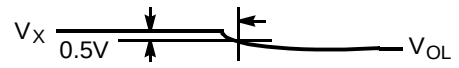
Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[9]	V_X	Output Waveform Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{thc}	

(d) Test Waveforms

Switching Characteristics Over the Operating Range[10]

Parameter	Description	7C375-100		7C375-83		7C375L-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time[5]	3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[5]	3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns

Notes:

9. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
10. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[10]

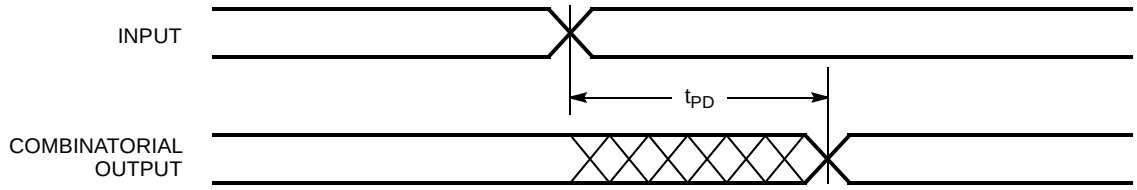
		7C375-100		7C375-83		7C375L-66		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		7		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	6		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	100		83		66		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	143		125		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	76.9		62.5		50		MHz
t_{OH}-t_{IH} 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[5, 11]	0		0		0		ns
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	10		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	100		83.3		66.6		MHz
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width[5]	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[5]	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width[5]	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[5]	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns

Note:

11. This specification is intended to guarantee interface compatibility of the other members of the CY7C370 family with the CY7C375. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Waveforms

Combinatorial Output



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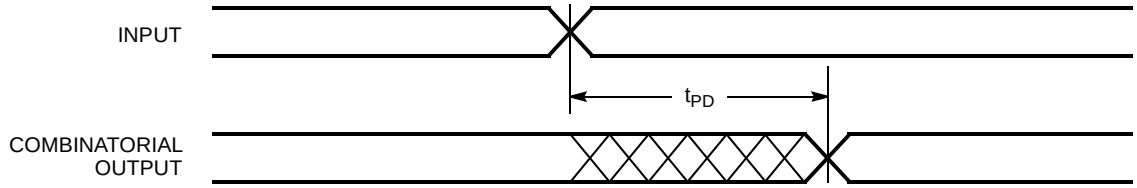
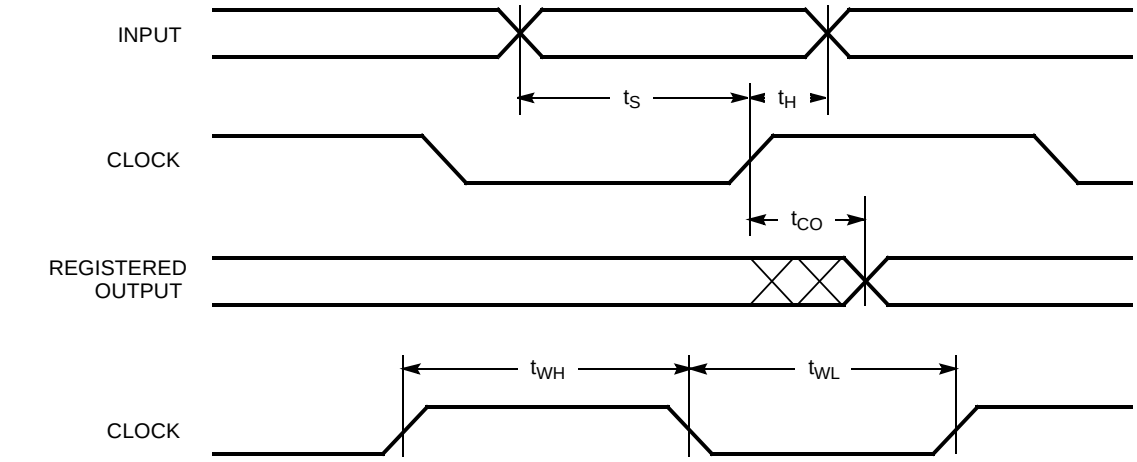
Combinatorial Output



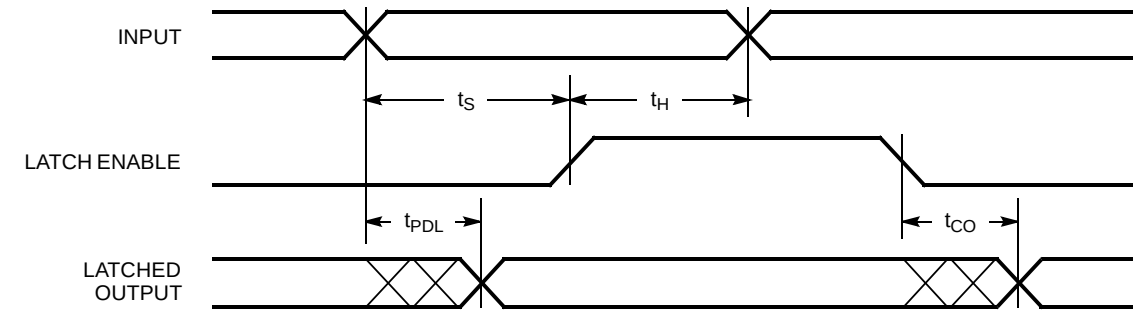
7C375–6

Registered Output



7C375–7

Latched Output



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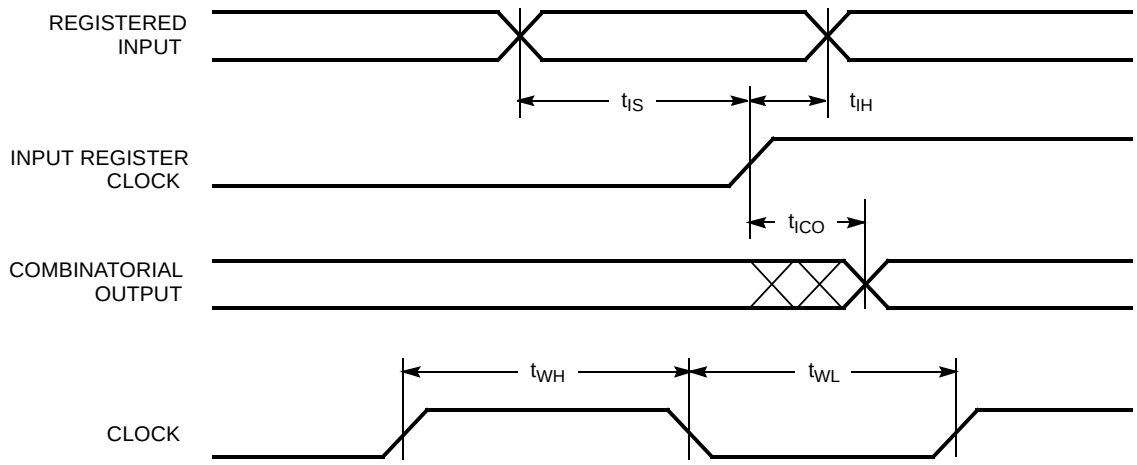
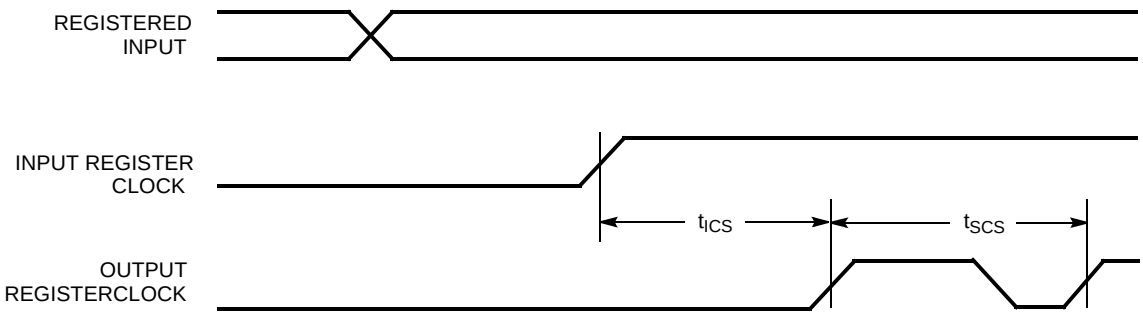
Switching Waveforms (continued)

Registered Input



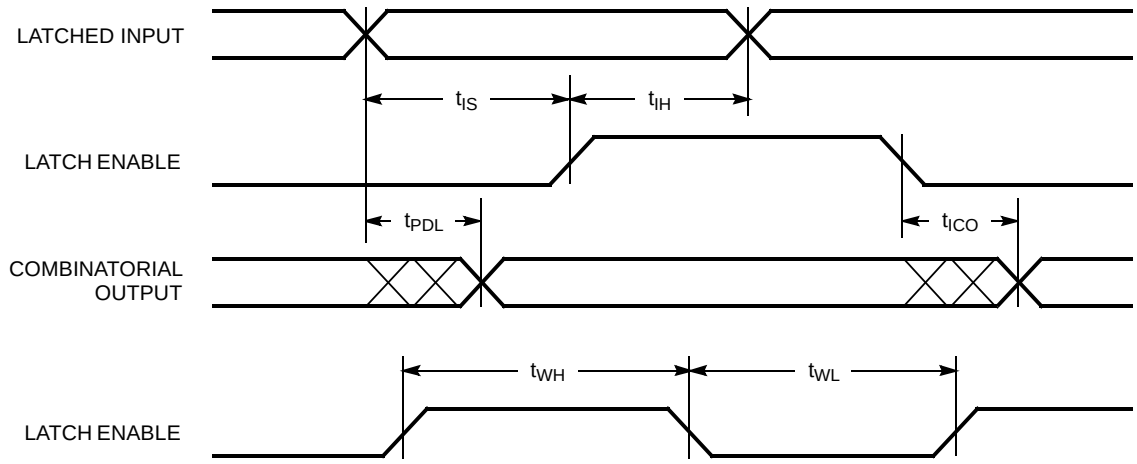
7C375–9

Clock to Clock



7C375–10

Latched Input



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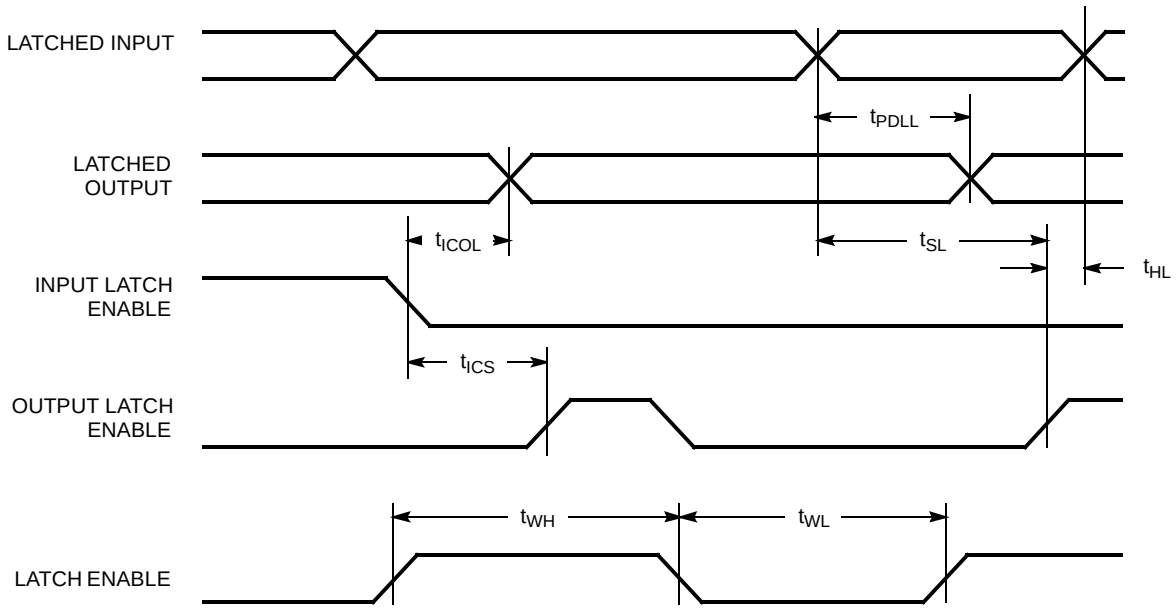
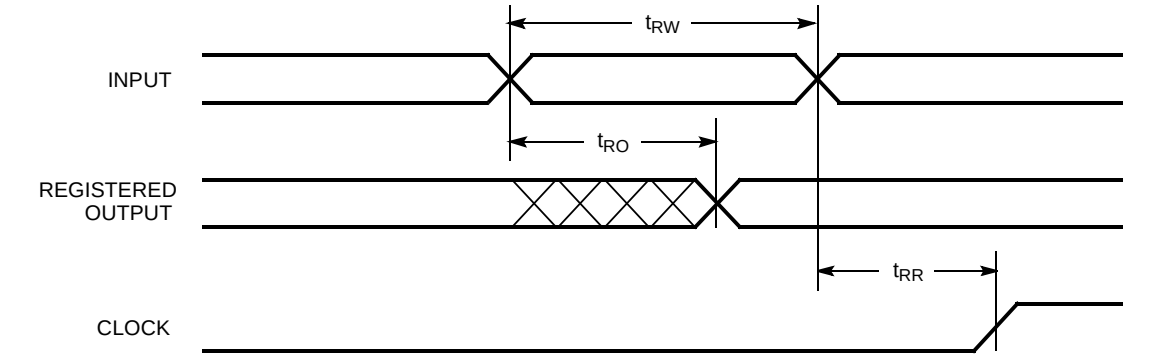
Switching Waveforms (continued)

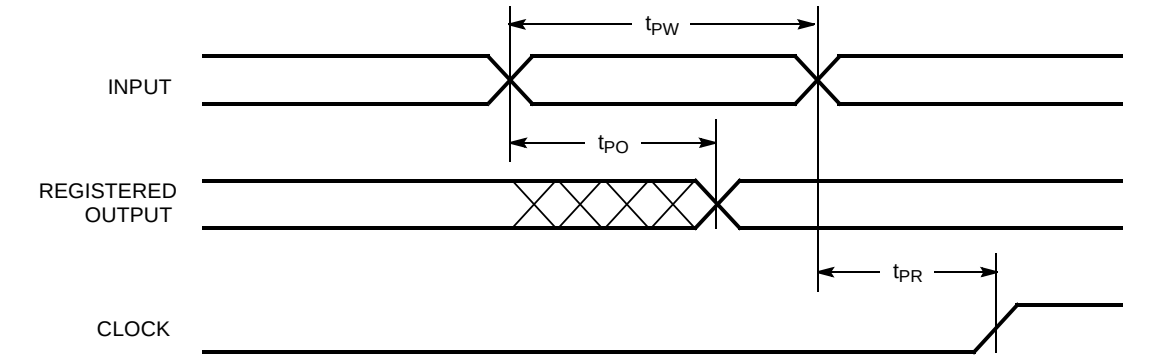
Latched Input and Output



Asynchronous Reset

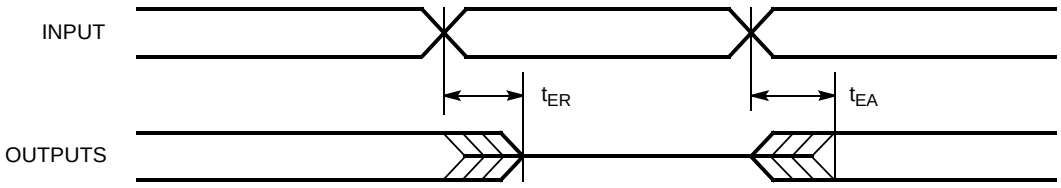


Asynchronous Preset



Switching Waveforms (continued)

Output Enable/Disable



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Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C375-100AC	A160	160-Lead Thin Quad Flatpack	Commercial
83	CY7C375-83AC	A160	160-Lead Thin Quad Flatpack	Commercial
	CY7C375-83AI	A160	160-Lead Thin Quad Flatpack	Industrial
	CY7C375-83GMB	G160	160-Pin Grid Array	Military
	CY7C375-83UMB	U162	160-Pin Ceramic Quad Flatpack[12]	
66	CY7C375-66AC	A160	160-Lead Thin Quad Flatpack	Commercial
	CY7C375-66AI	A160	160-Lead Thin Quad Flatpack	Industrial
	CY7C375-66GMB	G160	160-Pin Grid Array	Military
	CY7C375-66UMB	U162	160-Pin Ceramic Quad Flatpack[12]	
66	CY7C375L-66AC	A160	160-Lead Thin Quad Flatpack	Commercial

Note:

12. Available as custom trim and form version. Contact local Cypress office for package information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

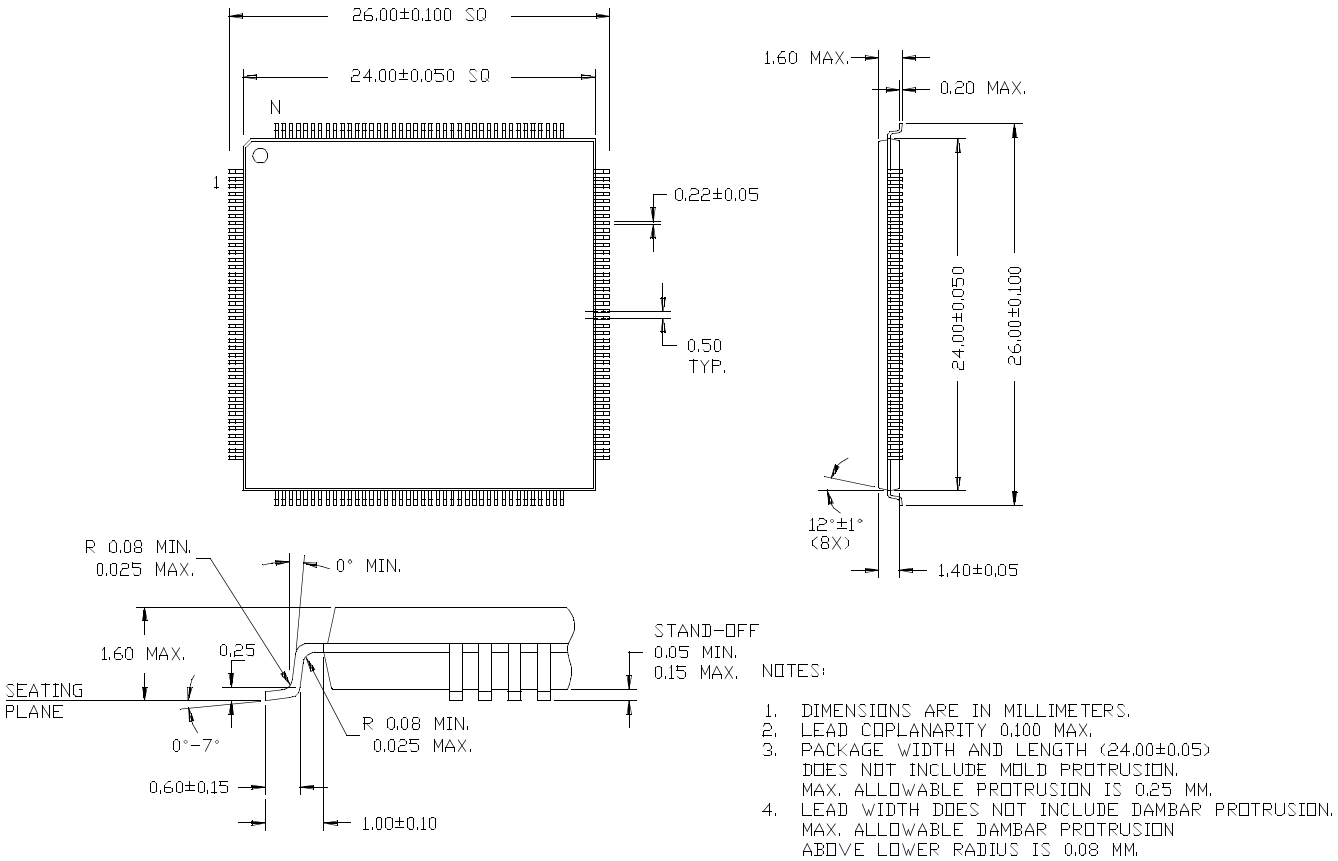
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

Package Diagrams

160-Lead Thin Quad Flat Pack (TQFP) A160

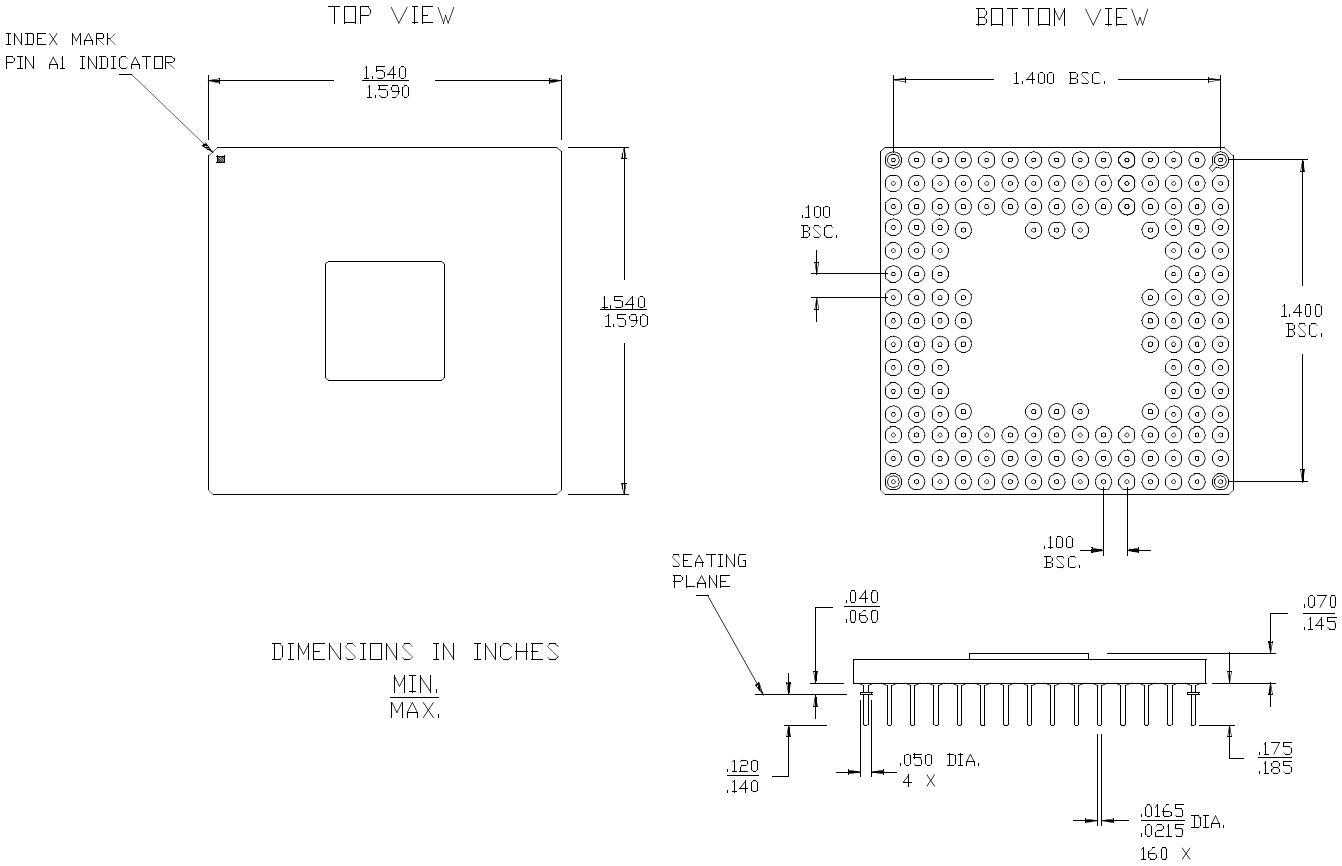


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH AND LENGTH (24.00±0.05) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

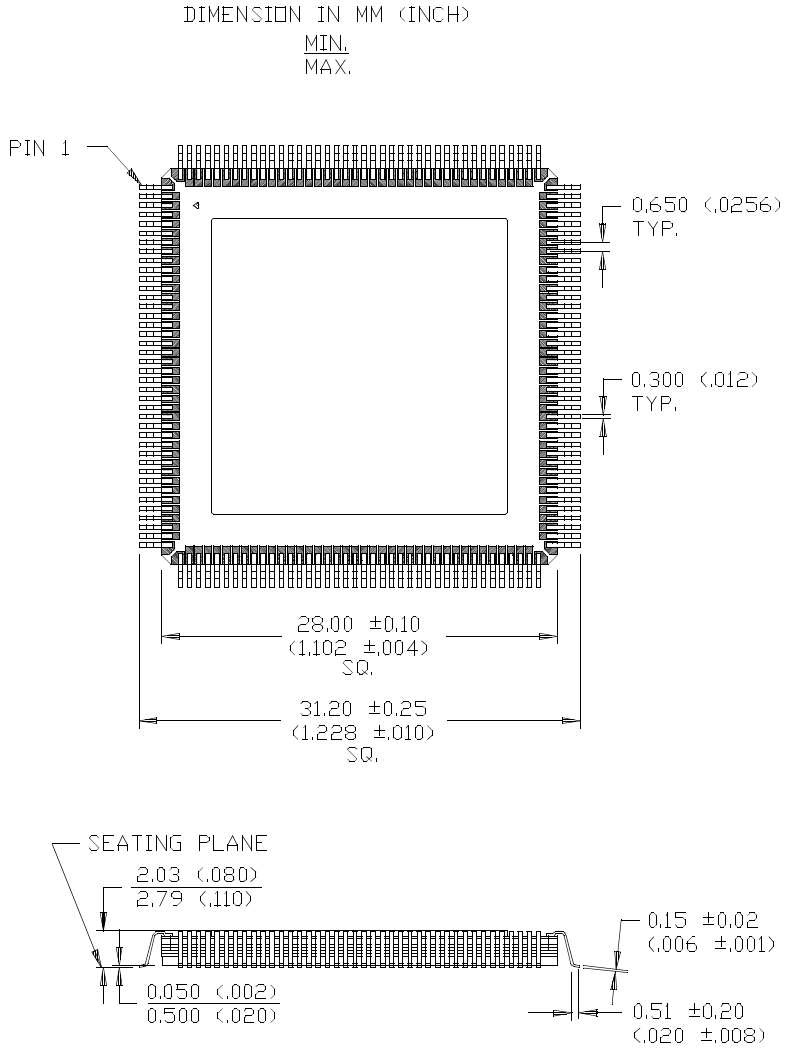
Package Diagrams (continued)

160-Pin PGA G160



Package Diagrams (continued)

160-Lead Ceramic Quad Flatpack (Cavity Up) U162



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**	106328	06/15/01	SZV	Change from Spec#: 38-00217 to 38-03024