Configuring Delta39K™/Quantum38K™ CPLDs

Overview

This application note discusses the configuration interfaces, modes, and processes of the Delta39K™ and Quantum38K™ CPLDs and includes examples on setting up the devices.

Each member of the Delta39K family is available in volatile and Self-Boot™ packages. An external CPLD boot EEPROM is used to store the configuration data for the volatile package while an internal Flash memory is embedded in the Self-Boot package. Programming is defined as the loading of a user's design into either the external CPLD boot EEPROM or the internal Flash device. Configuration, on the other hand, is the loading of a user's design into the volatile die.

The external EEPROM configures the Delta39K through the Serial Configuration port. Both the volatile and Self-Boot packages can also be configured through the JTAG port. The configuration process with the internal Flash is transparent to the user.

The Quantum38K family is architecturally similar to Delta39K but without some of the Delta39K's features. It is also only available in volatile packages. The configuration set-up and processes of the Quantum38K family are the same as those of the volatile Delta39K.

Configuration and Programming Paths

Delta39K devices can be configured in multiple ways (*Figure 1*). The bitstream can be sent through the JTAG port from a PC, through the Serial Configuration port from an external EEPROM, or through the Non-Volatile (NV) port from the internal Flash. For volatile Delta39K and Quantum38K, configuration through the internal Flash is obviously not available.

To program the internal Flash, the bitstream is sent from a PC through the JTAG port into the Delta39K, and is then passed on to the internal Flash though the NV port (*Figure 2*).

The configuration bitstream is in a compressed form when it is stored in an external EEPROM or in the internal Flash. The bitstream is then uncompressed by internal circuitry during configuration.

Configuration Interfaces

Delta39K/Quantum38K has three common configuration signals, a JTAG port, and a Configuration port. Delta39K also has the NV port to interface with the internal Flash. The three common configuration signals are MSEL, Reconfig, and Config_Done.

Common Configuration Signals

MSEL - *Input* - Selects the configuration mode when starting the configuration process. It will configure from the internal Flash when set to LOW/GND and from an external EEPROM when set to HIGH/V_{CCCNFG}. The MSEL level needs to be stable during the configuration process.

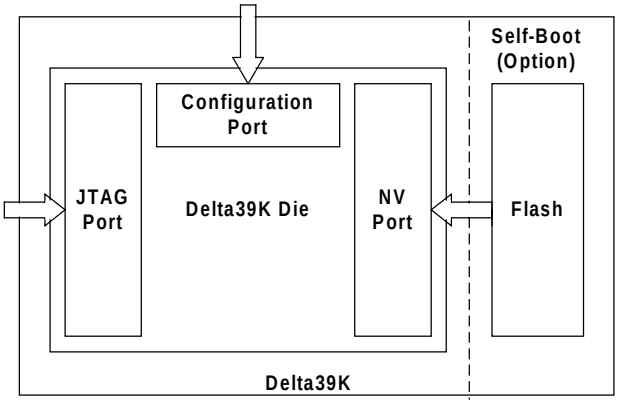

Figure 1. Configuration Paths into the Delta39K

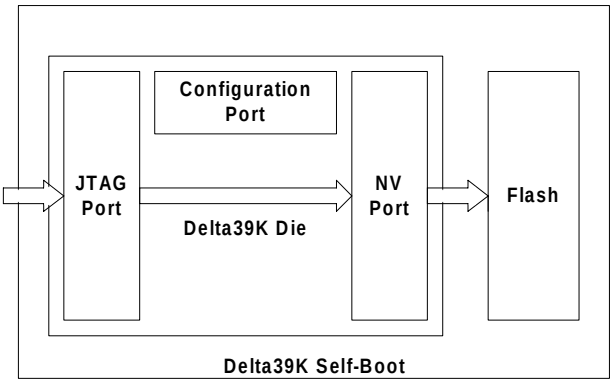

Figure 2. Programming Path into the internal Flash

Reconfig - *Input* - Initiates reconfiguration of the device when brought from logic level LOW to HIGH. When at a logic level LOW, it suppresses and resets the configuration process. Reconfig must be pulled HIGH for the device's logic to operate ("PAL mode"). The device will not attempt to configure unless Reconfig transitions from LOW to HIGH.

Config_DONE - *Output* - Signal is LOW during the configuration process and then switches to HIGH once the process is completed successfully. This is *not* an open-drain output.

JTAG Port

The JTAG port consists of four signals: TCK, TMS, TDI, and TDO. Data is shifted into the device through TDI and out of the device through TDO. TMS (Test Mode Select) and TCK (Test Clock) are used to control an internal state machine called the Test Access Port (TAP) Controller (Appendix D), which serves as the access point for boundary scan testing, device configuration/verification and non-volatile device pro-

gramming/verification. For more information on the TAP architecture, refer to IEEE Standard 1149.1, *IEEE Standard Test Access Port and Boundary-Scan Architecture.*

Configuration Port

Four signals, in addition to MSEL and Reconfig, are used to interface with an external EEPROM for configuring the Delta39K:

CCLK - *Output* - Internally generated configuration clock going to the external EEPROM.

CCE - *Output* - A LOW logic level signals the external EEPROM that the Delta39K/Quantum38K is ready to accept configuration data. This signal is used to start and stop serial data shifting into the device.

Reset - *Output* - A HIGH logic level resets the configuration address pointer in the external EEPROM.

DATA - *Input* - A one-bit configuration data input.

Non-Volatile (NV) Port

The NV port is a dedicated port used to interface with the internal Flash configuration memory. It is not directly accessible by the user, but it is indirectly accessible through the JTAG port of a Self-Boot Delta39K.

Power Supplies

There are six types of power supplies in Delta39K to allow independent and flexible configuration. They are V_{CC} (Core), V_{CCIO} (IO Cells), V_{CCPRG} (NV port and internal Flash), V_{CCCNFG} (Configuration port), V_{CCJTAG} (JTAG port), and V_{CCPLL} (PLL block). For PAL (Operation) mode power supply set-up, please refer to the Delta39K/Quantum38K family data sheet.

There is no required power-up sequence of these power supplies for successful configuration. However, all power supplies have to be up and stable before the device will start configuring. The power supplies are connected to the internal POR circuitry and trigger the POR operation when all power supplies reach at least 1.8V. Even when the design does not use the PLL feature of Delta39K, V_{CCPLL} will still need to be powered. The same rule applies to the other power supplies.

While V_{CCPRG} only needs to be at 1.8V for it to trigger the POR circuitry, it needs to be at 3.3V for successful operation of the internal Flash memory in Self-Boot Delta39K devices. For Delta39K and Quantum38K volatile devices, V_{CCCNFG} must be supplied by 3.3V. V_{CCJTAG} should be supplied according to the I/O interface of the JTAG port: 1.8V for LVCMOS18 operation, 2.5V for LVCMOS2 operation, 3.3V for LVCMOS/LVTTL operation. The I/O standard of the JTAG port is not “configurable” — it is effectively set by the supply voltage. If V_{CCJTAG} is 3.3V, use the C3ISR cable or the UltraISR cable. If V_{CCJTAG} is 1.8V or 2.5V, use the C3ISR cable.

Configuration Data Files

When compilation and fitting of a design to a Delta39K device is successful, *Warp*® generates a configuration data file in the project directory. The data file is easily recognized by the HEX extension.

The HEX file is compressed configuration data in Intel HEX format. It is used by the ISR software to program the internal Flash and/or configure the volatile die, and is used by the CPLD Boot PROM software to configure the external boot PROM.

For more information on how to use ISR software, please refer to the ISR-related application notes available at Cypress Semiconductor’s website (www.cypress.com).

For more information on how to program the external EEPROM, please refer to the application note “Programming CY3LV Configuration EEPROMs.”

Table 1 shows the uncompressed configuration bitstream length and the corresponding recommended EEPROM. Note that in all cases the Atmel equivalent part (AT17LV) may be used instead of the Cypress part (CY3LV).

Table 1. Uncompressed Configuration Bitstream Length

Device	Bitstream Length	Memory Device Recommendation
Delta39K15 Quantum38K15	225,824[1]	CY3LV256/512
Delta39K30 Quantum38K30	463,328[1]	CY3LV512
Delta39K50 Quantum38K50	714,080[1]	CY3LV512/010
Delta39K100 Quantum38K100	1,497,296	CY3LV010/020
Delta39K165	3,268,640	CY3LV020
Delta39K200	3,268,640	CY3LV020

Intel HEX Format

The general record format in an Intel HEX file is shown in *Table 3*. Each byte is represented by two ASCII characters except the RECORD MARK, which is always represented by a colon.

RECORD MARK ':'	RECLEN	LOAD OFFSET	RECTYPE	INFO/ DATA	CHECKSUM
1 char	2 chars	4 chars	2 chars	2n chars	2 chars
	1 byte	2 bytes	1 byte	n bytes	1 byte

Figure 3. General Record Format

RECORD MARK - Always a colon (:), it signals the start of a record line.

RECLEN - The number of bytes, between 0 and 255 bytes, contained in the INFO/DATA field.

LOAD OFFSET - 16-bit offset address for the data byte(s) in the INFO/DATA field.

Note:
1. Numbers are approximate

RECTYPE - Record Type: 00 for DATA, 01 for END OF FILE.

DATA - Contains a pair of ASCII characters to represent each byte of data specified in the RECLEN field.

CHECKSUM - The 2's Complement of the 8-bit addition of the bytes in RECLEN, LOAD OFFSET, RECTYPE, and INFO/DATA.

Example

Below is an example of an Intel HEX file that contains two sets of data. The first set has 4 bytes of data (0x05, 0xFA, 0x39, 0x4D) and the second set has 2 bytes of data (0x55, 0xAA).

:0400000005FA394D77

:0200040055AAFB

:00000001FF

How To Calculate The Checksum

Add 1 byte of data at a time and negate the end result to give the final checksum value. Below is the calculation for the first data set of the above example.

0x04 + 0x00 + 0x00 + 0x00 = 0x04

0x04 + 0x05 = 0x09

0x09 + 0xFA = 0x03

0x03 + 0x39 = 0x3C

0x3C + 0x4D = 0x89

–(0x89) = 0x77

Compressed Configuration Bitstream Format

The compressed bitstream format follows the following sequence:

1. DTCB (1 Byte of data)
2. Data (1024 Bytes of data)
3. CRC (2 Bytes of data)

(Repeat 2 and 3 until all configuration bits are covered)

When the configuration bitstream does not fully utilize the final 1024 bytes of data, all data bits after the last configuration bit will be set to 0.

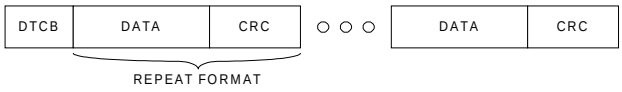

Figure 4. Compressed Bitstream Format

Debug and Test Configuration Byte (DTCB)

The DTCB contains internal configuration settings as well as the configuration clock wait state value. The default value of the bits should not be changed except bits 4, 5, and 6 that users may manually modify. Bit 6 is the Even Parity bit of bit 0 through 6.

Configuration Time

The total time that Delta39K and Quantum38K devices take to be fully configured includes the JTAG TAP controller and-decompression overhead. The devices have an internal oscillator that generates the CCLK signal used both in the configuration process through the internal Flash and external EEPROM. CCLK operates between 2.02 MHz with 3 wait states and 8.06 MHz with 0 wait states. *Table 3* shows the approximate configuration times of CY39100 and CY38100 devices. Future versions of *Warp* will provide the ability to specify the wait state configurations and directly control the configuration clock.

Table 2. Debug and Test Configuration Byte

Bit	Default	User	Description
7(MSB)	0	N	Reserved
6	0	Y	Even Parity Check
5	0	Y	Wait State 1
4	0	Y	Wait State 0
3	0	N	Reserved
2	0	N	Enables Ring Oscillator
1	0	N	Reserved
0(LSB)	0	N	Enables CRC

Table 3. Configuration Time

Interface Ports	Wait State (DTCB[5:4])	CCLK (MHz)	Approximate Config Time (CY39100, CY38100)
Serial Configuration and Non-Volatile	0	8.06	200 ms
	1	4.03	384 ms
	2	2.69	568 ms
	3	2.02	756 ms
JTAG (ISR S/W)	N/A	~0.6	8 sec.

To calculate the approximate configuration time of the other devices, use the following formula:

Config Time = (Total Config Bits/CCLK) * 1.08 Eq. 1

Programming Time

ISR takes approximately 60 seconds to program the internal Flash. This programming time also varies depending on the PC. For the CPLD Boot PROM's programming time, please refer to the CY3LV programming application note.

Configuration Sequence

Powering-up the system will initiate the configuration process when the Reconfig input is driven HIGH. After the system is powered-up, there are two ways to initiate the Delta39K/Quantum38K configuration process:

1. ISR instructions through the JTAG port
2. Toggle Reconfig

Toggling the Reconfig signal will only work when the JTAG TAP Controller (Appendix C) is in the Test-Logic-Reset state. So, ISR must first complete its operation. If ISR issues an instruction anytime during the configuration process, the configuration process will cease and execute the latest JTAG instruction.

If MSEL is LOW, the device will go into the NV Configure mode. If MSEL is HIGH, the device will select the Master Serial mode. Config_Done will be LOW during configuration and will switch to HIGH when the process is complete.

If a CRC error is encountered, the internal configuration circuitry will restart the configuration process immediately.

NV Configure Mode

NV Configure loads configuration bits from the internal Flash device to the memory cells of the Self-Boot Delta39K device. This is done via the NV port. The configuration process is transparent to the user.

Master Serial Mode

This mode loads configuration bits from an external EEPROM to the Delta39K or Quantum38K device through the Configuration port. To stop the configuration process, hold the Reconfig signal LOW. To start the configuration process, toggle the Reconfig signal from LOW to HIGH. The clock signal for the external EEPROM and the internal circuitry is generated by the Delta39K or Quantum38K and is output as the CCLK signal. After receiving the rising edge on Reconfig, the device will set the Config_Done, CCE and Reset signals to LOW. It will then activate the CCLK. After all configuration data have been shifted in, the device will deactivate the CCLK and set CCE, Reset, and Config_Done High.

Hardware Setup[2]

The hardware set-ups described below apply to CY39100V208B and all other Delta39K/Quantum38K devices.

Volatile

For the volatile package, use a pull-up resistor to connect the Ready signal of the EEPROM to V_{CCCNFG} and a capacitor to GND (*Figure 5*). You can also connect a separate 10-pin header to allow the CPLD Boot PROM to be reprogrammed with the CPLD Boot PROM Programming kit, CYDH2200E. The external Boot PROM, such as the CY3LV, should be set as a Slave since Delta39K generates the CCLK signal. The programmable RESET option of the CY3LV needs to be set such that logic HIGH resets the Boot PROM.

During power-on reset, the READY pin of the Boot PROM will send out a LOW signal to the Reconfig pin of the Delta39K/Quantum38K device. This will hold the CPLD in a reset state and prevent it from attempting to configure. After the power supplies have met the power-on reset requirements described in the section “Power Supplies” above, the READY pin will be three-stated by the Boot PROM. The 4.7-kΩ pull-up resistor will bring the READY net to a logic high once the 1 µF capacitor is charged. The diode in *Figure 5* prevents any external signal (during normal operation or power-up) that drives the Reconfig line LOW from also activating the $\overline{\text{SER\_EN}}$ input of the CY3LV Boot PROM.

Pin 10 of the CPLD Boot PROM ISP connector is connected to the programmer through a standard 10-pin header. Mechanically, this is the same header that is used for the ISR connection to the Delta39K/Quantum38K CPLD. The “programmer” side of the cable has pin 10 grounded. This forces both $\overline{\text{SER\_EN}}$ and the Reconfig pin to be in a logic LOW state when the programmer cable is connected to the ISP header. This will turn on the programming mode of the CPLD Boot PROM and hold the Delta39K/Quantum38K device in reset. That is, the logic inside the Delta39K/Quantum38K device will not function (the device will not be in “PAL” mode) while the Boot EEPROM programming cable is connected to the header. After the data is programmed into the Boot PROM, removing the Boot PROM programming cable will cause $\overline{\text{SER\_EN}}$ to go HIGH due to the pull-up resistor on $\overline{\text{SER\_EN}}$. Provided the Boot PROM is ready (i.e., the READY output of the Boot-PROM is three-stated), the pull-up resistor on the Reconfig net will allow the Reconfig signal to be pulled HIGH, causing the Delta39K/Quantum38K device to start configuration.

Note:
2. For the hardware setup for CY39100V208 and CY39100V208A devices, please refer to Appendix E.

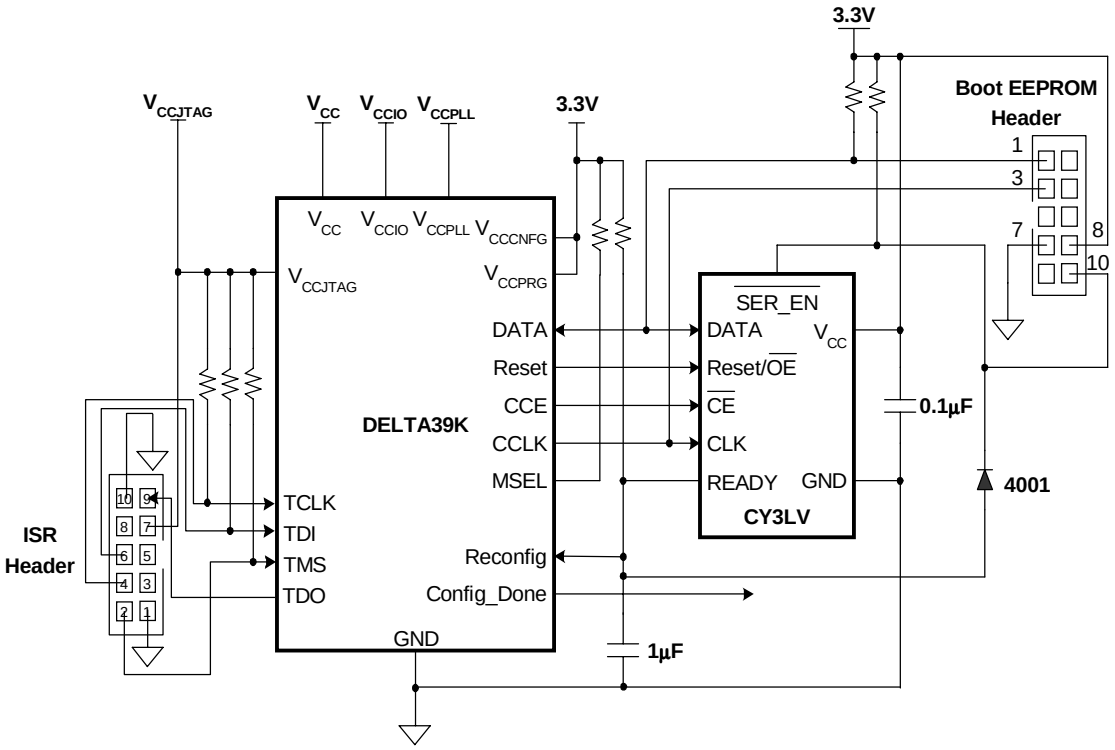

Figure 5. Volatile Delta39K Hardware Setup

Self-Boot

In the Self-Boot device, the MSEL signal can be connected directly to GND (*Figure 6*). This will select the internal Flash memory as the configuration source. The DATA pin should be pulled HIGH or LOW and the CCLK, CCE, and Reset pins can be left unconnected. If an external EEPROM is to be used with a Self-Boot part as a configuration source, set up the connection the same way as in the volatile device hardware set-up.

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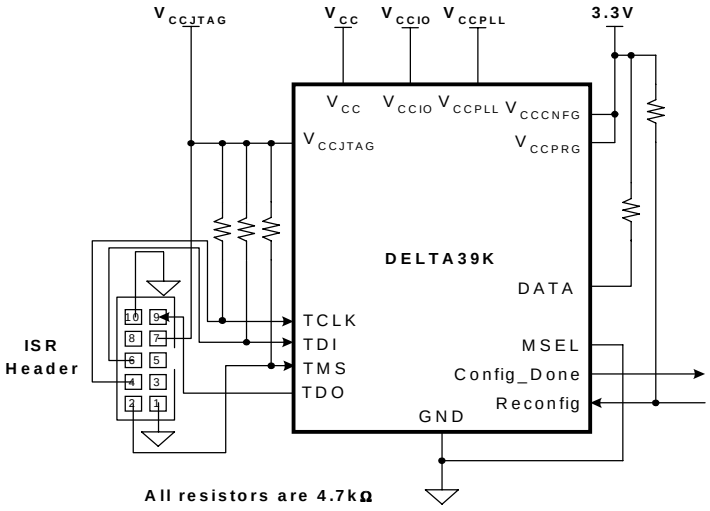


Figure 6. Self-Boot Delta39K Hardware Set-up (including CY39100V388 and CY39100V388A)

APPENDIX A - Timing Diagrams and Parameters

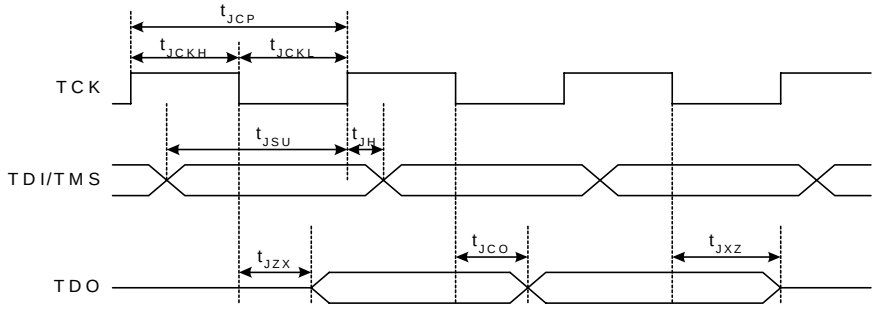


Figure 7. JTAG Timing Diagram

Table 4. JTAG Timing Parameters (Max. operating frequency at 20 MHz)

Parameter	Definition	Min.	Max.	Unit
t_{JCKH}	TCK Clock High Time	20		ns
t_{JCKL}	TCK Clock Low Time	20		ns
t_{JCP}	TCK Clock Period	50		ns
t_{JSU}	JTAG Port Set-up Time (TDI/TMS)	10		ns
t_{JH}	JTAG Port Hold Time (TDI/TMS)	10		ns
t_{JCO}	JTAG Port Clock to Output (TDO)		20	ns
t_{JXZ}	JTAG Port Valid Output to High Impedance (TDO)		20	ns
t_{JZX}	JTAG Port High Impedance to Valid Output (TDO)		20	ns

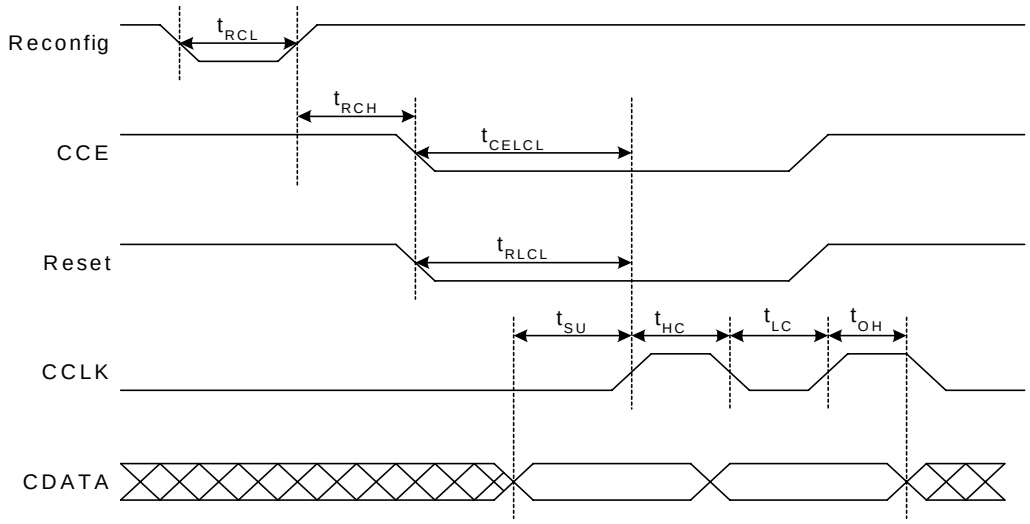
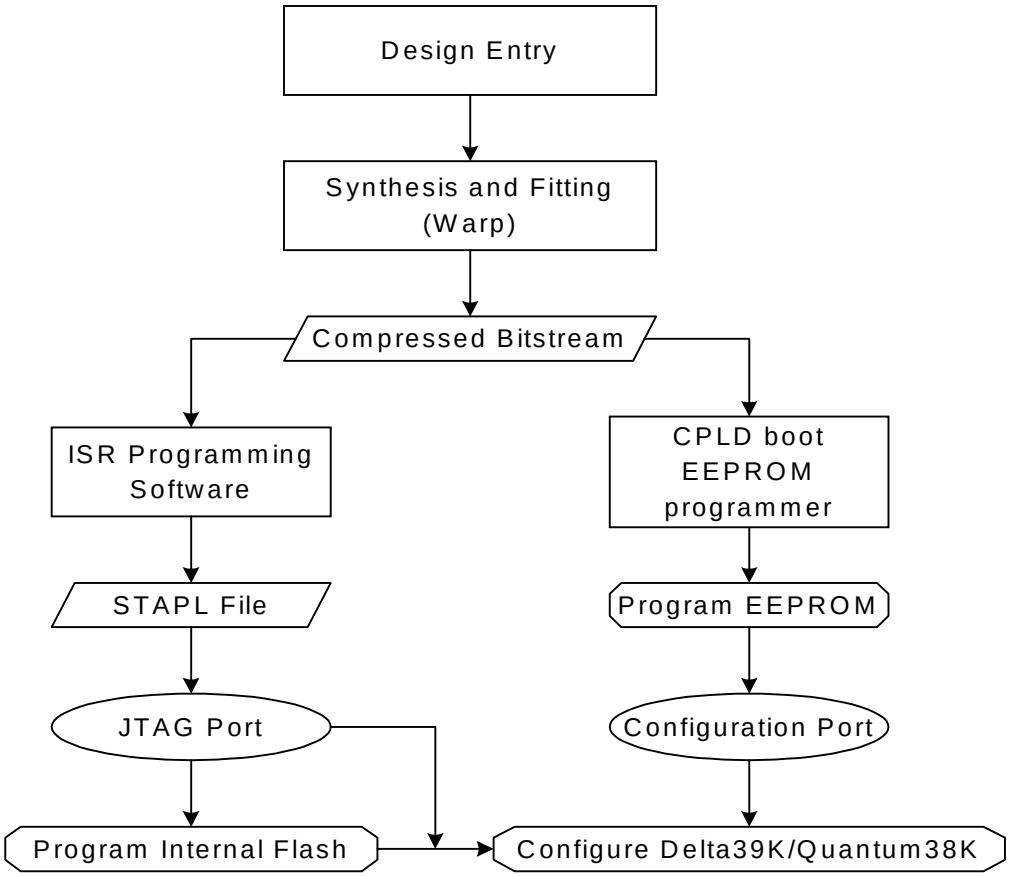


Figure 8. Configuration Port (Master Serial) Timing Diagram

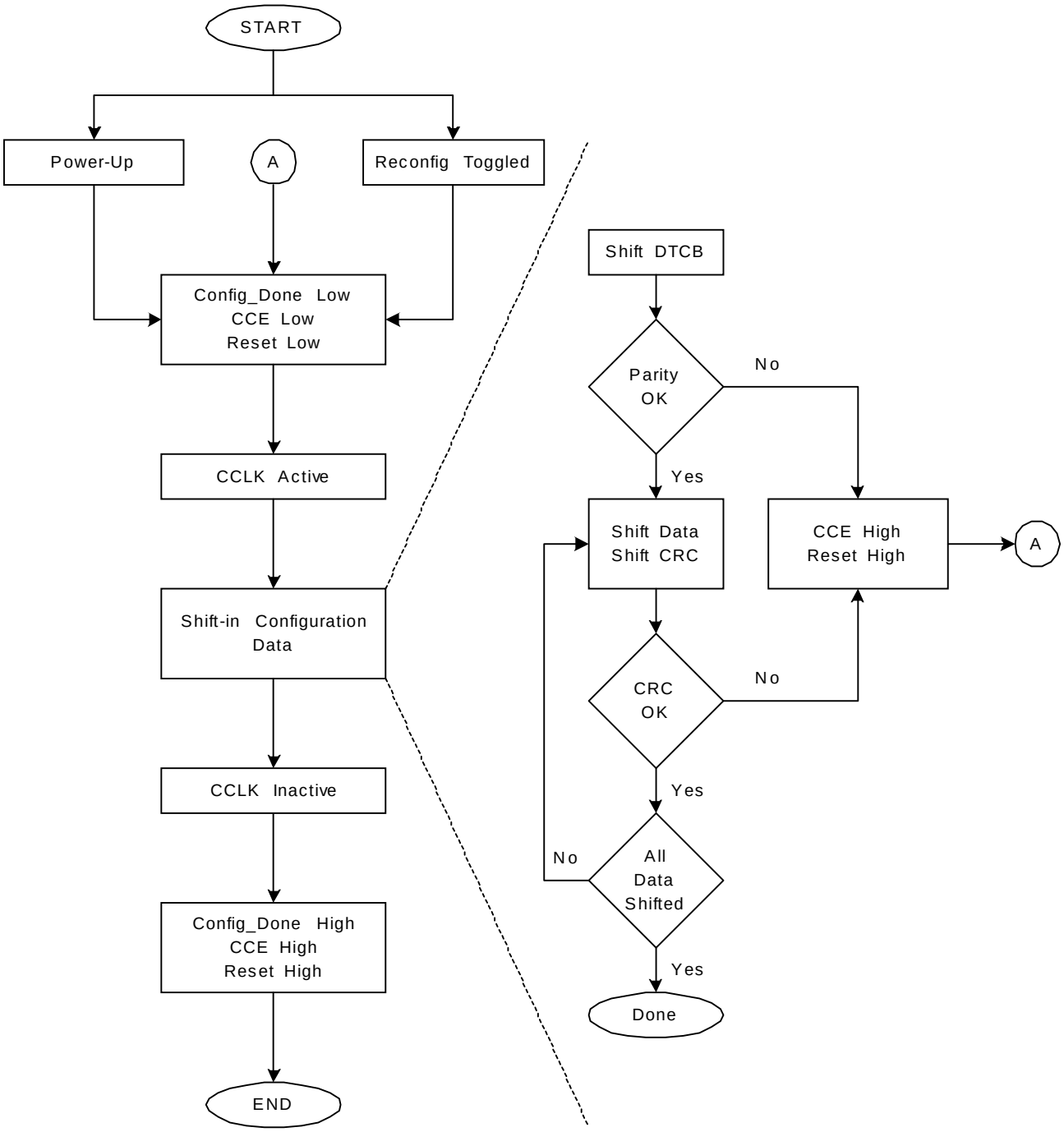
Table 5. Configuration Port (Master Serial) Read Cycle Timing Requirements

Parameter	Definition	Min.	Max.	Unit
t_{RCL}	Reconfig Low Time	200		ns
t_{RCH}	Reconfig High Time		200	ns
$t_{CELCL/RLCL}$	CCE/Reset Low to First CCLK Positive Edge		3.5	µs
t_{SU}	CDATA Set-up to CCLK	20		ns
t_{OH}	CDATA Hold from CCLK	0		ns
$t_{HC/LC}$	CCLK - High/Low time	60	250	ns

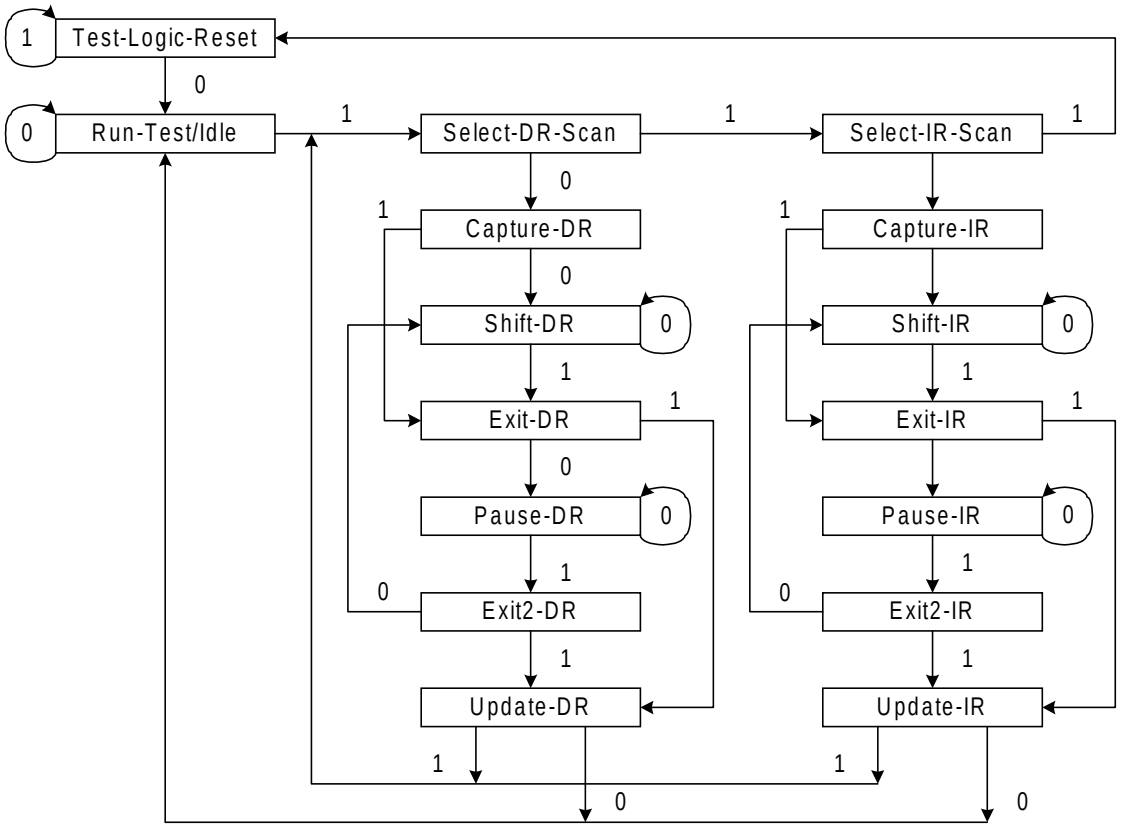
APPENDIX B - Delta39K/Quantum38K Design Flow



APPENDIX C - Internal Flash and External EEPROM Configuration Flow

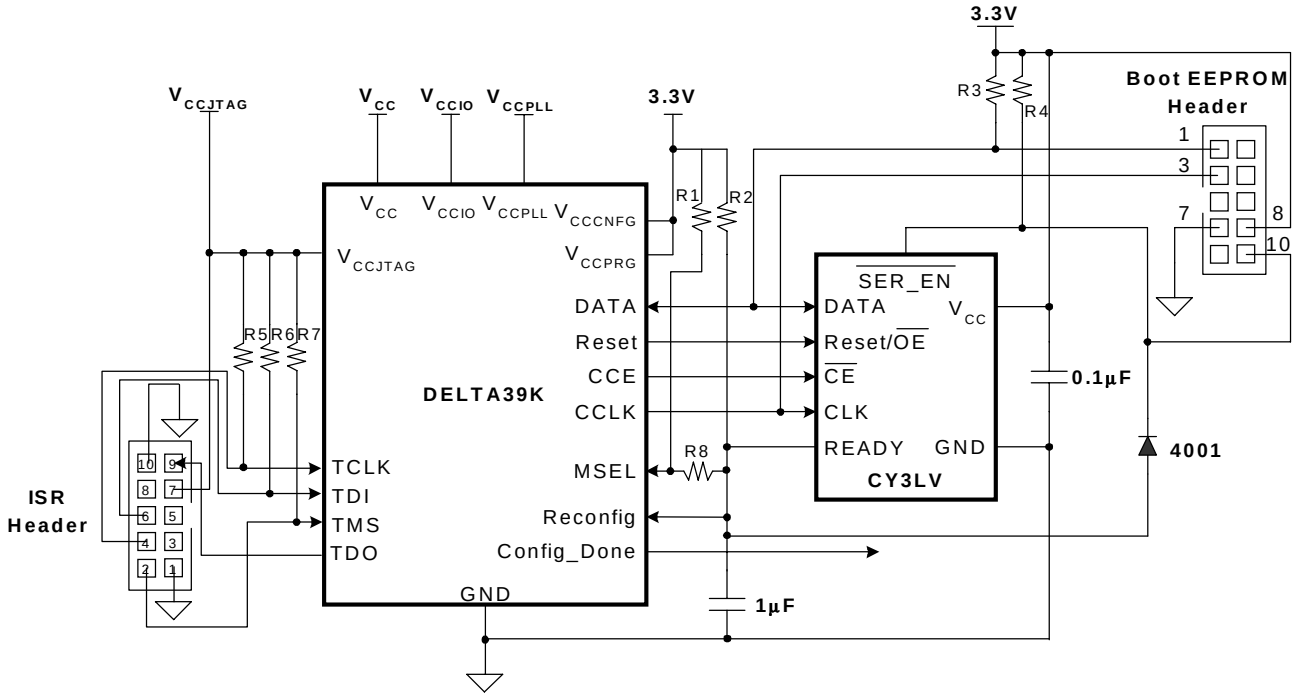


APPENDIX D - JTAG TAP Controller



Transitions based on TMS on the rising edge of TCK

APPENDIX E - CY39100V208 and CY39100V208A Board Setup



Follow the population guidelines below to allow migration from CY39100V208 or CY39100V208A to CY39100V208B. For further information on CY39100V208, CY39100V208A, and CY39100V208B please refer to the Delta39K Datasheet Errata page.

CY39100V208 and CY39100V208A:
R1: Not Populated
R2-R7: 4.7kΩ
R8: 0Ω

CY39100V208B:
R1-R7: 4.7kΩ
R8: Not Populated

The intent of the schematic above is to allow a designer using CY39100V208 or CY39100V208A to lay out their board once by providing a migration path from CY39100V208/CY39100V208A to CY39100V208B. The PCB of a design using CY39100V208/CY39100V208A should be laid out to match the schematic above (the schematic for the CY39100V208B and all other Delta39K family members can be found on page 5 of this application note). The population guidance on the left should be followed when the devices used are CY39100V208/CY39100V208A. Once the CY39100V208B is received, the same PCB layout can be used — except this time the resistors are populated differently. The effect of the population change is to have Reconfig separate from MSEL for CY39100V208B and to have Reconfig shorted to MSEL for CY39100V208 and CY39100V208A.