Understanding Bus-Hold—A Feature of Cypress CPLDs

This application note covers the bus-hold feature of Cypress's FLASH370i™, Ultra37000™, and Ultra37000V™ families of complex programmable logic devices (CPLDs). Included is a discussion of the history behind the bus-hold feature and specific details about Cypress's implementation of bus-hold.

Introduction

The FLASH370i, Ultra37000, and Ultra37000V families of CPLDs have a unique feature called bus-hold on all I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototypes as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Why Bus Hold—A Brief History

To fully understand the need for the bus-hold feature, a knowledge of the history behind bus-hold is essential. There are three configurations of device I/Os and dedicated inputs that have been historically used in CPLDs. These configurations are:

1. Inputs and I/Os that are unbiased by internal circuitry,
2. Inputs and I/Os with internal pull-up resistors, and
3. Inputs and I/Os with internal bus-hold latches.

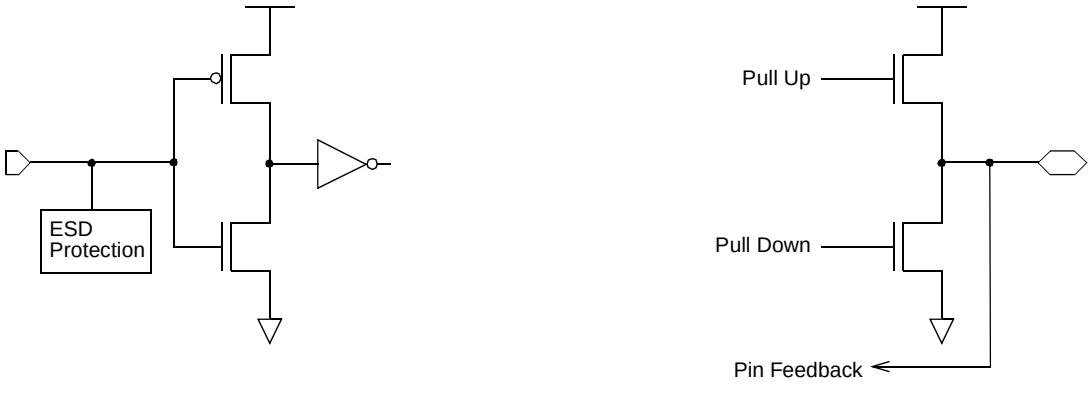
A detailed description of each of these configurations is given in the sections that follow.

Devices With Unbiased Inputs and I/Os

Many CPLDs on the market today have dedicated inputs and I/Os similar to those shown in *Figure 1*. These inputs and I/Os have no internal biasing circuitry and are therefore commonly referred to as "floating" when no other circuitry is actively driving the inputs.

When the input to the CPLD is floating, oscillations can occur due to the potential of externally biasing the input buffer around its trip point. Due to the fact that the floating input is very high impedance, noise injected from other components on the board can cause the input to move around the trip point of the input buffer as shown in *Figure 2*. Each time the input voltage transitions across the trip point of the input buffer, the input buffer will change state. The change in state can propagate completely through the device and cause outputs of the CPLD to switch. Switching the CPLD outputs creates more noise on the board, increases the switching noise on the floating input, and potentially creates device oscillation. This oscillation can result in functional problems with the design as well as increase the power requirements of the CPLD.

Due to the oscillation problems inherent with floating inputs, designers must ensure that the inputs to the CPLD are always properly biased. This requires all unused pins to be connected to V_{CC} or GND. This hard-wired connection will require the designer to cut PCB traces to make any modifications to the design that requires the use of a previously unused pin. Designs that have bus interfaces, or inputs that can be left floating by circuitry external to the device, must take care to bias the signal traces on the board to prevent this oscillation. This requires, at minimum, an external pull-up resistor to ensure that the input is biased to a voltage that is not near the trip point of the device.



a. Input **b. I/O**

Figure 1. Schematic of Dedicated Input and I/O with No Internal Biasing Circuitry

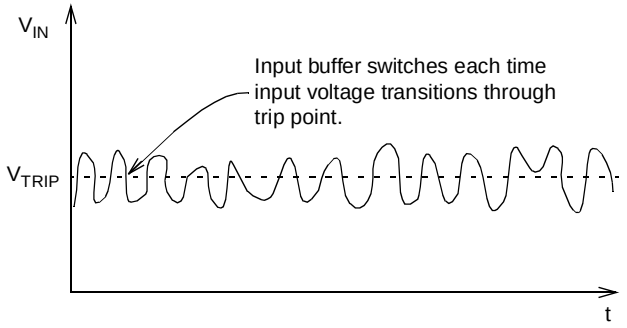


Figure 2. Possible Floating Input Voltage Due to Noise

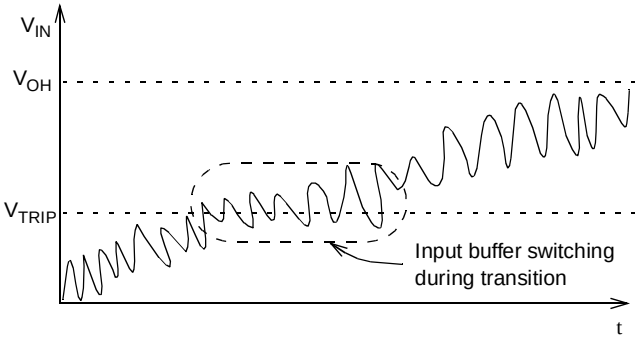


Figure 4. Slow Rise Time with Pull-up Resistor

Devices With Internal Pull-Up Resistors

As an improvement over the inputs and I/Os that are unbiased, an internal pull-up resistor is offered on some CPLDs as shown in *Figure 3*. This internal pull-up resistor eliminates the need for the designer to connect unused pins to V_{CC} or GND. Therefore, any unused pins can be utilized to implement design changes without the need to cut the PCB traces to V_{CC} or GND.

However, the pull-up resistor does not eliminate the potential for device oscillation for designs that have bus interfaces or designs that have pins that can be left floating by external circuitry. When a bus signal transitions to three-state, the previous state will determine if the potential for device oscillations exist. If the previous state of the bus signal was HIGH, the pull-up resistor will simply maintain the current HIGH state. However, if the previous state of the bus signal was LOW, the pull-up resistor will slowly transition the input or I/O to V_{CC}. This results in an input voltage that slowly transitions through the region near the trip point of the input buffer. In order to allow the pull-up resistor to be easily overpowered by external drivers of the input or I/O, the internal pull-up resistances are typically large (50KΩ to 100KΩ). The large resistance value results in a very slow slew rate of the input voltage during the time it transitions from LOW to HIGH. Since the input voltage passes through the region near the trip point very slowly, noise from other components can potentially create device oscillation. *Figure 4* is an example of what the actual input voltage waveform can look like during this transition.

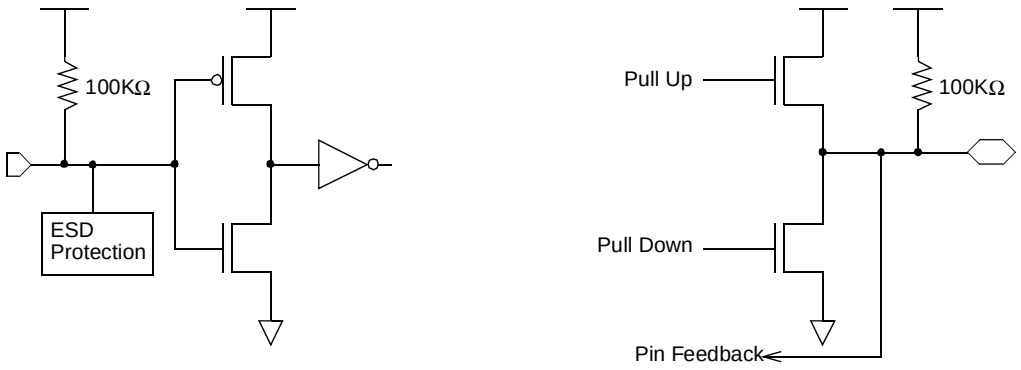
Devices With Bus-Hold Latches

To alleviate the condition where the pull-up resistor slowly transitions from LOW to HIGH, the bus-hold circuit, shown in *Figure 5*, is connected to each dedicated input and I/O. The circuit is a latch that will hold the existing state of the bus whenever the bus is three-stated, hence the name bus-hold. By retaining the previous state of the bus, the input voltage can not transition across the trip point of the input buffer when the bus is three-stated.

The latch is simply two inverters that loop back to the input of the device. The output voltage of the bus-hold circuit is limited to an NMOS threshold voltage below V_{CC} to match the V_{OH} characteristics of the output driver in the I/Os, except for the Ultra37000V devices. The bus-hold feature is available on all FLASH370i, Ultra37000, and Ultra37000V devices.

Bus-Hold Electrical Specifications

Table 1 lists the electrical specifications of the bus-hold latch. I_{BHL} and I_{BHH} are the LOW and HIGH sustaining currents respectively. This specification indicates that the bus-hold latch will sink or source 75 µA and still maintain the current state. As a result of this specification, the bus-hold latch will contribute 75 µA to the existing I_{OL} and I_{OH} specifications. This additional current results in a very small percentage change of I_{OH} and I_{OL} since these specifications are typically –3.2 mA and 16 mA respectively.



a. Input **b. I/O**

Figure 3. Input and I/O with an Internal Pull-up Resistor

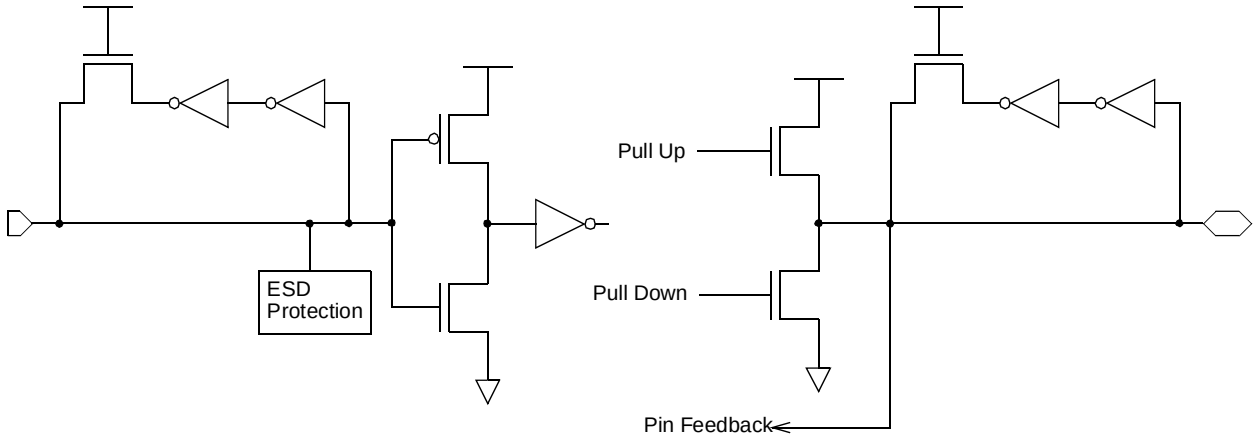


Figure 5. Input and I/O with Bus-hold Latch

Table 1. Bus-Hold Electrical Specifications

Param	Description	Min	Max	Unit
I_{BHL}	Input Bus-Hold LOW Sustaining Current	+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current		+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current		–500	µA

I_{BHLO} and I_{BHHO} are the LOW and HIGH overdrive currents respectively. In order to change the state of the bus-hold latch, an external driver must source I_{BHLO} or sink I_{BHHO}, depending on the state of the bus-hold latch. For example, if the current state of the bus-hold latch is HIGH, an external driver must sink 500 µA to change the state of the bus-hold latch to LOW.

Another electrical specification that is affected by the bus-hold feature is I_{OZ}. I_{OZ} is defined to be the output leakage current when the CPLD I/O is in three-state. For CPLDs that do not have bus-hold, or any other internal biasing circuits, this specification is usually a constant value regardless of the input voltage that appears on the device I/O. However, for devices with bus-hold, or any other internal biasing circuits, the I_{OZ} specification must account for the additional current supplied by this biasing circuitry. *Figure 6* shows the worst-case additional current that is present on each input or I/O that has the bus-hold feature. As the input voltage, Vin, transitions from one state to another, the bus-hold latch will source or sink the amount of current indicated on the graph.

For more specific details about bus-hold electrical specifications and the test conditions, see the appropriate device data sheet.

Bus-Hold and 3.3V I/Os

The FLASH370i and the Ultra37000 families of CPLDs can be configured to operate in both 3.3V and 5.0V systems. There are two power supply configurations that allow the I/Os to operate at 3.3V:

1. Both the FLASH370i and the Ultra37000 families of CPLDs allow a 5.0V internal and 3.3V I/O power supply.
2. The Ultra37000V family of devices allow a 3.3V only power supply operation.

5.0V Internal, 3.3V I/O Configuration

All devices in both the FLASH370i and the Ultra37000 families of CPLDs have two separate sets of supply pins: one set, V_{CCINT}, for the internal operation and input buffers and another set, V_{CCIO}, for I/O output drivers. The V_{CCINT} pins must be connected to a 5.0V power supply. However, the V_{CCIO} pins may be connected to either a 3.3V or 5.0V power supply, depending on the output requirements.

Regardless of whether or not the V_{CCIO} supply voltage is connected to 3.3V, the bus-hold circuitry is connected to the V_{CCINT} supply which is connected to a 5.0V power supply. Therefore, when the V_{CCIO} supply is connected to a 3.3V power supply, the bus-hold latch will affect the V_{OH} of the device when the I/O is in three-state. This effect on V_{OH} is described by the V_{OHZ} electrical specification in the device

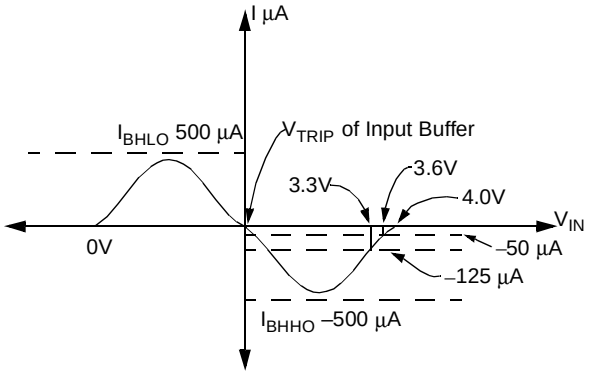


Figure 6. Bus-Hold IV Characteristics for 5.0V Internal and 5.0V/3.3V I/O Supplies

data sheets. In general, if no I_{OH} current is being supplied by the device, the bus-hold latch will pull the output voltage up to approximately 4.0V as indicated in *Figure 6*. If this higher V_{OH} presents a problem for devices connected to this output, the V_{OH} can be lowered by simply placing a resistor to GND on the device I/O. If this resistor is sized such that an I_{OH} of –50 µA is present, it will lower the output voltage to 3.6V as indicated in *Figure 6*. Lower V_{OH} values, down to 3.3V, can be achieved by simply resizing the pull-down resistor in accordance with the values on the graph in *Figure 6*. If the device I/O is not in three-state, the output driver will actively supply a 3.3V V_{OH}.

3.3V Internal, 3.3V I/O Configuration

The Ultra37000V family of devices will allow a 3.3V-only power supply operation. For the 3.3V-only devices, the N-channel device in the output path of the bus-hold circuit is removed on both the inputs and I/Os as shown in *Figure 7*. Both the bus-hold latch and the I/O output driver are connected to the 3.3V power supply. Even though the bus-hold latch is connected to a 3.3V power supply, the I_{BHLO} and I_{BHHO} specs are the same as if the bus-hold latch were connected to a 5.0V power supply. The only difference is the V_{OH} of the output driver and the bus-hold latch will be limited to 3.3V. *Figure 8* is a graph of the worst-case bus-hold current for the 3.3V power supply option on the Ultra37000V family of devices.

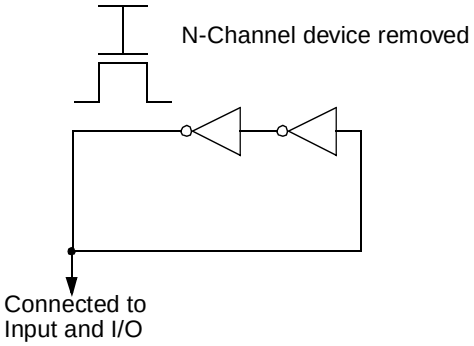


Figure 7. 3.3V Bus-hold Latch

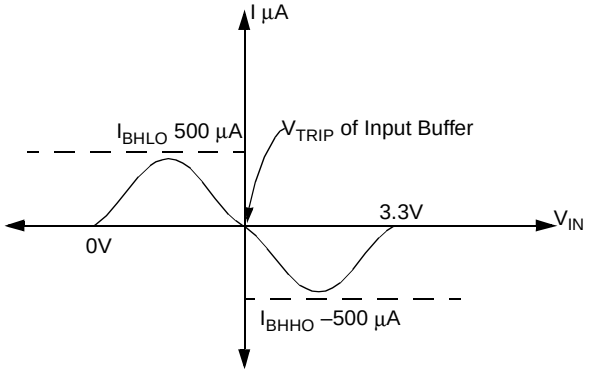


Figure 8. Bus-Hold IV Characteristics for 3.3V Internal and 3.3V I/O Supply

Bus-Hold and External Circuitry

The interface of devices with the bus-hold feature is different from devices that have internal pull-up resistors or to devices that have no internal biasing. Several specific differences include how to properly size an external resistor to V_{CC} and the fan-out effects of connecting multiple device inputs or I/Os to a signal in a bus. These differences are discussed in the examples that follow. These examples assume that the devices are configured for 5.0V power supply operation; however, the same applies for 3.3V I/O power supply operation.

Proper External Resistor Sizing

Many designs require the use of an external pull-up resistor with a CPLD. An example is a design with a set of DIP switches that allow the user to configure the design according to their specific needs. *Figure 9* shows an equivalent schematic of how the DIP switch could be connected. When the switch is closed, the pin on the CPLD is shorted to GND and when the switch is open, the pull-up resistor will pull the pin on the CPLD to V_{CC}.

Several parameters must be known in order to properly size the pull-up resistor, R1, shown in *Figure 9*:

1. The bus-hold overdrive current, I_{BHLO}.
2. The trip point of the bus-hold latch, V_{TRIP}. This value is always the same as the normal input buffer of the device. For the FLASH370i, Ultra37000, and Ultra37000V devices, the input trip point is nominally 1.5V.
3. Worst case V_{CC}, V_{CC} MIN. For the commercial temperature range of the 5.0V FLASH370i and Ultra37000 families of CPLDs, V_{CC} MIN is 4.75V.

Once these parameters are known, the proper pull-up resistor size can be determined by:

$$R1 = \frac{V_{CC}MIN - V_{TRIP}}{I_{BHLO}}$$

Which results in a pull-up resistance of:

$$R1 = \frac{4.75V - 1.5V}{500\mu A} = 6.5K\Omega$$

Designers that have applications that require a pull-down resistor can use a similar method to determine the resistor sizing.

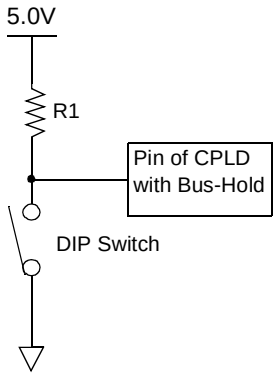


Figure 9. Example Design with DIP Switches

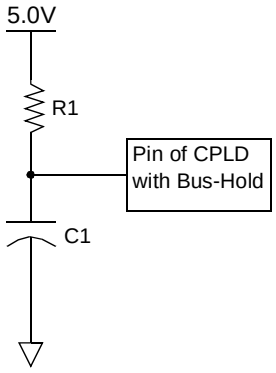


Figure 10. Typical Power-up Circuit for CPLDs

RC Power-up Circuits and Bus-hold

Another common circuit configuration that can be affected by the external pull-up resistor sizing is shown in *Figure 10*. This circuit configuration is often used as a power-up circuit for the CPLD and the system. In order to achieve the correct RC time constant for the circuit, the resistor size cannot be adjusted above the 6.5 KΩ calculated above. If a pull up resistor larger than 6.5 KΩ is used, the bus-hold latch will prevent the capacitor from being charged to a voltage that is high enough to switch the bus-hold latch. Therefore, the circuit will never transition out of the powered down state.

Fan-out Effects of Bus-hold Devices

Many designs that contain buses will also have multiple CPLDs connected to a signal in the bus. The designer should be aware of the additive nature of the overdrive currents of the bus-hold latch. For example, if a signal in a bus connects to three different CPLDs, each of which have a bus-hold latch, the overdrive current will be the maximum of (3 * I_{BHLO}) or (3 * I_{BHHO}). For the specifications given in *Table 1*, the overdrive current for bus signals that connect to 3 CPLDs would increase to 1.5 mA. *Figure 11* illustrates this example.

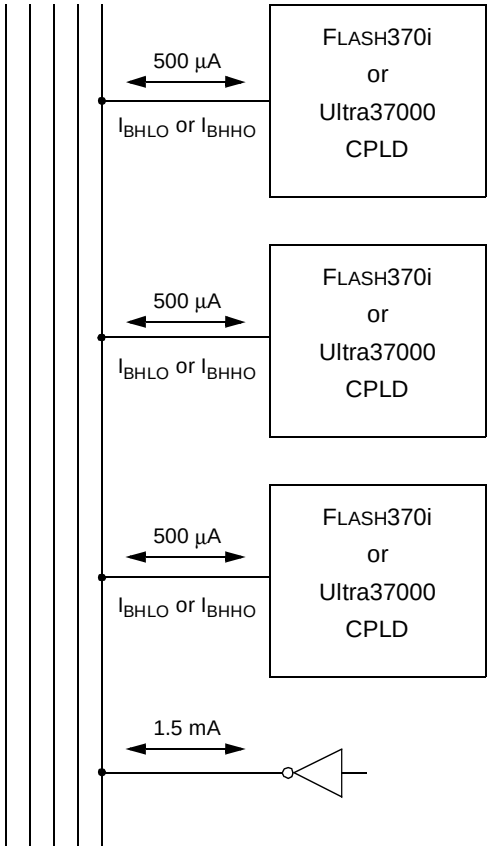


Figure 11. Additive Nature of I_{BHLO} and I_{BHHO}

Summary

This application note provides the history behind the bus-hold feature and information on how to more effectively design with CPLDs that have bus-hold. The bus-hold feature is currently available on the FLASH370i, Ultra37000, and Ultra37000V families of CPLDs.

The bus-hold feature of Cypress CPLDs can greatly improve the noise immunity of a design. By retaining the last state of the inputs, there is no opportunity for the floating input voltage to slowly transition through the trip point of the input buffer, thereby eliminating the potential for unwanted device oscillations. The bus-hold feature also has the added benefit of allowing designers to leave unused input or I/O pins unconnected. The bus-hold latch will bias the unconnected pins to a HIGH or a LOW state and keep the floating input voltage away from the trip point of the input buffer.