Board Layout Considerations for ISR™ Programming of Cypress CPLDs

Introduction

This application note provides information regarding board layout and design for In System Reprogrammable™ (ISR™) programming from a PC through an ISR cable. ISR enables devices to be programmed and reprogrammed on the Printed Circuit Board (PCB) after they have been soldered on to the board. Included are the schematics of the ISR programming cables, which provides buffering of the serial programming interface from the parallel port of a PC to the devices soldered onto the PCB. It also discusses transmission line effects that can arise from the ISR chain and provides suggestions for trace layout to minimize these effects, which can cause signal integrity problems. Transmission line effects are inherent in the ISR programming set-up due to both impedance mismatching between the ISR cable and traces on the PCB and the trace layout itself on the PCB. Buffering on the board with termination, while not required in most cases, produces the highest quality waveforms and provides the best solution to reducing transmission line effects.

UltraISR™ Cable Schematic

The UltraISR cable schematic is shown in *Figure 1*. The ISR cable, for programming the FLASH370i™ devices is also shown in *Figure 2*. The UltraISR cable was designed to program a variable number of devices in an ISR chain, from 1 to

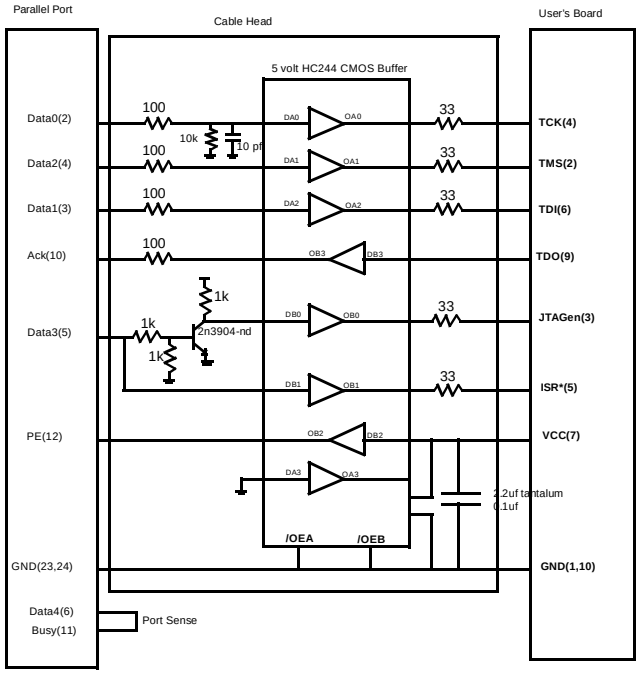

Figure 1. UltraISR Cable Schematic rev 0.03

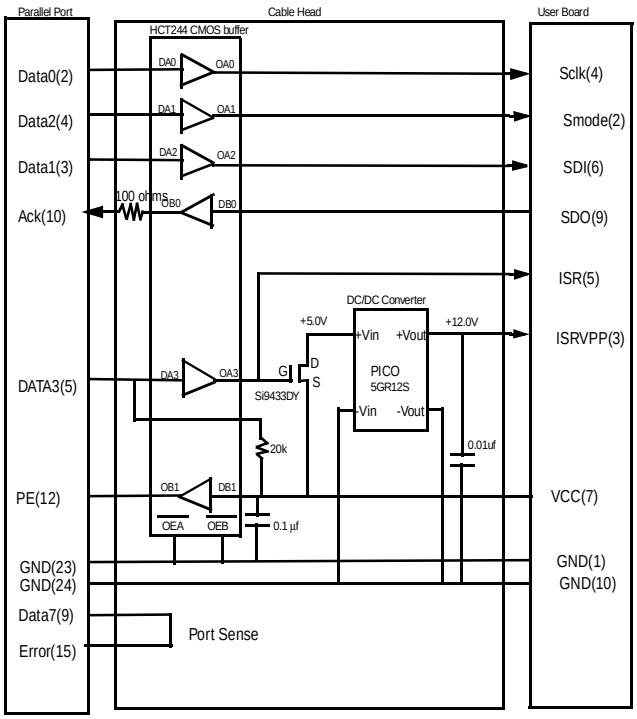

Figure 2. ISR Cable Schematic rev 0.03

8 devices. An additional requirement of the cable is that termination resistors would not be required in most cases. The frequency of the clock signal during ISR operations is slow, about 1 MHz, but the signal transition edge rates are fast, 5 to 10 ns, relative to the propagation delay from the buffer driver through the ribbon cable to the end of the ISR chain. Transmission line effects are therefore inevitable; however, certain layout practices can greatly reduce their harmful effects. These effects can occur on any of the four ISR signals but it will only cause potential ISR failure on the clock signal. This is because there is plenty of time, many hundreds on nanoseconds, for the signals to settle before the rising clock edge. Care should be taken on the clock signal trace layout. A discussion of possible transmission line effects is necessary to understand how to best design the ISR chain. While this application note focuses on ISR programming from a PC at low frequency, the following discussion can also apply to other methods of programming occurring at higher frequency such as from an on board microprocessor.

Transmission Line Effects

There are two transmission line effects that can be encountered. They are illustrated in *Figures 3* and *4*. These are overshoots with ringing after the edge transition and notching of

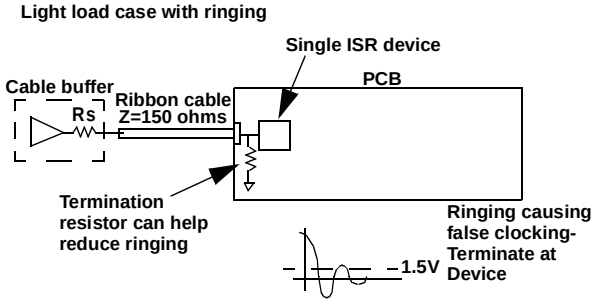

Figure 3. Transmission Line Effect—Ringing

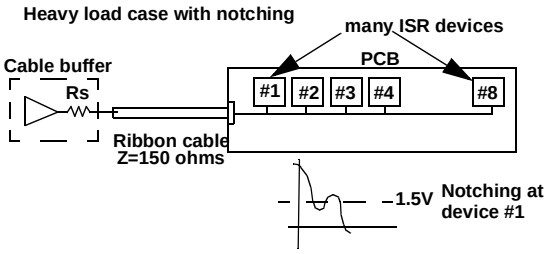

Figure 4. Transmission Line Effects—Notching

the signal during the edge transition itself. The first effect, overshooting and ringing, is worst-case with very light capacitive load. It can be minimized by matching the impedance of the load to the line impedance and the cable impedance to the buffer impedance. While the ringing is not typically big enough to cause failure, it can be diminished by terminating the single device load near the device with a single 200-ohm resistor to ground as shown in *Figure 3*. Values much smaller than 200 ohms can begin to degrade the output high level due to the voltage divider effect of the termination resistor and the buffer plus Rs resistance. Parallel termination, which employs a resistor connection to V_{CC} and to ground, is not recommended because it can degrade the V_{OL} of the output buffer due to the voltage divider action of the resistor to V_{CC} and the buffer plus Rs resistance to ground.

The other transmission line effect that can cause false clocking is a notching, or glitching, of the clock transition in the middle of the transition itself. The notch is evident on both edges of the clock. The notch occurs because of a voltage divider effect between the source impedance of the buffer, plus 33 ohms in this case, and the characteristic impedance of the transmission line Z. If the notch resides near the trip point of the ISR device, (1.5 volts for both Ultra37000™ and Ultra37000V devices), then it could result in a false clock resulting in ISR operation failure. This effect more typically occurs with multiple devices in the ISR chain because of differing clock line trace lengths.

The layout of the clock shown in *Figure 5* makes a big difference in reducing this transmission line effect. If the clock trace is laid out exactly as shown in *Figure 4* then the first device can experience a notch of duration 2T, where T is the transmission line delay from device #1 to the end of the chain at device #8. Making the clock trace the same length to device #1 as device #8 as shown in the second figure in *Figure 5* can

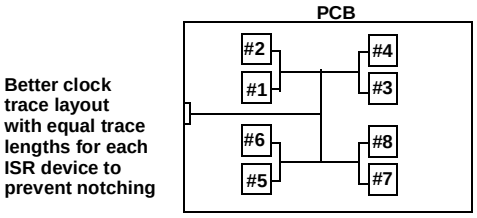

Figure 5. Clock Trace Layout

remove this notching effect. In general it is good to avoid stubs on the clock line to minimize this effect.

Adding Extra Buffering on the PCB

While the UltraISR cable buffer and series resistor are designed to give good results from 1 to 8 devices in the programming chain without on board buffering, the best signal integrity for the clock line is achieved by incorporating buffering on the board as shown in *Figure 6*. This buffering, with termination, can guard more effectively against both of the transmission line effects previously described. The buffer and 200-ohm termination resistor should be placed close to the 10-pin header connector so that the termination resistor can match the cable characteristic impedance and prevent reflection at the on board buffer input. The on board buffer can provide separate buffering for each ISR device clock line and the 33-ohm series resistor, placed close to the buffer output, can match the characteristic impedance of the trace on the board and prevent reflections at the buffer output. In *Figure 6*

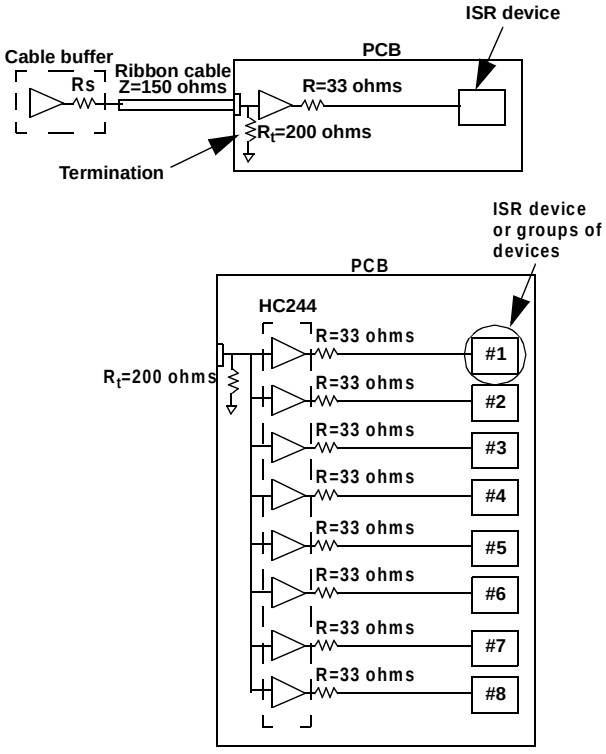

Figure 6. Buffering with Termination

it is not crucial that the clock traces be the same for each device clock since there is no danger of a race condition from one ISR device to the next. This is because the data output from one ISR device does not propagate to the next device until the falling edge of the clock as defined in the IEEE 1149.1 specification. The HC buffer, such as the HC244, is recommended for on board buffering. Avoid the FC buffer since the faster edge rates will worsen transmission line effects. Extra buffering with termination is recommended whenever the impedance of the trace changes greatly, such as the connection between a PCB and an add-on card. For the case where more than 8 devices are required in the ISR programming chain then *Figure 6* can be followed with each clock buffer driving multiple devices as shown in *Figure 5*. If many more than 8 ISR devices reside on the PCB then the scheme in *Figure 6* can be used where multiple devices can exist at each of the numbers locations, 1 to 8, as shown in the figure. Equal clock trace lengths can then be employed for each of these groups of ISR devices.

Summary

The UltraISR cable is designed to program from 1 to 8 ISR devices on the PCB without extra buffering and termination. This UltraISR cable provides good clock signal integrity for different number of devices in the ISR chain and different clock trace layout configurations. The best clock signal integrity; however, can be achieved by buffering the ISR clock signal on the PCB with termination as described in this application note.

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