Using Cypress CPLDs in Mixed-Voltage Systems

Introduction

Improvements in process technologies provide better densities, increased performance and lower power consumption in programmable logic devices. As device dimensions are reduced, the voltage that the transistors can withstand also decreases. The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-volt and 5.0-volt systems while maintaining the lowest possible total-system power consumption.

This application note explains the mixed-voltage flexibility that Cypress CPLDs offer. It also discusses how Cypress's FLASH370i and Ultra37000/37000V can interface with different logic families in a mixed 3.3-volt and 5-volt environment.

Interfacing 3.3-Volt and 5-Volt Devices

The FLASH370i and the Ultra37000 families of CPLDs can be configured to operate in both 3.3-volt and 5.0-volt systems.

There are two power-supply configurations that allow the I/Os to operate at 3.3 volt:

1. Both the FLASH370i and the Ultra37000 families of CPLDs allow for a 5.0 volt internal and 3.3 volt I/O power supply.
2. The Ultra37000V family of devices allow for a 3.3 volt only power supply operation.

5.0-Volt Internal, 3.3-Volt I/O Configuration (5.0V/3.3V)

All devices in both the FLASH370i and the Ultra37000 families of CPLDs have two separate sets of supply pins: V_{CCINT} for the core and V_{CCIO} for the I/Os. V_{CCINT} pins must be connected to a 5.0V power supply while V_{CCIO} can be connected to either 3.3V or 5V. Refer to *Tables 1* and *2* for the V_{CCINT} and V_{CCIO} distribution in the FLASH370i and the Ultra37000 family.

When there are 3.3V and 5V devices on the same board, care must be taken to assure that the I/O signals from both the devices are compatible. There is no problem interfacing logic LOW levels in either direction. But compatibility issues need to be considered with logic HIGH levels.

5.0V/3.3V Driving 5V Devices

The minimum output high voltage (V_{OH}) of devices operating in this configuration is 2.4V. This is more than the minimum input high voltage for TTL levels (V_{IH}= 2.0V). So these devices can directly drive inputs on 5V TTL devices.

However, the V_{IH} for devices operating with CMOS input levels is 3.5V (the maximum V_{OH} of Cypress 5V devices is 3.6 volts). So for these CPLDs to drive a CMOS input high, a pull-up resistor (1K ohms to 4.7K ohms) must be used to pull the output above the CMOS V_{IH}min. The value of the pull-up is determined from speed and power considerations with smaller resistor values giving higher speed and higher power when the device output is in the LOW state.

Table 1. V_{CCINT} and V_{CCIO} for FLASH370i

Device	Package	V_{CCIO} (3.3V or 5.0V)	V_{CCINT} (5.0 V)
7c371i	PLCC(44)	44	22
7c371i	TQFP(44)	38	16
7c372i	PLCC(44)	44	22
7c372i	TQFP(44)	38	16
7c373i	PLCC(84)	21, 44, 63, 84	2, 42
7c373i	TQFP(100)	12, 24, 40, 49, 62, 74, 87, 99	90, 37
7c374i	PLCC(84)	2, 21, 42, 63	84, 44
7c374i	TQFP(100)	12, 37, 62, 90, 24, 49, 74, 99	62, 140
7c375i	TQFP(100)	20, 40, 60, 80,100, 120, 142, 160	62, 140

Table 2. V_{CCINT} and V_{CCIO} for Ultra37000/Ultra37000V

Device	Package	V_{CCIO} (3.3V or 5.0V)	V_{CCINT} (3.3V or 5.0V)
37256	TQFP(160)	20, 40, 60, 80, 100, 120, 142, 160	62, 140
37256	PQFP(208)	27, 52, 78, 104, 131, 157, 184, 207	80, 129, 182, 208
37128	PLCC(84)	2, 21, 42, 63	44, 84
37128	TQFP(100)	12, 24, 37, 49, 74, 90, 99	40, 87
37128	TQFP(160)	20, 40, 60, 80, 100, 120,142, 160	62, 140

5.0V/3.3V Driving 3.3V Devices

Cypress CPLDs have a bus-hold feature on all dedicated inputs and I/Os to prevent them from floating and generating excess noise. Regardless of whether or not the V_{CCIO} is connected to the 3.3V, the bus-hold circuitry is connected to V_{CCINT} of 5.0 V. Therefore, when the V_{CCIO} supply is connected to a 3.3 V power supply, the bus-hold latch will affect the V_{OH} of the device when the I/O is three-stated. This effect on

V_{OH} is described by the V_{OHZ} electrical specification in the device data sheets. In general, if no I_{OH} current is being supplied by the device, the bus-hold latch will pull the output voltage up to approximately 4.0V. If this drives a device operating at 3.3V and if this high V_{OH} poses a problem, then a resistor can be connected to ground on the device I/O to lower the V_{OH}. For more details, refer to the note *Understanding Bus Hold —A Feature of Cypress CPLDs*.

5.0V/3.3V Driven By 5V Devices

The FLASH370i and Ultra37000 devices do not employ a diode clamp to V_{CC}. TTL and CMOS devices operating 5 volts can drive FLASH370i and Ultra37000 directly. These devices can tolerate 5V without the need of an external resistor to limit input current.

5.0V/3.3V Driven By 3.3V Devices

The minimum input logic HIGH threshold, V_{IH}min, of these family of devices is 2.0V which is less than the minimum V_{OH} (CMOS) threshold specification for 3.3V devices. The V_{OH} minimum is 3.3 volts because there is no DC current loading for the CMOS inputs of Cypress devices. So 3.3V devices may directly drive CPLDs in this configuration.

3.3-Volt Internal, 3.3-Volt I/O Configuration (3.3V/3.3V)

The Ultra37000V requires 3.3V on all of the V_{CC} pins. These devices support 3.3V JEDEC standard CMOS output levels. Both the bus-hold latch and the I/O output driver are connected to the 3.3V power supply. So the V_{OH} of the output driver and the bus-hold latch will be limited to 3.3V.

3.3V/3/3V Driving 5V Devices

The minimum output high voltage (V_{OH}) of devices operating in this configuration is 2.4V. This is more than the minimum input high voltage for TTL levels (V_{IH}= 2.0V). So these devices can directly drive inputs on 5V TTL devices.

However, the minimum V_{IH} for devices operating with CMOS input levels is 3.5V. So for a Cypress CPLD to drive a CMOS input high, a pull-up resistor (1K to 4.7K) must be used to pull it above the CMOS V_{IH}min.

3.3V/3.3V Driving 3.3V Devices

The Ultra37000V devices can drive 3.3V devices without any interface issues.

3.3V/3.3V Driven By 3.3V and 5V Outputs

A CMOS output structure will normally draw current on the output pin when the output is driven one diode voltage above the 3.3-volt V_{CC} voltage. The current flows directly from the output pins to the V_{CC} supply. The I/Os of the Ultra37000V employ special 5-volt tolerant circuits to prevent this current from flowing. The dedicated inputs do not employ a diode clamp to V_{CC} so they are also 5-volt tolerant. Therefore the 3.3V devices can tolerate 5V without the need for current limiting resistors. This makes them suitable for mixed voltage systems. Please note that the 3.3V device cannot be driven by more than 3.3V before Vcc is applied.

The 37000V devices can be driven directly without any interface issues from 3.3V devices.

Conclusion

Many new designs require lower operating voltages. Cypress not only offers 3.3V compatibility but also provides an ISR (In-System Reprogrammable) solution to facilitate design changes and field upgrades. As discussed above, with Cypress CPLDs, interfacing in today's mixed voltage environment is pretty simple. Designers can take advantage of the In-System Reprogrammability and easily transition to 3.3V operation for their existing designs without a change in the board layout.