Power Estimation and Thermal Management for Cypress CPLDs

Introduction

The amount of power consumed by a programmable logic device is dependent upon the design's utilization of its resources. Understanding the architecture of the device is the first step in estimating a design's power consumption. In the FLASH370i™ and Ultra37000™ family of CPLDs, the architecture consists of two or more logic blocks which communicate with each other and the pins of the device via a programmable interconnect matrix (PIM). Logic block inputs from the PIM first enter an AND-array where a product term is implemented by enabling the connection between the logic block input signal and the input to the product term. The number of implemented product terms is one of the major design-dependent factors in the consumption of power. Once the product terms have been implemented, the product term output must be enabled so the OR-array can use them. This is the second major design-dependent factor on power consumption. After the sum-of-products through the AND-array and the OR-array have been implemented, each resulting signal enters a macrocell where it may be registered or nonregistered, sent to outputs, or several other functions. The macrocells in the logic block and the frequency at which they operate are the third significant contributor to power consumption of the device. If there are multiple clocks in the design, each has to be taken into account separately. In addition to the aforementioned features, the Ultra37000 family has logic blocks which may be powered down individually to consume about half as much power.

Once power has been calculated for the device, it may be used to determine the thermal behavior of the circuit. Knowing the junction temperature helps operate the device safely with optimum performance. Power estimation and thermal calculation should be done early in the design to help choose the right package type and, if necessary, additional power saving methods.

Disclaimer: This document is for reference only. The following equations are for power consumption estimations only. Cypress does not provide a guarantee of any kind on these power estimations.

Icc Model

To calculate power consumption, the total Icc current must be determined. The total Icc is comprised of three components: DC (or standby) current, AC (or operation) current, and external (or load) current.

$Icc_{TOTAL} = Icc_{DC} + Icc_{AC} + Icc_{EXT}$

DC Supply Current

The formula for calculating the DC supply current for a FLASH370i or Ultra37000 design is:

$Icc_{DC} = Icc_{Blank} + Kpt_{LowPower} * Npt_{LowPower} + Kpt_{FullPower} * Npt_{FullPower} + Icc_{FullPower} * Nlb_{FullPower} + Icc_{LowPower} * Nlb_{LowPower}$

(The low-power terms do not apply to FLASH370i devices)

Icc is the current draw of a part measured in mA. Icc_{Blank} is the current draw of an unprogrammed device. See *Table 1* to find the supply current for your device.

Kpt is the product term current draw constant measured in mA per product term. Refer to *Table 1* for Kpt values.

Npt is the number of product terms used in the device.

Nlb is the number of logic blocks used in the device. The total of logic blocks used in low power and full power mode is the number of available logic blocks in that device (e.g., the sum of $Nlb_{FullPower}$ and $Nlb_{LowPower}$ of Ultra37064 is 4).

The *Warp* report file (.rpt) for your design will reveal the number of product terms used and which logic blocks are running in lower power mode. The report file contains a product term placement chart (labelled, "Logic Block N Placement") for every logic block in the device. Following the chart are several statistics for the logic block, including the maximum number of product terms used in the logic block (*Figure 1*).

To determine whether the logic block is running in lower power mode, look for the Signal Requests section (under the heading, "Design Header Information"). There will be a LOW_POWER group listing all the logic blocks running in low power (*Figure 2*).

To find the **Npt** value, total up the maximum number of product terms used for every logic block. Don't forget to separate the product terms as LowPower or FullPower when using an Ultra37000 device with powered down logic blocks.

AC Supply Current

AC supply current increases linearly with the frequency of the application implemented in the device. It is comprised of two primary components: current drawn by the clock tree and current drawn by the macrocells. The following equation models the AC supply current for each clock in the design:

$Icc_{AC\ Clock\ \#} = (Kclk + Kmc * Nmc_{Clock\ \#}) * fmax(avg)_{\ Clock\ \#}$

The AC supply current values for each clock are summed together to give the total value

$Icc_{AC\ Total} = Icc_{AC\ Clock\ 1} + Icc_{AC\ Clock\ 2} + Icc_{AC\ Clock\ 3} + Icc_{AC\ Clock\ 4} + Icc_{AC\ Clock\ PT}$

Table 1. Icc_{BLANK}, $Icc_{FullPower}$, $Icc_{LowPower}$, and Kpt Values

	Icc_{Blank} (mA)	$Icc_{FullPower}$ (mA)	$Icc_{LowPower}$ (mA)	$Kpt_{FullPower}$ (mA/PT)	$Kpt_{LowPower}$ (mA/PT)
CY7C371i	11.5	N/A	N/A	0.237	N/A
CY7C372i CY7C373i	26.8	N/A	N/A	0.237	N/A
CY7C374i CY7C375i	42.0	N/A	N/A	0.237	N/A
CY37032	18.18	1.00	0.46	0.14	0.07
CY37064	21.35	1.00	0.46	0.14	0.07
CY37128	27.71	1.00	0.46	0.14	0.07
CY37192	34.06	1.00	0.46	0.14	0.07
CY37256	40.42	1.00	0.46	0.14	0.07
CY37384	53.13	1.00	0.46	0.14	0.07
CY37512	65.84	1.00	0.46	0.14	0.07
CY37032V	12.75	0.64	0.48	0.09	0.07
CY37064V	13.51	0.64	0.48	0.09	0.07
CY37128V	15.02	0.64	0.48	0.09	0.07
CY37192V	16.52	0.64	0.48	0.09	0.07
CY37256V	18.03	0.64	0.48	0.09	0.07
CY37384V	21.05	0.64	0.48	0.09	0.07
CY37512V	24.06	0.64	0.48	0.09	0.07

Kclk is the clock tree current draw constant measured in mA/MHz. This value is the same for each of the clocks in the design. See *Table 2* to find this constant value.

fmax(avg) is the maximum (average) operating frequency in MHz for the clocks (product term clocks) in the design.

Kmc is the macrocell current draw constant measured in mA/pt. See *Table 2* to find this constant value.

Table 2. Kclk and Kmc Values

	Kclk (mA/MHz)	Kmc (mA/PT)
CY7C371i	0.7	0.0334
CY7C372i CY7C373i	1.4	0.0334
CY7C374i CY7C375i	2.6	0.0240
CY37032	0.11	0.02
CY37064	0.21	0.02
CY37128	0.43	0.02
CY37192 CY37256	0.86	0.02
CY37384 CY37512	1.71	0.02
CY37032V	0.06	0.01
CY37064V	0.12	0.01
CY37128V	0.25	0.01
CY37192V CY37256V	0.49	0.01
CY37384V CY37512V	0.98	0.01

Nmc is the average number of macrocells switching every clock cycle for each clock. This value is application specific and must be determined by the designer.

The product term clock frequency is the average operating frequency of the product term clocks in the device.

Supply Current Due to Output Loading

The external supply current component has a DC part and an AC part, which are modeled by the following equation:

Icc_{EXT} = Iccext_DC + Iccext_AC

The DC external supply current is negligible for CMOS loads.

The AC external supply current for each clock in the design is formulated as:

$Iccext\_AC_{Clock\ \#} = 1/2 * N_{Out\ Clock\ \#} * C_{Load\ Clock\ \#} * V_{Swing} * fmax(avg)_{Clock\ \#} * tog_{IO} * Vcc_{IO}$

The AC external supply current values for each clock are summed together to give the total value:

$Iccext\_AC_{Total} = Iccext\_AC_{Clock\ 1} + Iccext\_AC_{Clock\ 2} + Iccext\_AC_{Clock\ 3} + Iccext\_AC_{Clock\ 4} + Iccext\_AC_{Clock\ PT}$

N_{Out} is the number of outputs associated with each clock.

C_{Load} is the output capacitance in Farads for each of the outputs specific to one of the clocks.

fmax is the maximum (average) frequency the outputs are toggling in MHz for each of the clocks in the design.

tog_{IO} is the ratio of outputs toggling for each of the clocks. Typically, a value of 0.125 may be used.

Vcc_{IO} is the voltage the I/Os are powered at.

V_{Swing} is the voltage swing of the external supply voltage. Use 3.8V for 5V devices and 2.5V for 3.3V.

Junction Temperature

The junction temperature may be found using the power calculated for the device and a thermal resistance constant. Thermal resistance is a measure of the ability of a device package to transfer the heat generated by the die to ambient or case. Θ_{JA} and Θ_{JC} are the most widely used constants in calculating the junction temperature. The equations are formulated as:

$T_J = \Theta_{JA} * P + T_A$

$T_J = \Theta_{JC} * P + T_C$

Θ_{JA} is the junction-to-ambient thermal resistance. The junction-to-ambient environment is a still-air environment. See *Table 3* for values.

Θ_{JC} is the junction-to-case thermal resistance. This is mainly a function of the thermal properties of the materials constituting the package. See *Table 3* for values.

P is the power at which the device operates. This value may be found from the power calculations, where $P = Vcc_{INT} * Icc_{Total}$

T_A is the ambient temperature at which the device is operated. Most common standard temperature of operation is room temperature to 70°C.

T_C is the temperature of the case (package).

Power Saving Suggestions

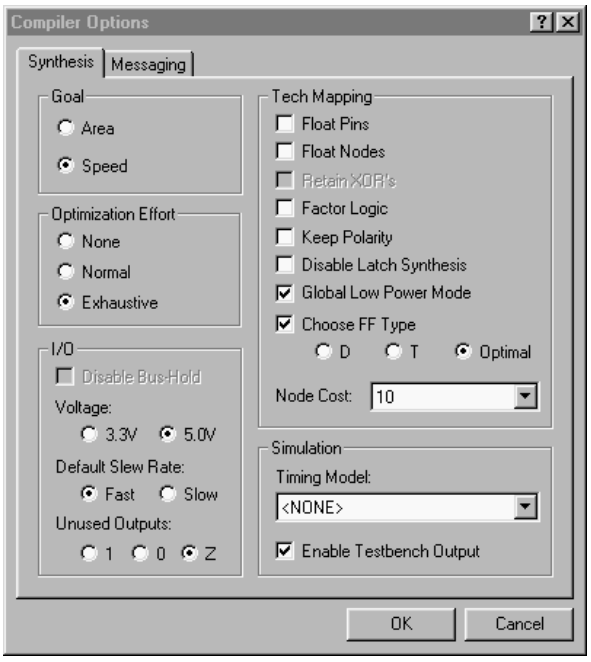
The rated speed of the FLASH370i and Ultra37000 CPLDs is dependent on the junction temperature. For commercial Ultra37000 devices, the junction temperature is 90°C; for industrial devices the junction temperature is 110°C. If the calculated junction temperature exceeds these values, then an estimated 100-ps performance degradation will occur for every 10°C above this temperature. However, if the temperature exceed 130°C, the reliability of the device will also degrade. A variety of methods can be used to dissipate heat faster and lower the junction temperature. The easiest way to dissipate more heat is to use a different kind of package. Looking at the Θ_{JA} and Θ_{JC} constants for the packages (*Table 3*), a lower value means that heat will be dissipated more quickly.

If there is no choice in the package, then maybe the design can be modified with one of the following techniques:

- Fewer clocks, which decreases the total current used by the clock trees
- Fast clocks for critical parts of the design and slow clocks for non-critical parts
- Fewer outputs switching in the design
- Further optimization of the design to use less logic
- Smaller load on the outputs by decreasing the capacitance
- 3.3V outputs instead of 5V

If there is flexibility in choosing the device, then the Ultra37000 family of CPLDs is a good choice if the design can run at 3.3V and/or has non-critical logic that may be run in a powered down logic block. In order for the logic block to run in lower power mode, a synthesis directive has to be included in *Warp* that instructs the software to output a JEDEC file that will program a specific logic block for low-power operation. The syntax of the directive in VHDL is: *low_power of my_design: entity is "a, b c"* where *my_design* is the name of the top-level entity, and *"a, b, c"* is a list of logic blocks which are to be powered down.

If you want all the logic blocks to run in low-power mode, you can set the Global Low Power Mode option in the Project -> Compiler Option menu.



If the above suggestions do not provide enough power reduction to help cool down the part, then forced air-cooling and/or heat sinking can provide the necessary heat dissipation. Please refer to our "Using Heat Sinks with Larger CPLDs" application note for more information.

Table 3. Θ_{JA} and Θ_{JC} Values

CPLD Part	Package	Θ_{JA} (C/W)	Θ_{JC} (C/W)
CY37032P44	44-Pin Thin Quad Flatpack	48	19
CY37032P44	44-Pin Plastic Leaded Chip Carrier	66	18
CY37064P44	44-Pin Thin Quad Flatpack	48	18
CY37064P44	44-Pin Plastic Leaded Chip Carrier	66	18
CY37064P44	44-Pin Ceramic Leaded Chip Carrier	69	8
CY37064P84	84-Pin Plastic Leaded Chip Carrier	42	17
CY37064P100	100-Pin Thin Quad Flatpack	34	8
CY37128P84	84-Pin Plastic Leaded Chip Carrier	42	17
CY37128P84	84-Pin Ceramic Leaded Chip Carrier	36	7
CY37128P100	100-Pin Thin Quad Flatpack	34	8
CY37128P160	160-Pin Thin Quad Flatpack	31	7
CY37192P160	160-Pin Thin Quad Flatpack	30	7
CY37256P160	160-Pin Thin Quad Flatpack	30	7
CY37256P160	160-Pin Ceramic Quad Flatpack	30	5
CY37256P160	160-Pin Ceramic Pin Grid Array	30	3
CY37256P208	208-Pin Plastic Quad Flatpack	30	16
CY37256P256	256-Pin Ball Grid Array	25	3
CY37384P208	208-Pin Plastic Quad Flatpack	29	15
CY37384P256	256-Pin Ball Grid Array	20	3
CY37512P208	208-Pin Plastic Quad Flatpack	29	15
CY37512P208	208-Pin E/Ceramic Quad Flatpack	20	5
CY37512P256	256-Pin Ball Grid Array	20	3
CY37512P352	352-Pin Ball Grid Array	20	3
CY7C371i	44-Lead Thin Plastic Quad Flat Pack	62	17
CY7C371i	44-Lead Plastic Leaded Chip Carrier	54	18
CY7C372i	44-Lead Plastic Leaded Chip Carrier	38	16
CY7C372i	44-Pin Thin Quad Flatpack	56	6
CY7C373i	84-Lead Plastic Leaded Chip Carrier	35	16
CY7C373i	100-Pin Thin Quad Flatpack	50	7
CY7C374i	84-Lead Plastic Leaded Chip Carrier	35	16
CY7C374i	100-Pin Thin Quad Flat Pack	29	5
CY7C374i	84-Pin Ceramic Leaded Chip Carrier	50	7
CY7C375i	160-Lead Thin Quad Flatpack	34	7
CY7C375i	160-Pin Grid Array	24	3
CY7C375i	160-Pin Ceramic Quad Flatpack	30	5

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LOGIC BLOCK A PLACEMENT   (16:20:35)

Messages:

_____________________________________________________________________________
          1111111111222222222233333333334444444444555555555566666666667777777777
01234567890123456789012345678901234567890123456789012345678901234567890123456789
_____________________________________________________________________________
| 0 |stout_9
XXXX++++++++++++.....................................................................
| 1 |UNUSED
......++++++++++++++.................................................................
| 2 |(oestat)
..........X++++++++++++++............................................................
| 3 |(ind2_q1)
..............X++++++++++++++.........................................................
| 4 |(oen)
..................X++++++++++++++.....................................................
| 5 |(dird0)
......................XX++++++++++++++.................................................
| 6 |stout_8
.........................XXXX++++++++++++.............................................
| 7 |(intm2)
.............................XX++++++++++++++.........................................
| 8 |stout_11
.................................XXXX++++++++++++.....................................
| 9 |(intm3)
.....................................XX++++++++++++++.................................
|10 |(dird1)
.........................................XX++++++++++++++.............................
|11 |(ind1_q1)
.............................................X++++++++++++++.........................
|12 |(ind3_q1)
...............................................X++++++++++++++.......................
|13 |(oen_end)
.................................................X++++++++++++++.....................
|14 |stout_10
.....................................................XXXX++++++++++++.................
|15 |(intm1)
...........................................................XX++++++++++++++...........
_____________________________________________________________________________

Total count of outputs placed        =  15
Total count of unique Product Terms  =  32
Total Product Terms to be assigned   =  32
Max Product Terms used / available   =  32 /  80   = 40.1  %
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Figure 1. Product Terms in *Warp* Report File

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DESIGN HEADER INFORMATION  (16:17:50)

Input File(s): test.pla
Device       : CY37256P160
Package      : CY37256P160-154AC
ReportFile   : test.rpt

Program Controls:
                None.

Signal Requests:
    GROUP LOW_POWER A
    GROUP FAST_SLEW ALL
    GROUP FLOAT stout_4 stout_5 stout_6 stout_7 busdat_0 busdat_1 busdat_2
          busdat_3 busdat_4 busdat_5 busdat_6 busdat_7 busdat_8 busdat_9
          busdat_10 busdat_11 busdat_12 busdat_13 busdat_14 busdat_15
    GROUP SOFT int_4
          carry3 carry2 carry1 carry0 clock3 clock2 clock1 clock0

Completed Successfully
```

Figure 2. Logic Block Lower Power Mode

Power Calculation Estimation Worksheet for FLASH370i and Ultra37000 Family (Single Clock Design)		
Supply current of a blank device	Icc_{Blank}	_____ mA
Coefficient of product term current draw (FullPower mode - Ultra37000 & FLASH370i)	$Kpt_{FullPower}$	_____ mA/pt
Coefficient of product term current draw (LowPower mode - Ultra37000)	$Kpt_{LowPower}$	_____ mA/pt
Number of product terms used in the device (FullPower mode - Ultra37000 & FLASH370i)	$Npt_{FullPower}$	_____
Number of product terms used in the device (LowPower mode - Ultra37000)	$Npt_{LowPower}$	_____
Internal DC supply current	Icc_{DC}	_____ mA
$Icc_{DC} = Icc_{Blank} + Kpt_{LowPower} * Npt_{LowPower} + Kpt_{FullPower} * Npt_{FullPower} + Icc_{Full-Power} * Nlb_{FullPower} + Icc_{LowPower} * Nlb_{LowPower}$		
Internal DC power (Vcc * Icc_{DC})	$Pint_{DC}$	_____ mW
Internal AC Power Calculation		
Coefficient of clock tree current draw	Kclk	_____ mA/MHz
Frequency of clock	fmax	_____ MHz
Coefficient of macrocell current draw	Kmc	_____ mA/pt
Average number of switching macrocells per cycle	Nmc	_____ pt/MHz
Internal AC supply current		
$Icc_{AC} = (Kclk + Kmc * Nmc) * fmax$	Icc_{AC}	_____ mA
Internal AC power (Vcc * Icc_{AC})	$Pint_{AC}$	_____ mW
External Power Calculation		
Number of outputs associated with the clock	N_{Out}	_____
Output capacitance load	C_{Load}	_____ µF
Frequency of Clock	fmax	_____ MHz
Ratio of toggling outputs to untoggling outputs	tog_{IO}	_____
I/O voltage	Vcc_{IO}	_____ V
External AC supply current	Iccext_AC	_____ mA
$Iccext\_AC = 1/2 * N_{Out} * C_{Load} * V_{Swing} * fmax * tog_{IO} * Vcc_{IO}$	Iccext_DC	_____ mA
External DC supply current	Icc_{EXT}	_____ mA
Total external supply current (Iccext_DC + Iccext_AC)	Pext	_____ mA
External power (Vcc * Icc_{EXT})		_____ mW
Total Power Estimation		
P_{TOTAL} ($Pint_{DC}$ + $Pint_{AC}$ + Pext)	P_{TOTAL}	_____ mW
Junction Temperature Calculation		
Junction-to-ambient thermal resistance	Θ_{JA}	_____ C/W
Ambient temperature	T_A	_____ C
Junction temperature ($\Theta_{JA} * P + T_{A)}$	T_J	_____ C

Power Calculation Estimation Worksheet for FLASH370i and Ultra37000 Family (Multiple Clock Design)		
Supply current of a blank device	Icc_{BLANK}	_____ mA
Coefficient of product term current draw (FullPower mode - Ultra37000 & FLASH370i)	$Kpt_{FullPower}$	_____ mA/pt
Coefficient of product term current draw (LowPower mode - Ultra37000)	$Kpt_{LowPower}$	_____ mA/pt
Number of product terms used in the device (FullPower mode - Ultra37000 & FLASH370i)	$Npt_{FullPower}$	_____
Number of product terms used in the device (LowPower mode - Ultra37000)	$Npt_{LowPower}$	_____
Internal DC supply current	Icc_{DC}	_____ mA
$Icc_{DC} = Icc_{Blank} + Kpt_{LowPower} * Npt_{LowPower} + Kpt_{FullPower} * Npt_{FullPower} + Icc_{FullPower} * Nlb_{FullPower} + Icc_{LowPower} * Nlb_{LowPower}$		
Internal DC power (Vcc * Icc_{DC})	$Pint_{DC}$	_____ mW
Internal AC Power Calculation		
Coefficient of clock tree current draw	Kclk	_____ mA/MHz
Frequency of operation for Clock 1	$fmax_{Clock\ 1}$	_____ MHz
Frequency of operation for Clock 2	$fmax_{Clock\ 2}$	_____ MHz
Frequency of operation for Clock 3	$fmax_{Clock\ 3}$	_____ MHz
Frequency of operation for Clock 4	$fmax_{Clock\ 4}$	_____ MHz
Average Frequency of operation for Product Term Clocks	$favg_{Clock\ PT}$	_____ MHz
Coefficient of macrocell current draw	Kmc	_____ mA/pt
Average number of switching macrocells per cycle for Clock 1	$Nmc_{Clock\ 1}$	_____ pt/MHz
Average number of switching macrocells per cycle for Clock 2	$Nmc_{Clock\ 2}$	_____ pt/MHz
Average number of switching macrocells per cycle for Clock 3	$Nmc_{Clock\ 3}$	_____ pt/MHz
Average number of switching macrocells per cycle for Clock 4	$Nmc_{Clock\ 4}$	_____ pt/MHz
Average number of switching macrocells per cycle for Product Term Clocks	$Nmc_{Clock\ PT}$	_____ pt/MHz
Internal AC supply current		
$Icc_{AC\ Clock\ 1} = (Kclk + Kmc * Nmc_{Clock\ 1}) * fmax_{Clock\ 1}$	$Icc_{AC\ Clock\ 1}$	_____ mA
$Icc_{AC\ Clock\ 2} = (Kclk + Kmc * Nmc_{Clock\ 2}) * fmax_{Clock\ 2}$	$Icc_{AC\ Clock\ 2}$	_____ mA
$Icc_{AC\ Clock\ 3} = (Kclk + Kmc * Nmc_{Clock\ 3}) * fmax_{Clock\ 3}$	$Icc_{AC\ Clock\ 3}$	_____ mA
$Icc_{AC\ Clock\ 4} = (Kclk + Kmc * Nmc_{Clock\ 4}) * fmax_{Clock\ 4}$	$Icc_{AC\ Clock\ 4}$	_____ mA
$Icc_{AC\ Clock\ PT} = (Kclk + Kmc * Nmc_{Clock\ PT}) * favg_{Clock\ PT}$	$Icc_{AC\ Clock\ PT}$	_____ mA
$Icc_{AC\ Total} = Icc_{AC\ Clock\ 1} + Icc_{AC\ Clock\ 2} + Icc_{AC\ Clock\ 3} + Icc_{AC\ Clock\ 4} + Icc_{AC\ Clock\ PT}$	$Icc_{AC\ Total}$	_____ mA
Internal AC power (Vcc * $Icc_{AC\ Total}$)	$Pint_{AC}$	_____ mW
External Power Calculation		
Number of outputs associated with Clock 1	$N_{Out\ Clock\ 1}$	_____
Number of outputs associated with Clock 2	$N_{Out\ Clock\ 2}$	_____
Number of outputs associated with Clock 3	$N_{Out\ Clock\ 3}$	_____
Number of outputs associated with Clock 4	$N_{Out\ Clock\ 4}$	_____
Number of outputs associated with Product Term Clock(s)	$N_{Out\ Clock\ PT}$	_____
Output capacitance load for Clock 1 outputs	$C_{Load\ Clock\ 1}$	_____ µF
Output capacitance load for Clock 2 outputs	$C_{Load\ Clock\ 2}$	_____ µF
Output capacitance load for Clock 3 outputs	$C_{Load\ Clock\ 3}$	_____ µF
Output capacitance load for Clock 4 outputs	$C_{Load\ Clock\ 4}$	_____ µF

Power Calculation Estimation Worksheet for FLASH370i and Ultra37000 Family (Multiple Clock Design) (continued)		
Output capacitance load for Product Term Clock(s) outputs	$C_{Load\ Clock\ PT}$	_____ µF
Frequency of Clock 1	$fmax_{Clock\ 1}$	_____ MHz
Frequency of Clock 2	$fmax_{Clock\ 2}$	_____ MHz
Frequency of Clock 3	$fmax_{Clock\ 3}$	_____ MHz
Frequency of Clock 4	$fmax_{Clock\ 4}$	_____ MHz
Average Frequency of Product Term Clock(s)	$favg_{Clock\ PT}$	_____ MHz
Ratio of toggling outputs to untoggling outputs	tog_{IO}	_____
I/O voltage	Vcc_{IO}	_____ V
External AC supply current		
$Iccext\_AC_{Clock\ 1}=1/2 * N_{Out\ Clock\ 1} * C_{Load\ Clock\ 1} * V_{Swing} * fmax_{Clock\ 1} * tog_{IO} * Vcc_{IO}$	$Iccext\_AC_{Clock\ 1}$	_____ mA
$Iccext\_AC_{Clock\ 2}=1/2 * N_{Out\ Clock\ 2} * C_{Load\ Clock\ 2} * V_{Swing} * fmax_{Clock\ 2} * tog_{IO} * Vcc_{IO}$	$Iccext\_AC_{Clock\ 2}$	_____ mA
$Iccext\_AC_{Clock\ 3}=1/2 * N_{Out\ Clock\ 3} * C_{Load\ Clock\ 3} * V_{Swing} * fmax_{Clock\ 3} * tog_{IO} * Vcc_{IO}$	$Iccext\_AC_{Clock\ 3}$	_____ mA
$Iccext\_AC_{Clock\ 4}=1/2 * N_{Out\ Clock\ 4} * C_{Load\ Clock\ 4} * V_{Swing} * fmax_{Clock\ 4} * tog_{IO} * Vcc_{IO}$	$Iccext\_AC_{Clock\ 4}$	_____ mA
$Iccext\_AC_{Clock\ PT}=1/2 * N_{Out\ Clock\ PT} * C_{Load\ Clock\ PT} * V_{Swing} * fmax_{Clock\ PT} * tog_{IO} * Vcc_{IO}$	$Iccext\_AC_{Clock\ PT}$	_____ mA
$Iccext\_AC_{Total} = Iccext\_AC_{Clock\ 1} + Iccext\_AC_{Clock\ 2} + Iccext\_AC_{Clock\ 3} + Iccext\_AC_{Clock\ 4}$	$Iccext\_AC_{Total}$	_____ mA
External DC supply current	Iccext_DC	_____ mA
Total external supply current (Iccext_DC + Iccext_AC)	Icc_{EXT}	_____ mA
External power ($Vcc * Icc_{EXT}$)	Pext	_____ mW
Total Power Estimation		
P_{TOTAL} ($Pint_{DC} + Pint_{AC} + Pext$)	P_{TOTAL}	_____ mW
Junction Temperature Calculation		
Junction-to-ambient thermal resistance	Θ_{JA}	_____ C/W
Ambient temperature	T_A	_____ C
Junction temperature ($\Theta_{JA} * P + T_A$)	T_J	_____ C

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