ADVANCE INFORMATION

CY7C9536

Packet over SONET/SDH IC - POSIC™

Features

- **OC-48/STS-48/STM-16, OC-12/STS-12/STM-4, OC-3/STS3/STM-1 rates, Concatenated and Non-concatenated**
  - **Complies with ITU-Standards G.707/Y.1322 & G.783**
  - **Complies with Bellcore GR253 rev.1, 1997**
  - **Channelized operation: Supports 16xOC-3 and 4xOC-12 within OC48 stream**
- **Virtual Concatenation enables secure and dedicated bandwidth provisioning**
  - **Up to 16 channels**
  - **From 100 Mbps to 1.2 Gbps bandwidth per channel**
  - **STS-1 and STS-3c granularity**
- **Full duplex mapping of ATM cells over SONET/SDH**
  - **Complies with ITU-Standards I 432.2**
- **Full duplex mapping of packet-over-SONET/SDH: IETF RFC 1619/1662/2615 (PPP)**
- **Generic Protocol Framer delineates packets/frames with length-CRC frame construct**
  - **Simple Data Link (SDL)- IETF RFC2823**
  - **Generic Framing Protocol (GFP) per ANSI T1X1.5**
  - **Cypress Hybrid Data Transport (HDT)**
- **User-programmable encapsulation**
- **User-Programmable clear channel transport**
- **User-programmable SONET/SDH bypass**
- **Programmable Frame Tagging Engine, for packet pre-classification, enables features such as:**
  - **MPLS label lookup and tagging**
  - **PPP: LCP and NCP tagging**
  - **PPP Control packets optionally sent to host CPU interface**
  - **MAC/layer 3 address look up & tagging**
- **Programmable A1A2 processing bypass in Rx direction with frame sync input**
- **Complete SOH, LOH and POH processing**
- **APS extraction, CPU interrupt generation and programmable insertion of APS byte**
- **Line side APS port interface**
- **Provision for protection switching on SONET/ SDH port**
- **Programmable PRBS generator and receiver**
- **Serial port to access line/section Data Communication Channel (DCC) & Voice Communication Channel (VCC)**
- **Full duplex UTOPIA/POS-PHY level 3 or HBST interface**
- **16-bit/32-bit Host CPU interface bus**
- **JTAG & Boundary Scan**
- **Glueless interface with Cypress CY7B9532V OC-48 PHY**
- **0.18µ CMOS, 504-pin BGA package**
- **+1.8V for core, +3.3V for i/o, +1.5V for HSTL i/o supply and +0.75V reference**

Applications

- Multi-service nodes
- ATM switches and routers
- Packet routers
- Multi service routers
- SONET/SDH/add-drop mux for packet/data applications
- SONET/SDH/ATM/POS test equipment

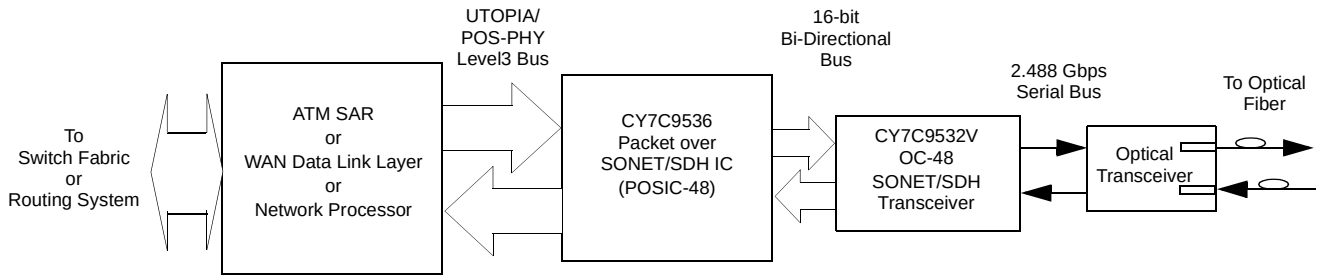
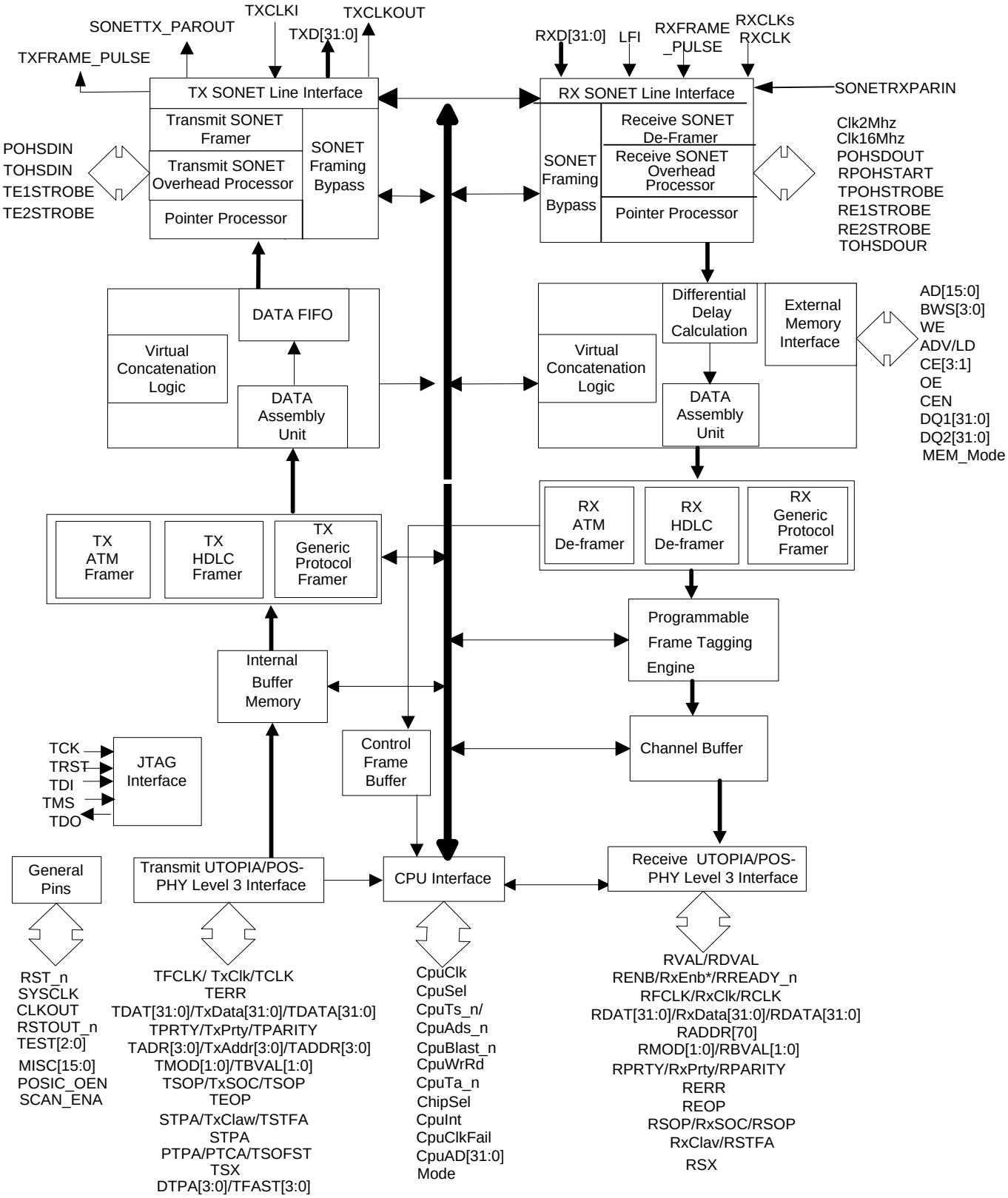


Figure 1. POSIC™ System Application Diagram

Block Diagram



Overview

The CY7C9536 (POSIC™) is a highly integrated SONET/SDH framer device for transport of ATM and IP Packets over SONET/SDH links. It features special functions and architecture to support next-generation optical networking protocols for both SONET/SDH and direct data-over-fiber networks. UTOPIA/POS-PHY (Level 3) and HBST interfaces are provided on the system side.

POSIC performs complete Section Overhead (SOH), Line Overhead (LOH) and Path Overhead (POH) processing. Complete access to all overhead bytes is provided through register access via the host CPU interface. Access to selected overhead bytes also available through serial port. Optional frame sync input and Transport Overhead (TOH) bypass enables better interface with STS-1 switched streams.

The virtual concatenation feature, with up to 16 channels, enables provisioning of secure, dedicated and right-sized bandwidth for Ethernet or ATM transport. Up to 16 virtual channels can be created with STS-1 or STS-3c granularity. Bandwidth from 100 Mbps to 1.2 Gbps can be allocated per channel.

POSIC supports packet-over-SONET/SDH as PPP in HDLC-like frame as per IETF rfc 1619/1662/2615 (PPP). POSIC also supports full duplex ATM over SONET/SDH transport in compliance with ITU I432.2.

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The Generic Optical Networking Protocol Framer features wire rate framing, frame delineation and deframing with length-CRC pair header construct. Optional payload scrambling/descrambling and payload FCS also provided. This enables POSIC to support many new generation protocols like SDL, GFP and HDT over SONET/SDH.

Clear channel mode enables transport of TDM traffic on selected virtual channels, while the rest of the channels are transporting data through any one of framing / encapsulation engines. Clear channel mode can also be used to transport raw byte streams.

The Programmable Frame Tagging Engine enables wire rate tagging of packets/frames. For new generation networking features such as MPLS, this engine can be programmed to tag based on existence/lack of specific label/field values, in the first 64 bytes of each packet. This way, packets are tagged for a variety of conditions, all programmable by the user, enabling sorting of packets in the incoming data stream and buffering packets accordingly. In a PPP application, control packets can optionally be sent over the host CPU interface directly.

SONET/SDH bypass mode allows use of this device for data transport in non SONET/SDH point-to-point and mesh optical networks

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106799	05/03/01	PLZ	New short form of CY7C9536 Data Sheet. Extracted from Spec number 38-02004