PRELIMINARY **CY7C955**

AX™ ATM-SONET/SDH Transceiver

Features

- **WAN and LAN ATM physical layer device**
- **Provides complete physical layer transport of ATM cells at:**
  - **— STS–3c/ STM–1 rate of 155.52 MHz**
  - **— STS–1 rate of 51.84 MHz**
- **Compliant with ATM Forum User Network Interface 3.1 specification**
- **UTOPIA ATM interface**
- **ATM cell processing including:**
  - **— HEC generation/verification**
  - **— Cell scrambling/descrambling**
  - **— Rate adaption/idle cell filtering**
  - **— Local Flow Control**
  - **— Cell alignment**
- **SONET frame processing including:**
  - **— Compliant with Bellcore GR–253, I.432, T1.105, and G.709 for Jitter Tolerance and Jitter Generation**
  - **— Frame generation/recovery**
  - **— SONET scrambling/descrambling**
  - **— Frequency justification/pointer processing**
- **Complete line interface including:**
  - **— Clock and data recovery**
  - **— Transmit timing derived from receiver or byte-rate source**
  - **— SONET compliant PLL**
  - **— 100K PECL compatible I/O**
- **Alarm indications including:**
  - **— Loss Of Signal**
  - **— Out Of Frame, Loss Of Frame**
  - **— Line Far End Receive Failure**
  - **— Line Alarm Indication Signal**
  - **— B1 Parity Error**
  - **— Loss Of Cell Alignment**
  - **— Loss Of Receive Data**
- **Controller interface for internal interrupt and configuration registers including:**
  - **— Error monitoring**
  - **— Status indication**
  - **— Device configuration**
- **0.65µ Low Power CMOS**
- **128-pin PQFP**

Functional Description

The Cypress Semiconductor CY7C955 is a Transceiver chip designed to carry ATM cells across SONET/SDH systems.

On the transmit side, ATM cells coming from the Utopia interface are being mapped into SONET/SDH frames and then serialized for transmission over fiber or twisted pair (through an optical module or an equalizer chip).

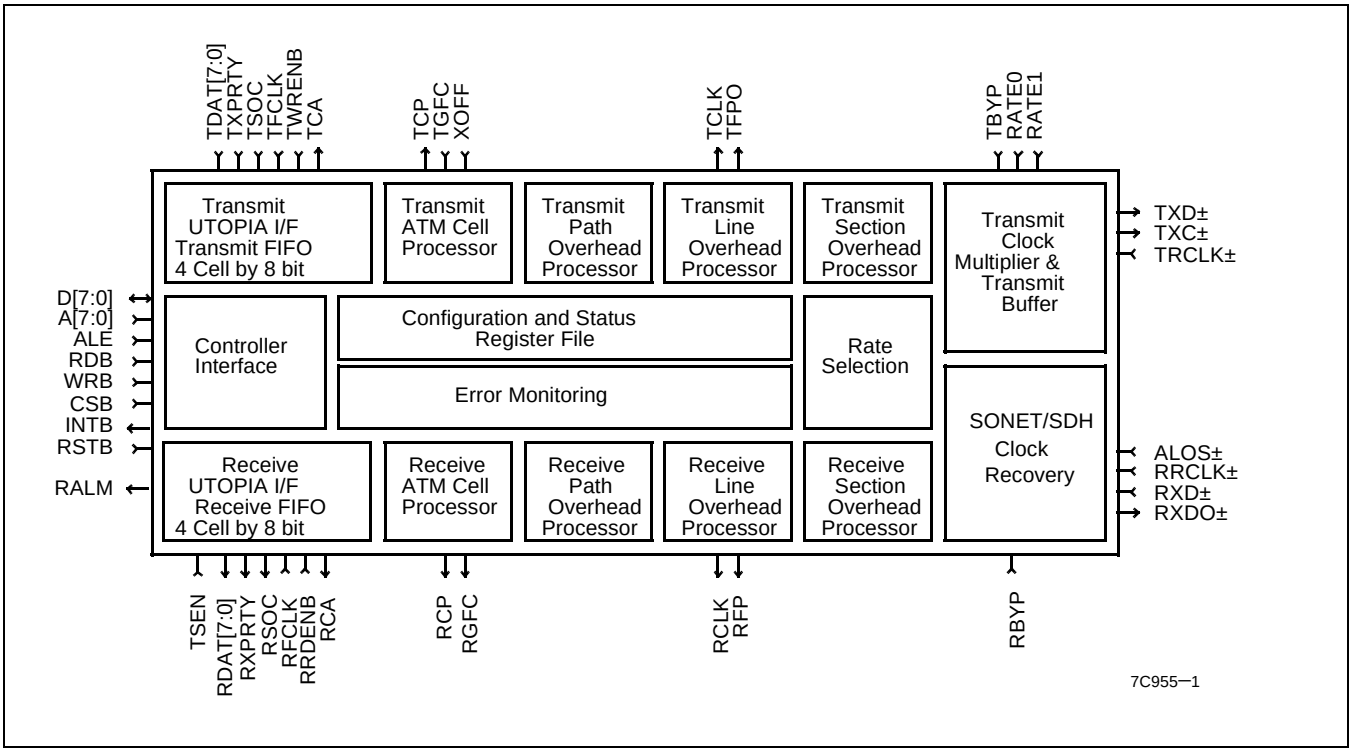
On the receive side, serial SONET/SDH datastreams coming from an optical module or an equalizer chip are being recovered by the intergrated clock and data recovery phase-locked loop, framed, processed, and presented as parallel ATM cells on the Receive Utopia Interface.

The CY7C955 can be used in a Network Interface Card (NIC) design to connect the segmentation and Reassembly (SAR) chip to the optical modules or equalizer chip.

The CY7C955 can also be used in work group or enterprise switches to connect the I/O FIFOs of the switch fabric to the optical module or equalizer in the interface boards.

The applications of the CY7C955 include adapters, switches, routers, hubs, and proprietary systems.

TABLE OF CONTENTS



Pin Descriptions

CY7C955 ATM-SONET/SDH Transceiver

Transmit Utopia Interface

Name	Pin	I/O	Description
TDAT[7:0]	87–94	Input	Transmit Utopia data: Byte-wide data driven from the ATM to PHY layer. TDAT[7] is the MSB.
TPRTY	95	Input	Transmit Utopia Data Parity: Data parity calculated over TDAT[7:0]. Odd parity is assumed unless the TXPTYP bit (Reg–63, bit 7) is set to even parity
TSOC	96	Input	Transmit Utopia Start of Cell: Assert TSOC HIGH when TDAT[7:0] contains the first byte of an ATM cell. If TSOC is asserted sooner than 53 writes after the previous SOC, an error condition will be generated. This input is optional after the first TSOC pulse.
TFCLK	84	Input	Transmit Utopia Clock: Data transfer clock. Data is transferred to the AX on the rising edge of TFCLK when TWRENB is asserted (LOW).
TWRENB	85	Input	Transmit Utopia Data Enable: Enables the TFCLK input for data transfer to the AX. This signal is active LOW.

Transmit Utopia Interface (continued)

Name	Pin	I/O	Description
TCA	86	Output	Transmit Utopia Cell Available: An active state on this signal indicates that the Transmit FIFO can accept at least N more cells (53 octets) of data where N and the active state of the signal (HIGH or LOW) are programmable through the configuration registers (Reg–63H and Reg–01H). In a special case, if Reg–63H bit2–3 is set to 00, Reg–01H, bit 3 is set to 0, and TCALEVEL0 (Reg–63H, bit 1) set to 0. TCA will behave as an active HIGH FULL indicator.

Transmit ATM Interface

Name	Pin	I/O	Description
XOFF	50	Input	Transmit Idle Cell: A HIGH state on this pin will force the ATM Cell Processor to send an IDLE cell even if there are cells to send in the Transmit FIFO. XOFF is an asynchronous input and has an integrated pull down resistor.
TGFC	52	Input	Transmit Generic Flow Control: This bit serial input provides the ability to overwrite the four bits of the ATM cell header GFC field. These bits may be optionally written during the four TCLK clock periods following the assertion of the TCP output.
TCP	51	Output	Transmit Start Of GFC: This indicates that the first bit of the GFC for the next cell read from the Transmit FIFO is expected on the TGFC pin during the next rising edge of TCLK.

Transmit Clock Generator

Name	Pin	I/O	Description
TRCLK±	9–10	Differential In	Transmit Input Clock: Accepts either a differential PECL, or a TTL or a CMOS byte rate reference connected to TRCLK– with TRCLK+ grounded for the Transmit frequency multiplier PLL. Optionally, this input can accept also the bit rate reference when TBYP is true (held HIGH). In this mode the Transmit frequency multiplier is bypassed and the bit rate clock is used directly for transmit side clocking.
TXC±	13–14	Differential Out	Transmit Output Clock: Provides clock output for the transmit data. TXD± is updated on the falling edge of this signal. In the default setting, TXC is disabled if RATE0 is HIGH and a 51.84-MHz clock if RATE0 is LOW. XORTXC (Reg–04H, bit 6) can be used to invert the default setting such that TXC is a 155.52-MHz clock if RATE0 is HIGH and is disabled when RATE0 is LOW.
TXD±	15–16	Differential Out	Transmit Data Output: Accepts NRZ encoded output data. This signal is updated on the falling edge of TXC±.
TBYP	2	Input	Transmit Clock Bypass: When this input is held HIGH the transmit frequency multiplier is disabled and TRCLK± input is used directly for transmit side clocking. When this input is held LOW the transmit frequency multiplier multiplies the TRCLK± input by 8, 24, or 8/3 (depending on the TREFSEL (Reg–06H, bit 0) setting to provide the internal bit rate clock.
RATE0 RATE1	97–98	Input	RATE: When the RATE0 input is HIGH the Transmit frequency generator and the Receive clock recovery are selected to operate at the STS–3c/STM–1 rate of 155.52 MHz. When the RATE0 pin is LOW, the Transmit frequency generator and the Receive clock recovery are selected to operate at the STS–1 rate of 51.84 MHz. RATE1 is for factory testing use only and should be tied HIGH. Both RATE0 and RATE1 have integrated pull-up resistors.
TCLK	54	Output	Transmit Byte Reference: Byte rate reference clock derived from the transmit line bit rate.
TFPO	53	Output	Transmit Frame Reference. This signal is an 8-kHz frame rate reference that goes HIGH during the transmission of the first A1 byte of the SONET/SDH frame. TFPO is updated by the rising edge of TCLK.

Receive Clock Recovery

Name	Pin	I/O	Description
RXD±	25–26	Differential In	Receive Input Data: These line receiver inputs are connected to an internal Receive PLL that recovers the embedded clock and data information. The incoming data rate can be within one of two frequency ranges depending on the state of the RATE0 pin.

Receive Clock Recovery (continued)

Name	Pin	I/O	Description
RXDO±	22–23	Differential Out	Receive Output Data: These differential outputs represent the retimed version of the input data stream (RXD±) in normal mode and the buffered version of the input datastream (RXD±) in bypass mode. This output pair can be used as inputs to decision feedback equalizers to correct for baseline wander. RXDO can be turned off to save power by setting RXDOD (Reg–04H, bit 7) to 1.
RRCLK±	33–34	Differential In	Receive Clock: These inputs are used to clock in the differential data (RXD±) when the Receive clock recovery block is bypassed (RBYP=HIGH). If RBYP is LOW, RRCLK is multiplied by 8, 24, or 8/3 depending on the setting of RREFSEL (Reg–07H, bit 0) and use as a reference for the Receiver PLL. Refer to the section on “Interface Termination and Bias of Schemes” for connection examples to these pins.
RBYP	41	Input	Receive Clock Bypass: When this input is HIGH the Receiver clock recovery block is bypassed. In this mode the device does not recover clock and data from the Receive input data stream (RXD±) but instead uses the RRCLK± inputs to clock the differential data into the device. When this input is LOW the Receiver clock recovery block recovers the clock and data from the input data stream. In this mode a byte-rate clock is expected on the RRCLK± inputs.
RCLK	57	Output	Receive Byte Reference: Provides a byte-rate reference derived from the recovered bit- rate Receive clock. RALM, RCP, and RGFC are aligned with this clock.
RFP	58	Output	Receive Frame Reference: This output provides a frame-rate reference clock aligned to the SONET/SDH frame alignment bytes. RFP will pulse HIGH for one RCLK cycle every 125 seconds even at OOF and LOF situations.
LF+	42	Input	NC. This pin is for factory testing only.
LF–, LFO	43, 44	Input	These are the PLL filter pins. Connect a 0.47-µF capacitor across LF– and LFO.

Receive ATM Interface

Name	Pin	I/O	Description
RGFC	59	Output	Receive Generic Flow Control: This output provides the four bits of the current ATM cell header GFC locations at each successive RCLK pulse. The RCP output indicates the first GFC bit location. This output is forced LOW if the ATM Cell Processor has lost cell delineation.
RALM	63	Output	Receive Interrupt: This active HIGH signal is aligned with the RCLK byte-rate clock and signals the presence of LAIS, PAIS, LOS, LOF, LOP, or LCD.
RCP	60	Output	Receive Start Of GFC: This output indicates the first bit of the GFC presented on the RGFC output. This output goes HIGH for 1 RCLK cycle 6 byte times after the corresponding cell is written into the Receive FIFO.

Receive Utopia Interface

Name	Pin No	I/O	Description
RDAT[7:0]	70–71 74–79	Output	Receive Utopia Data: Byte-wide data driven from the PHY to ATM layer. RDAT[7] is the MSB
RPRTY	82	Output	Receive Utopia Data Parity: Data parity calculated over RDAT[7:0]. Odd parity is assumed unless the TXPRTY bit is set to even parity by Reg–50H, bit 6.
RSOC	83	Output	Receive Utopia Start of Cell: Asserted HIGH when RDAT[7:0] contains the first byte of an ATM cell.
RFCLK	67	Input	Receive Utopia Clock: Data transfer clock. Data is transferred from the AX on the rising edge of RFCLK when RRDENB is asserted (LOW).
RRDENB	68	Input	Receive Utopia Enable: Enables the RFCLK input for data transfers from the AX.
RCA	69	Output	Receive Utopia Cell Available: An active signal indicates that the Receive FIFO contains at least 1 or 4 more bytes of data. RCA is controlled by RCAINV (Reg–01H, bit 2) and RCALEVEL0 (Reg–59H, bit 2).

Receive Utopia Interface (continued)

Name	Pin No	I/O	Description
TSEN	66	Input	Receive Output Enable: This output operates in conjunction with the RRDENB output. When TSEN is HIGH and RRDENB is HIGH the Receive UTOPIA data bus (RDAT[7:0], RPRTY, and RSOC) is three-stated. When TSEN is HIGH and RRDENB is LOW the data bus is driven with the requested data. When TSEN is LOW the data bus will not three-state.

Controller Interface

Name	Pin No	I/O	Description
D[7:0]	110–112 115–118	I/O	Data[7:0]: Bidirectional data bus used to transfer data to and from the internal configuration, status, and error monitoring registers.
A[7:0]	119–126	Input	Address[7:0]: Address bus used to select the internal register for reading or writing.
ALE	127	Input	Address Latch Enable: When this input is LOW the address is latched from the A[7:0] inputs. When this input is HIGH, the input is transparent. ALE has an integrated pull-up resistor.
RDB	105	Input	Read: This active LOW signal is used to read the internal register. The AX drives D[7:0] when RDB and CSB are both LOW.
WRB	104	Input	Write: This active LOW signal is used to write the internal registers. Data is latched into the specified address register on the rising edge of WRB when CSB is LOW.
CSB	100	Input	Select: This active LOW device select has to be enabled during register accesses.
INTB	108	Output	Interrupt: This active LOW open drain output transitions LOW when an unmasked interrupt source is active. This output transitions HIGH when the appropriate register has been read. This interrupt signals the most critical error states of the device including Loss of Pointer, Line Alarm Indication Signal (LAIS), Line Far End Receive Failure (LFERF), Loss of Frame (LOF), Out of Frame (OOF), Loss of Signal (LOS), and many others.
ALOS±	27–28	Differential In	Carrier Detect: This differential input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at a Logic Low, the input data stream (RXD±) is recovered normally by the Receive Clock Recovery PLL. When this input is at a Logic High, the Receive PLL no longer aligns to RXD±, but instead aligns with the RRCLK * 8 frequency and the LOS alarm register (RDOOLV) will be set. Besides differential PECL, the ALOS– input can be set to accept single ended PECL input if ALOS+ is tied to GND. ALOS– has to be decoupled.
RSTB	101	Input	Reset: This active LOW signal provides a device reset. This line can be pulled LOW to put the CY7C955 into the power-down mode. RSTB has an integrated pull-up resistor.
VCLK	99	Input	Factory test pin. Must be LOW for normal operation. VCLK has an integrated pull-down resistor.

Transmit Power

Name	Pin No	I/O	Description
TXVDD	12	Power	The Transmit Pad Power supplies the TXD± outputs. TXVDD is physically isolated from the other device power pins and should be well regulated +5V DC and noise-free for good performance when driving category 5 unshielded twist pair cabling.
TAVD1	4	Power	The power pin for the transmit clock synthesizer reference circuitry. TAVD1 should be connected to analog +5V.
TAVD2	6	Power	The power pin for the transmit clock synthesizer oscillator. TAVD2 should be connected to analog +5V.
TAVD3	8	Power	The power pin for the transmit PECL inputs. TAVD3 should be connected to analog +5V.
TVDDO	18	Power	Power for TXC± and RXDO±.

Receive Power

Name	Pin No	I/O	Description
RAVD1	30	Power	The power pin for receive clock and data recovery block reference circuitry. RAVD1 should be connected to analog +5V.
RAVD2	36	Power	The power pin for receive clock and data recovery block active loop filter and oscillator. RAVD2 should be connected to analog +5V.
RAVD3	24	Power	The power pin for the RXD± and ALOS± PECL inputs. RAVD3 should be connected to analog +5V.
RAVD4	32	Power	The power pin for the RRCLK± PECL inputs. RAVD4 should be connected to analog +5V.

Core Power

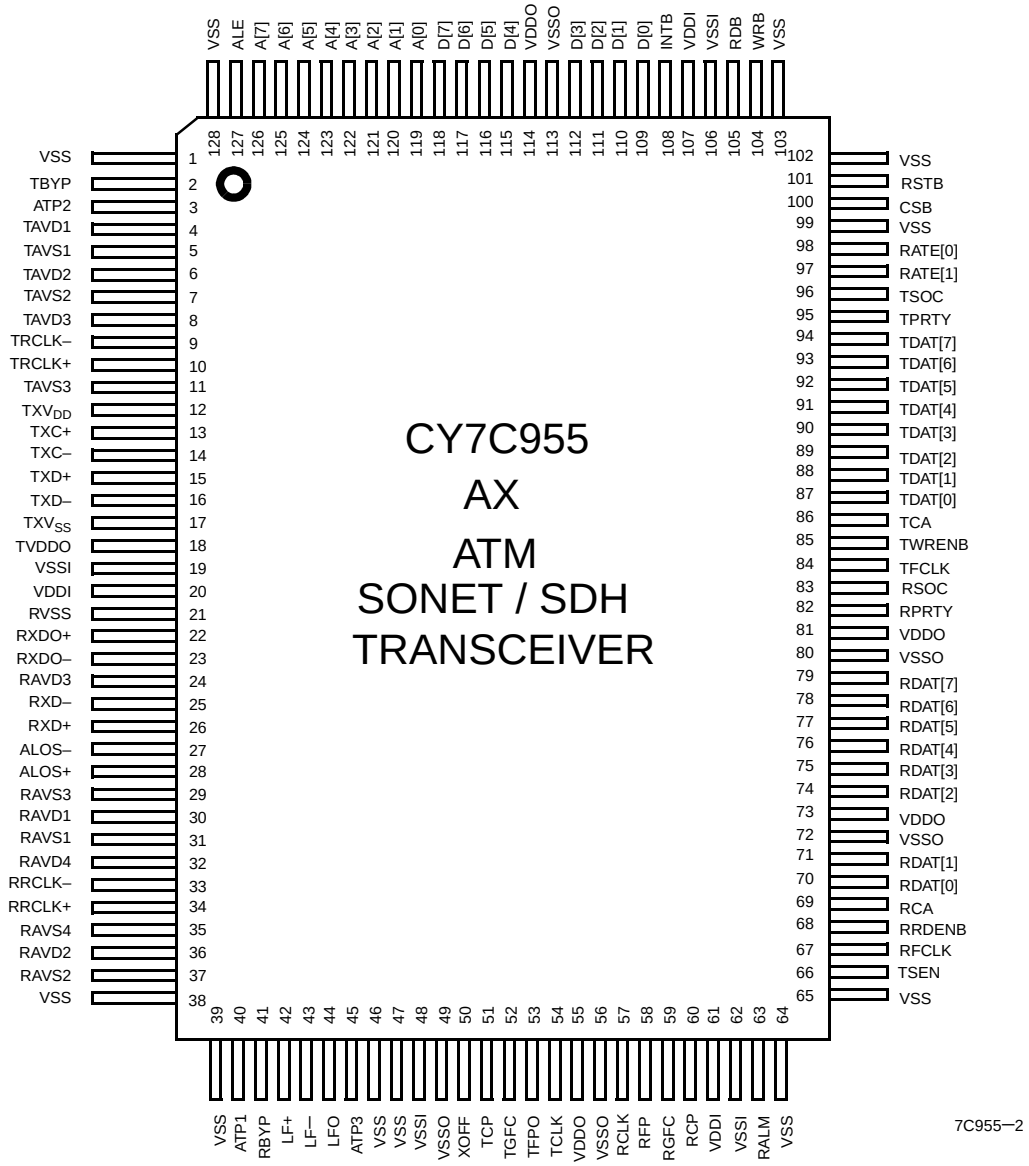
Name	Pin No	I/O	Description
V_{DDI}	20, 61, 107	Power	The core power pins should be connected to a well decoupled +5V DC in common with V_{DDO}.
V_{DDO}	55, 73, 81, 114	Power	The pad ring power pins should be connected to a well decoupled +5V DC in common with V_{DDI}.

Ground

Name	Pin No	I/O	Description
TAVS1	5	Ground	The ground pin for the transmit clock synthesizer reference circuitry. TAVS1 should be connected to analog GND.
TAVS2	7	Ground	The ground pin for the transmit clock synthesizer oscillator. TAVS2 should be connected to analog GND.
TAVS3	11	Ground	The ground pin for the transmit PECL inputs. TAVS3 should be connected to analog GND.
TXV_{SS}	17	Ground	The transmit pad ground is the return path for the TXC± and TXD± outputs. TXV_{SS} is physically isolated from the other device ground pins and should be noise-free for good performance when driving category 5 unshielded twisted pair cabling.
RAVS1	31	Ground	The ground pin for receive clock and data recovery block reference circuitry. RAVS1 should be connected to analog GND.
RAVS2	37	Ground	The ground pin for receive clock and data recovery block active loop filter and oscillator. RAVS2 should be connected to analog GND.
RAVS3	29	Ground	The ground pin for the RRCLK± PECL inputs. RAVS3 should be connected to analog GND.
RAVS4	35	Ground	The ground pin for the RSD± and ALOS± PECL inputs. RAVS4 should be connected to analog GND.
RVSSO	21	Ground	This pin is grounded for TXC± and RXDO±.
V_{SSI}	19, 62, 106,48	Ground	The core ground (V_{SSI}) pins should be connected to GND in common with V_{SSO}.
V_{SSO}	56, 72, 80, 113, 49	Ground	The pad ring ground (V_{SSO}) pins should be connected to GND in common with V_{SSI}.
V_{SS}	1, 38, 39, 46, 47, 64, 65, 102, 103, 128	Ground	These pins must be connected to GND for correct operation.
ATP1, ATP2, ATP3	40, 3, 46	I/O	These Analog Test Points (ATPx) are for factory testing use only. These pins have to be tied to GND for correct chip operation.

Pin Configuration

128-pin PQFP
Top View



7C955—2

Description

Transmit Section

Transmit Utopia Interface (TUI)

The transmit interface provides a simple access from the external environment to the ATM Transceiver. The operation of this interface is compliant with the Utopia interface specification. The interface provides a 9-bit by 4-cell FIFO to decouple the system interface from the ATM physical layer timing. 9-bit words are clocked into the device through a clocked FIFO system interface. These 9 bits include an 8-bit data word along with a Start Of Cell (SOC) indication. The interface also provides full and almost full indications (TCA). Maximum clock rate for this interface is 33 MHz.

Transmit ATM Cell Processor (TACP)

The ATM cell processor provides HEC generation, idle/unassigned cell header modification, payload scrambling, and GFC insertion.

HEC Generator

The Header Error Check (HEC) code is contained in the last byte of the ATM cell header and is capable of single error correction and multiple error detection. When optionally generated, the Transmit ATM Cell Processor calculates a CRC–8 over the first four bytes of the ATM cell header using the polynomial $x^8 + x^2 + x + 1$. The coset $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the residue of this function. The HEC is calculated in accordance with ANSI T1.624–1993 and CCITT Recommendation I.432. This HEC sequence is placed in the 5th byte of the ATM cell header.

Idle/Unassigned Cell Header Modification

Idle (Unassigned) cells are sent by the ATM cell processor whenever a complete cell is not contained within the Transmit FIFO. This transforms the non-continuous cell input stream into a continuous stream of assigned and unassigned cells.

The ATM cell processor provides the ability to overwrite the Generic Flow Control (GFC), the Payload Type Indication (PTI), and the Cell Loss Priority (CLP) fields of Idle (Unassigned) cells with the values contained in the corresponding configuration registers. VPI and VCI are set to zero in Idle (Unassigned) cells.

Payload Scrambler

The 48 bytes of the ATM payload are scrambled using a parallel implementation of the polynomial $x^{43} + 1$ as described in CCITT Recommendation I.432. The scrambler can be optionally deselected.

GFC Insertion

The transmitted GFC field of an ATM cell can be derived from different sources. For assigned cells, the default is from pins TDAT[7:0]. For Idle (Unassigned) cells, the default is from GFC[3:0] (Reg–61H, bit 7–bit 4). However, if any bit of TGFCE[3:0] (Reg–67H, bit 7–bit4) is set, the corresponding transmitted GFC location will instead be taken from the serial TGFC (pin 52) input following the functional timing specifications described in the section on Transmit GFC Serial Link Interface.

Transmit SONET Path Overhead Processor (TPOP)

The SONET path overhead processor provides payload pointer alignment (H1, H2), path overhead insertion, and insertion of the Synchronous Payload Envelope (SPE). ATM cells (both assigned and unassigned) are inserted into the SPE for transmission in the SONET frame

SONET Overhead Insertion

The SONET/SDH STS–3c/STM–1 frame structure is shown in *Figure 1* and the SONET STS–1 frame structure is shown in *Figure 2*. The SONET frame occurs once every 125 µs and is transmitted beginning with the A1 bytes, followed by the A2 bytes, C1 bytes, 261 bytes (87 bytes for STS–1) of the Synchronous Payload Envelope (SPE), B1 bytes, etc., until the entire frame is transmitted.

The TPOP generates the H1 and H2 bytes that indicate the beginning of the SPE and the H4 byte that indicates the ATM cell offset within the SPE. The default initial value for H1 and H2 pointer is 522, meaning that the first byte of the SPE (J1) corresponding to a frame actually starts after the C1 byte of the next frame.

In the default case described above, a 6h is present in the New Data Flag (NDF) portion of the first H1 (bits 0–4), a 2h is present in bits 5–7 and a 0Ah is present in the first H2 byte. The remaining H1 bytes for STS–3c/STM–1 are set to 93h and the remaining H2 bytes are set to FFh which is the concatenation indication for the J1 pointer. The Pointer Action byte, H3, is set to 00h. During Path AIS all of the H1 and H2 bits are set to 1.

The STS path trace J1 is set to all zeros. The path BIP–8 (B3) byte provides path error monitoring. This function calculates the bit-interleaved parity-8 code using even parity over the previous SPE before scrambling and is inserted into the current B3 byte before scrambling. Bit-interleaved parity-8 forces the number of 1s in the xth bit of every byte in the previous SPE plus the xth bit of the B3 byte in the current SPE to be an even number.

The path signal level indicator, C2, defaults to 13h.

The path status, G1, has several functions. Bits 1 through 4 are used to indicate Far End Block Errors (FEBE) derived by counting the number of BIP–8 errors occurred in the last frame received. Valid codes are 0 through 8. If more than 8 errors have accumulated since the last, frame the maximum value is sent with the current frame, the FEBE counter is decremented by 8, and the remaining errors are sent with the next frame. FEBE may be inserted through register control for diagnostic purposes. Bits 1 through 4 can also be used to transmit Far End Receive Failures by setting these bits to 9 (1001). This error indicates to the far end that cell delineation has been lost. Bit 5 can be used to generate a yellow alarm condition. The default value for this bit is 0 (no alarm).

The multi-frame indicator, H4, is used to indicate the first ATM cell and may take on values of 00 to 34h.

The remaining bytes, F2, Z3, Z4, and Z5, are not used by the SONET path processing and are set to 00h upon transmission. When operating in STS–1 mode, SPE columns 30 and 59 can be configured as fixed stuff columns.

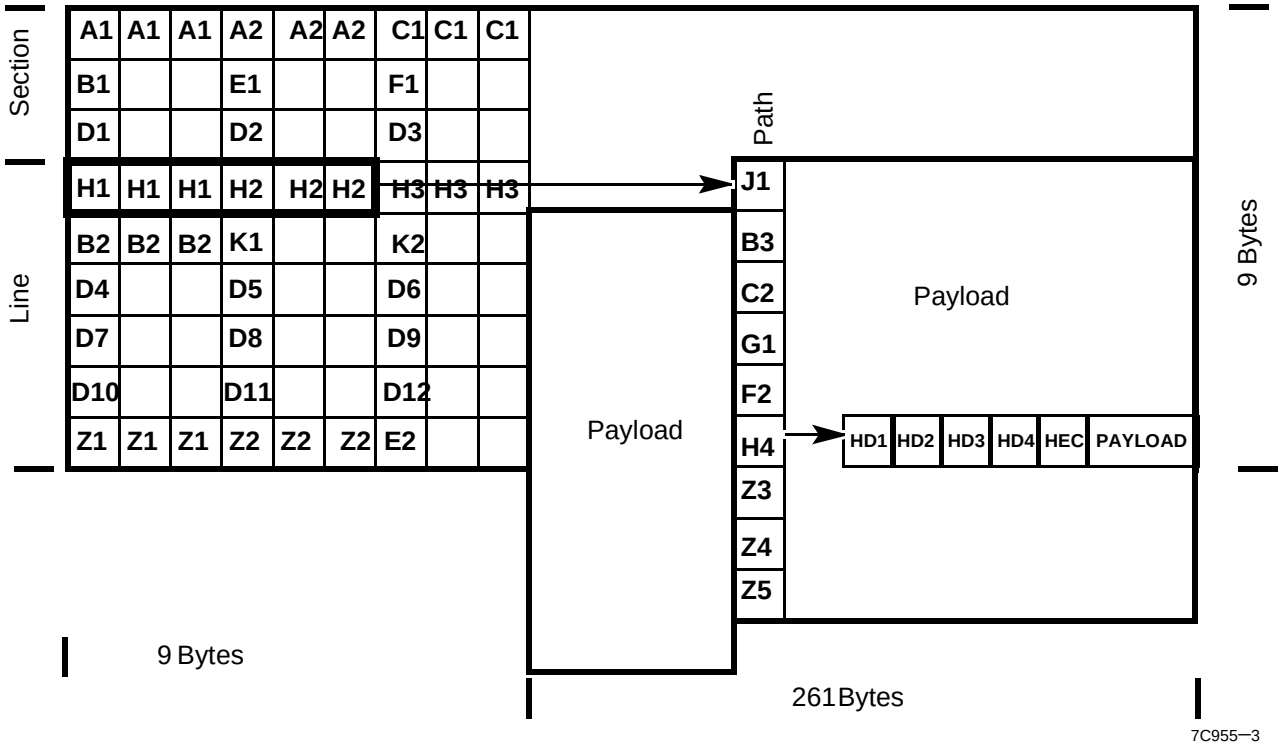


Figure 1. STS–3c/STM–1 Framing Format

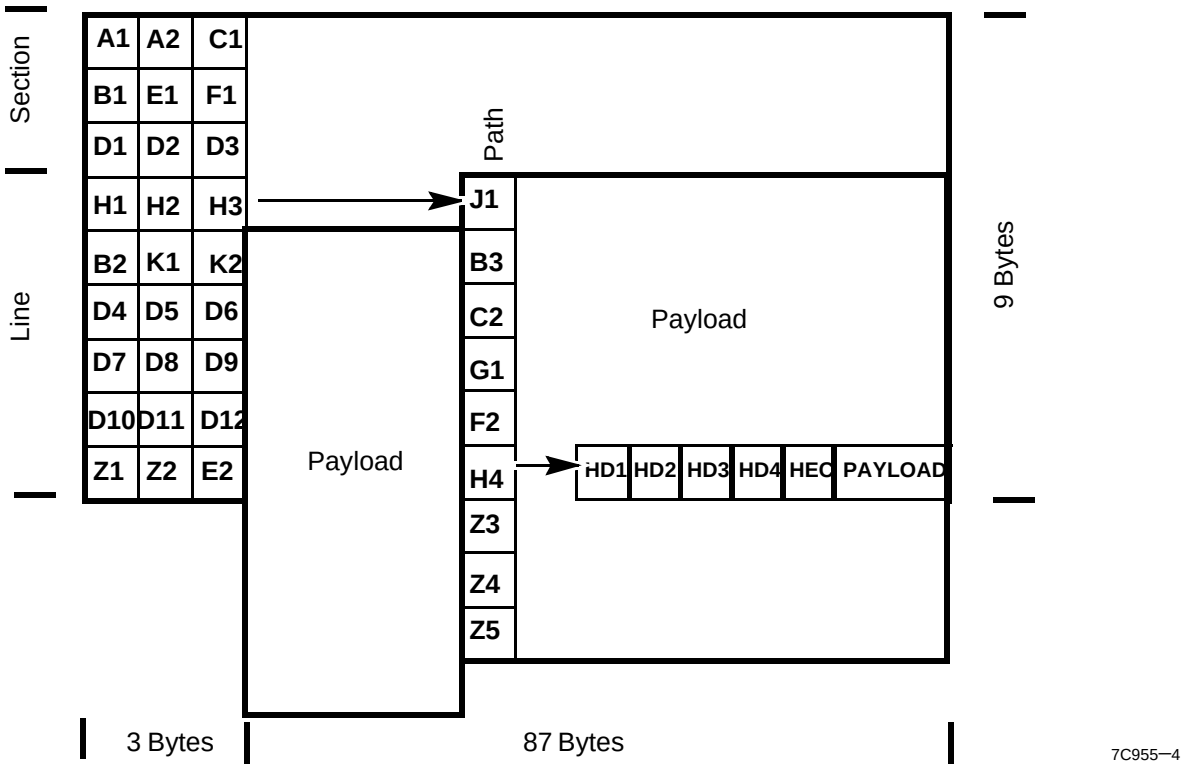


Figure 2. STS–1 Framing Format

Transmit SONET Line Overhead Processor (TLOP)

The Transmit SONET line overhead processor (TLOP) provides BIP–8/24 generation and line level alarms.

The BIP–8/24 code is calculated as if the STS–3c frame was composed of three STS–1s. The first B2 byte is calculated over the first STS–1 frame, the second B2 byte over the second STS–1 frame and the third B2 byte over the third STS–1 frame. Each B2 bit is calculated over the line and SPE portions of the previous frame before scrambling using even parity and inserted into the current frame before scrambling. For STS–1 RATE, a BIP–8 is calculated over the entire SPE and line overhead and placed in B2.

The Line Alarm Indication Signal (LAIS), is asserted by changing all bits of the SONET frame into 1 before scrambling. LAIS generation is controlled by a register setting (Reg–14H, bit 0).

The Line Far End Receive Failure (LFERF), also called Line RDI, is indicated by placing a 110 pattern in bits 6, 7, and 8 of the first K2 byte. LFERF can be asserted under register (Reg–20H, bit 0) control.

The Line Far End Block Errors (LFEBE) are located in the third Z2 byte and indicate the number of B2 errors in the previous frame interval. Legal values for this byte are 00h through 18h.

All bytes of the line data communication channel (D4–D12) and all other unused bytes are encoded to 00h.

Transmit SONET Section Overhead Processor (TSOP)

The Transmit SONET Line Overhead Processor (TSOP) provides A1,A2 framing pattern generation, section BIP–8 (B1) insertion, section level alarm insertion, and frame scrambling.

The A1 and A2 bytes provide a framing pattern for frame alignment. All A1 bytes are coded to F6h and all A2 bytes are coded to 28h. These bytes are not scrambled upon transmission.

The STS–1 identification bytes, C1, are used for framing and de-interleaving purposes and are coded the order in their appearance in the STS–3c frame. The first C1 byte is coded to 01h, the second to 02h, and the third to 03h.

The section BIP–8 (B1) is the byte-interleaved parity-8 calculated over all bytes of the previous frame after scrambling and inserted into the current frame before scrambling.

The bytes of the section data communication channel, D1–D3 and the remaining unused bytes are set to 00h.

The frame is scrambled prior to transmission with the generating polynomial $x^7 + x^6 + 1$. The A1, A2, and C1 bytes are not scrambled. The scrambler runs continuously through the frame and resets at the beginning of the next transmission frame. The scrambler may be optionally disabled.

Transmit Clock Generator (TCG)

The TCG accepts a byte-rate transmit clock from TRCLK that operates at either 19.44 MHz for STS–3c/STM–1 RATE or at 6.48 MHz for STS–1 RATE. The Transmit PLL multiplies this byte-rate reference by eight to produce the bit-rate clock used by the parallel-to-serial converter. Optionally a bit-rate source can be taken from an external source (TBYP = 1) or from the Receive Clock Recovery block when in loop-time mode (LOOPT = 1). In loop-time mode the recovered clock is used to provide timing to the transmitter.

Parallel to Serial Converter (PSC)

The PSC converts the parallel data from the TSOP to serial data. The bit rate clock is derived from the Transmit Clock Generator. The serialized data and aligned output clock are presented to the Transmit Output Multiplexer.

Transmit Output Multiplexer (TOM)

The TOM selects between the serialized output data stream and associated clock provided by the PSC and the recovered data and clock from the Receive Clock Recovery block for transmission based on the state of the local loop back enable (LLE) register (Reg–05H, bit 2). When LLE = 1 the recovered data and recovered clock is selected for output on the transmit data lines (TXD±) and the transmit clock lines (TXC±). The output signal is 100K compatible differential Positive-referenced ECL (PECL) signal capable of driving any copper or fiber based media with impedances as LOW as 50Ω.

Receive Section

Receive Clock Recovery (RCR)

The RCR provides clock and data recovery from an incoming differential PECL data stream. Clock and data are recovered from the incoming differential PECL data stream without the need for external buffering and AC-coupling. The built-in line receiver inputs have a wide common-mode range (2.5–5V) and the ability to receive signals with as little as 200 mV differential voltage. They are compatible with all PECL signals. They are compatible with all PECL signals driven by optical modules or twisted-pair equalizers. The Receive PLL uses the RRCLK as a byte-rate reference. This input is multiplied by 8 and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the RATE0 pin. To insure accurate data and clock recovery, the received data stream must be within 1000 ppm of RRCLK * 8 (The PLL will declare Out Of Lock if the data rate is different from REFCLK x 8 by more than 2000 ppm. The PLL will remain Out Of Lock until the data rate pulls back to within 700 ppm of REFCLK x 8 frequency). The standards, however, specify that the RRCLK*8 frequency accuracy be within 20–100 ppm. The wider frequency tolerance range of the CY7C955 is an advantage that allows for higher frequency tolerance in bench testing setups.

A Loss of Signal (ROOLV = 1) is declared when no transitions have been detected on the incoming data stream for more than 512 bit-times. LOS is cleared when two valid framing patterns (A1, A2) have been found and the intervening data does not contain a period that violates the minimum transitions limit.

Serial to Parallel Conversion (SPC)

The SPC converts bit serial data to byte serial data from either the recovered received data or the transmit data from the PSC depending on the state of the DLE register (Reg–05H, bit 1). When DLE =1 transmit data is used for serial to parallel conversion. The SPC also provides SONET framing by scanning the incoming data for the SONET framing pattern A1, A2. For STS–1 RATE the framer looks for the pattern F628h and for STS–3 RATE the framer looks for the pattern F6F6F6282828h. Out of Frame (OOF) is declared when four consecutive frames contain a framing error. OOF clears when two frames contain valid framing characters. Loss of Frame

(LOF) is declared when the OOF condition fails to clear within 3 ms. LOF clears after 3 ms of frames with valid framing characters.

Receive SONET Section Overhead Processor (RSOP)

The RSOP provides descrambling, SONET section alarm indication, and error monitoring.

The data is descrambled using the generating polynomial $1 + x^6 + x^7$. The A1, A2, and C1 bytes are not descrambled. The scrambling process may be disabled under register control.

The BIP–8 value calculated over the previous scrambled frame is compared with the B1 byte of the current frame section overhead after descrambling. If the two values do not match, the B1PAR output is taken HIGH. Up to 64,000 errors can be detected per second (8000 frames/second * 8 bit-errors (max)/frame). Errors are recorded in a 16-bit saturating counter that can be read through the controller interface.

Receive SONET Line Overhead Processor (RLOP)

The RLOP provides SONET line alarm indications and error monitoring.

A Line Alarm Indication Signal (LAIS) is asserted when a 111 pattern is detected for five consecutive frames in bits 6,7, and 8 of the first K2 byte of the Automatic Protection Switching channel. LAIS is removed when anything other than a 111 pattern is received for five consecutive frames.

A Line Far End Receive Failure (LFERF) or Line RDI is indicated with a 110 pattern is detected for five consecutive frames in bits 6,7, and 8 of the first K2 byte. LFERF is removed when anything other than a 110 pattern is received for five consecutive frames.

The BIP–24 (BIP–8 for STS–1 RATE) value calculated over the previous line overhead and SPE is compared with the B2 bytes of current frame. Up to 192,000 errors can be detected per second (3 channels/frame * 8 errors (max)/channel * 8000 frames/second). Errors are recorded in a 20-bit saturating counter that can be read through the controller interface.

Far End Block Errors (FEBE) are detected by examining the value in the third Z2 byte. This value (0–18h) is added to the count in an 18-bit saturating counter that can be read through the controller interface.

Receive SONET Path Overhead Processor (RPOP)

The RPOP provides pointer interpretation, SPE extraction, SONET path alarm indications, and error monitoring.

The payload location is determined by examining the values in the H1 and H2 bytes of the line overhead which indicate the J1 byte of the SPE. The RPOP can process a J1 byte located anywhere in the SPE. Loss of Pointer (LOP) is set when a valid pointer value has not been found within eight consecutive frames. This register bit is cleared when a valid pointer is found for three consecutive frames. Path Alarm Indication Signal (PAIS) (Reg30H, bit 3) is set when the H1 and H2 bytes are set to all ones for 3 consecutive frames. This register bit is cleared when a valid pointer is found for three consecutive frames. PAIS does not cause LOP to be set. The SPE location is provided to the Receive ATM Cell Processor for cell extraction.

The BIP–8 value calculated over the previous SPE is compared with the B3 byte of the current path overhead. Up to 65,535 errors can be detected per second. Errors are recorded in a 16-bit saturating counter that can be read through the controller interface.

Path Far End Block Errors (PFEBE) are detected by examining the value in bits 1 through 4 of G1. This value (0–8h) is added to the count in a 16-bit saturating counter that can be read through the controller interface.

Path Far End Receive Failures (PFERF) are detected by examining the value in bits 1 through 4 of G1. If this value is 9h for two consecutive frames, PFERF is set. This register bit is cleared when anything other than 9h appears for two consecutive frames.

Path Remote Defect Indication (Path RDI) is detected by examining bit 5 of G1. If this value is 1h for 5 consecutive frames, PYEL is set. This register bit is cleared when a 0 appears in bit 5 for 5 consecutive frames.

Receive ATM Cell Processor (RACP)

The RACP block provides cell delineation, HEC checking and correcting, cell filtering for idle/unassigned cells, cell payload descrambling, status indications, and error monitoring.

Cell delineation is performed by comparing the HEC sequence calculated over the first four bytes of the SPE to the fifth byte. If these values match, cell boundary has been determined. If not, the calculation advances one byte further into the payload (bytes 2–5) and the check is performed again. The HEC sequence is a CRC–8 calculated over the first 4 octets of the ATM cell header using the polynomial $x^8 + x^2 + x + 1$. The coset $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the residue before comparison with the received sequence. This is the HUNT state of the cell delineation process. When a valid match has occurred the process enters the PRESYNC state. When 7 consecutive matches occur the process enters the SYNC state. If 6 consecutive incorrect HEC matches are detected the process moves back to the HUNT state. The average time for cell delineation is 93µs for STS–1 and 31µs for STS–3C.

The HEC sequence is used not only to check for cell alignment, but also to insure that integrity of the ATM header. The HEC is used to correct single bit errors and to detect multiple bit errors. This feature can be disabled. The register file contains two saturating 8-bit counters for HEC errors; one for cells with single bit errors and another for multiple-bit errors. Cells with multiple bit errors are optionally discarded. *Figure 3* shows the state diagram for HEC.

The RACP optionally discards Idle/Unassigned cells. These cells contain a VPI/VCI address of 0h. Also, a Header Mask and Header Match register are provided to allow cells with a particular header characteristic in GFC, PTI and CLP to be filtered.

The payload of valid cells are descrambled using the polynomial $x^{43} + 1$. The cell headers are not descrambled since they

were not scrambled upon transmission. The descrambling feature can be disabled.

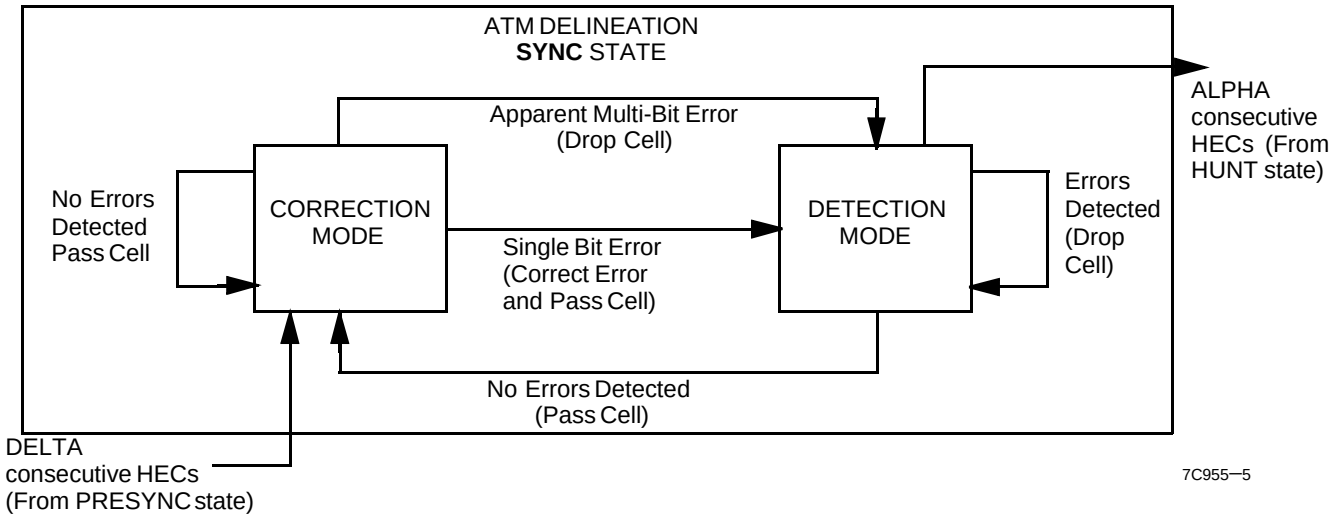


Figure 3. HEC Verification State Diagram

Receive Utopia Interface (RUI)

The RUI provides a simple access from the external environment to the ATM Transceiver. The operation of this interface is compliant with the Utopia interface specification that is being standardized by the ATM Forum. The interface provides a 10 bit by 4 cell FIFO to decouple the system interface from the ATM physical layer timing. Ten bit words are clocked out from the device through a clocked FIFO style interface. These 10 bits include an 8-bit data word along with an parity bit (RXPRTY) and a Start Of Cell (SOC) indication. The interface also provides a cell available (RCA) indication and a read enable (RRDENB) control. RCA allows the FIFO to indicate empty and almost empty conditions and RRDENB allows the downstream circuit to pause the reading process in case the downstream cannot accept anymore read. If the Receive FIFO overflows, FIFO reset will occur and up to 4 cells may be lost because of the operation.

Controller Interface (CI)

The CI interface provides external access to the internal register file, device resetting and external input for the carrier detect signal. The ALOS input allows an external carrier detect from an optical module to cause an interrupt to the controller. The INTB and RALM pins can be configured to interrupt the external controller whenever any of several different error conditions occur. RALM signals the most important error conditions such as LOS, LOF, line AIS, path AIS, LCD, and LOP. INTB may indicate all possible errors depending on the state of the mask registers. INTB provides notification of the individual processing block that generated the error condition. The error register contained in each block will determine the exact cause of the interrupt.

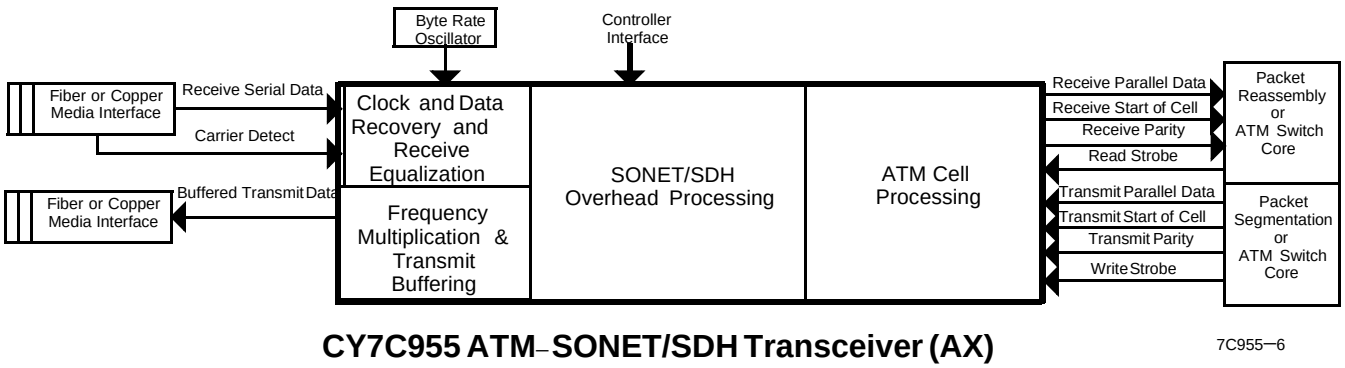


Figure 4. SONET/SDH and ATM Interface

$F6_H$ A1	$F6_H$ A1	$F6_H$ A1	28_H A2	28_H A2	28_H A2	01_H C1	02_H C1	03_H C1
NOTE 1 B1	00_H	00_H	00_H E1	00_H	00_H	00_H F1	00_H	00_H
00_H D1	00_H	00_H	00_H D2	00_H	00_H	00_H D3	00_H	00_H
62_H H1	93_H H1	93_H H1	$0A_H$ H2	FF_H H2	FF_H H2	00_H H3	00_H H3	00_H H3
[NOTE 1] B2	[NOTE 1] B2	[NOTE 1] B2	00_H K1	00_H	00_H	00_H K2	00_H	00_H
00_H D4	00_H	00_H	00_H D5	00_H	00_H	00_H D6	00_H	00_H
00_H D7	00_H	00_H	00_H D8	00_H	00_H	00_H D9	00_H	00_H
00_H D10	00_H	00_H	00_H D11	00_H	00_H	00_H D12	00_H	00_H
00_H Z1	00_H Z1	00_H Z1	00_H Z2	00_H Z2	[NOTE 1] Z2	00_H E2	00_H	00_H

7C955—7

Note:
1. B1, B2, Z2, G1, H4, and B3 are variables.

Figure 5. Default Values for the Transmitted Section and Line STS–3C/STM–1 Overhead

$F6_H$ A1	$F6_H$ A2	00_H C1
NOTE 1 B1	00_H E1	00_H F1
00_H D1	00_H D2	00_H D3
62_H H1	$0A_H$ H2	00_H H3
NOTE 1 B2	00_H K1	00_H K2
00_H D4	00_H D5	00_H D6
00_H D7	00_H D8	00_H D9
00_H D10	00_H D11	00_H D12
00_H Z1	NOTE 1 Z2	00_H E2

7C955—8

Figure 6. Default Values for the Transmitted Section and Line STS–1 Overhead

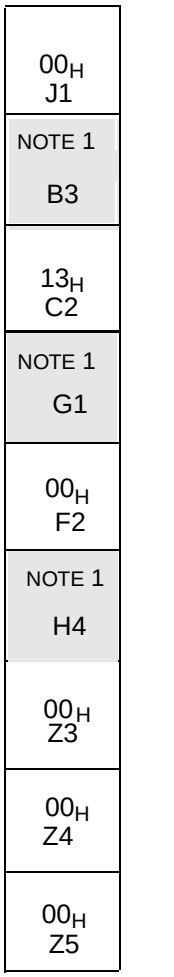
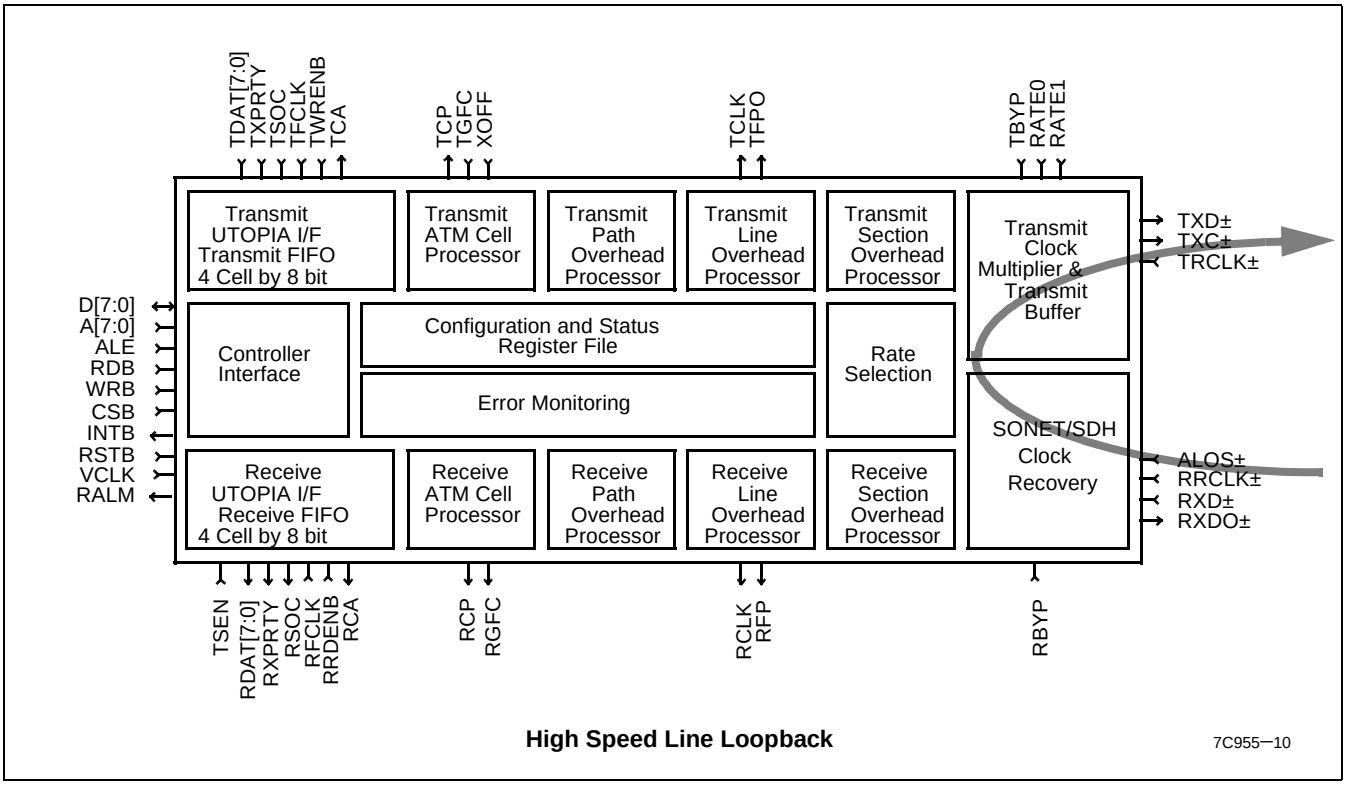


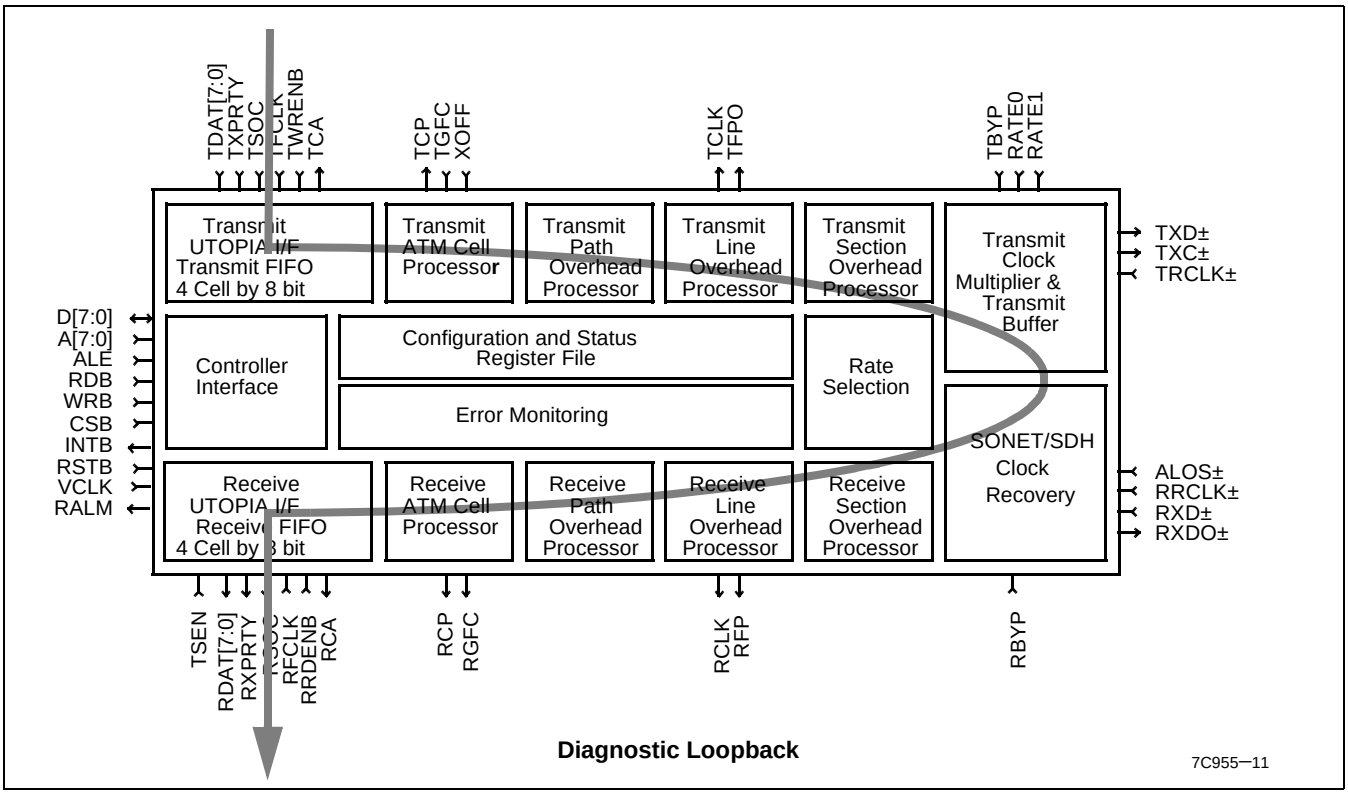
Figure 7. Default Values for the Transmitted Path Overhead

Loopback Operation



High Speed Line Loopback

7C955—10



Diagnostic Loopback

7C955—11

SONET Overhead Description

Signal Values	Description
A1, A2	The frame alignment bytes mark the beginning of a SONET frame. They are transmitted every 125 µs in both OC–1 and OC3c speeds. Transmit Side: In OC–1, A1($F6_H$) and A2 (28_H) are inserted into the transmitted stream at the beginning of every frame. These bytes are not scrambled by the frame synchronous SONET scrambler. Receive Side: The receiver will search for and frame onto the incoming A1, A2 bytes.
C1	This is the identification byte for the STS data stream. Transmit Side: In OC–1, C1 is transmitted as OH. In OC–3c, the sequence C1, C1, C1 of every frame is transmitted as 01_H, 02_H, 03_H. These bytes are not scrambled by the frame-synchronous SONET scrambler. Receive side: The receiver will ignore C1.
B1	This is the section bit interleave parity byte. Transmit Side: B1 is calculated using the BIP–8 algorithm described in I.432. It is inserted into the SONET data stream before the frame synchronous SONET scrambler. Receive Side: Received B1 error events are accumulated in the SBE [15:0] (Reg–12H and Reg–13H).
H1, H2	These are the pointer value byte. These bytes are used to locate the beginning of the Synchronous Payload Envelope (SPE) in the SONET/SDH frame. Transmit side: H1, H2 contains the normal new data flag (0110) together with 522 (decimal) as the fixed pointer value field. The concatenation indication byte is also inserted (H1* = 93, H2* = FF). Receive Side: H1 and H2 are used to locate the beginning of the SPE. If a valid pointer cannot be found, CY7C955 will indicate a Loss of Pointer State. Path AIS is detected by an all-ones pattern in H1 and H2 bytes.
H3	This is the pointer action byte. Transmit Side: H3 will be all zeroes. Receive Side: Synchronous Payload Data will be stuffed in the H3 byte if a negative stuff event occurs. This byte is ignored otherwise.
B2	This is the line bit interleaved parity bytes, it is used to monitor line errors. Transmit Side: B2 is calculated over all bits of the line overhead and the SPE capacity of the previous frame before the frame is being scrambled. The B2 byte itself is then placed in the current frame before scramble.
K2	This is the identity line layer maintenance signal. Transmit Side: Bits 6, 7, and 8 of this byte are ‘110’ before scrambling when Line Remote Defect Indication is true. The whole of K2 is an all-one pattern before scrambling if Line AIS is inserted. Receive Side: Bits 6, 7, and 8 of the K2 byte are being examined to determine the presence of AIS, and RDI signals. Access to APs registers will be available in future revisions.
Z2	This is the growth byte. It is used to provide far end block error function useful for remote performance monitoring. Transmit Side: The number of B2 errors detected in the last frame is inserted. Z2 is a number from 0–24 indicating 0–24 errors. Receive Side: A legal (0–24) Z2 number will be added to the line FEBE counter.
B3	This is the interleaved parity byte. Transmit Side: B3 is calculated over all bits of the SPE of the previous frame before scrambling and is placed in the current frame before scrambling. This provides path error monitoring capability for the link. Receive Side: The value in B3 is accumulated in a register.
C2	This is the path signal label byte for indicating the contents of the SONET payload. Transmit Side: It’s fixed value is 13H. This indicates the payload is ATM. Receive Side: The receive side expects C2 to be 13H. If the data is not 13H for 3 consecutive frames, an interrupt (if enabled) will be generated.
G1	This is the path status byte. Transmit Side: Path remote defect Indication (Path RDI) together with the number of B3 errors in the last frame are inserted into G1 before scrambling for transmission. G1 is a number from 0–8, indicating 0–8 errors. Receive side: A legal G1 value (0–8) will be accumulated in the FEBE counter. Path remote defect indication is also detected through this byte.
H4	This is the cell offset byte. Transmit Side: This byte indicates the offset in bytes between the H4 byte and the first cell byte after H4. Receive Side: H4 byte is ignored.

CY7C955 Register Map

Address	Register
Reg–00H	Master Reset/Type/Identify Register
Reg–01H	Master Configuration Register
Reg–02H	Master Interrupt Register
Reg–04H	Master Clock Monitor Register
Reg–05H	Master Control Register
Reg–06H	Transmit Clock Synthesis Control Register
Reg–07H	Receive Clock Synthesis Control Register
Reg–10H	Receive Section Overhead Processor Control Register
Reg–11H	Receive Section Overhead Processor Status Register
Reg–12H	LSB of the Receive Section Overhead Processor Status BIP-8 Counter
Reg–13H	MSB of the Receive Section Overhead Processor Status BIP-8 Counter
Reg–14H	Transmit Section Overhead Processor Control Register
Reg–15H	Transmit Section Overhead Processor Control Error Insertion Register
Reg–18H	Receive Line Overhead Processor Control and Status Register
Reg–19H	Receive Line Overhead Processor Interrupt Enable and Status Register
Reg–1AH	Line BIP–8/24 Register
Reg–1BH	Line BIP–8/24 Register
Reg–1CH	Line BIP–8/24 Register
Reg–1DH	Line Far-End Block Error Register
Reg–1EH	Line Far-End Block Error Register
Reg–1FH	Line Far-End Block Error Register
Reg–20H	Transmit Line Overhead Processor Register
Reg–21H	Transmit Line Overhead Processor Error Insertion Register
Reg–30H	Receive Path Overhead Processor Interrupt Register
Reg–31H	Receive Path Overhead Processor Register
Reg–33H	Receive Path Overhead Processor Interrupt Enable Register
Reg–37H	Receive Path Signal Label Register
Reg–38H	Path BIP–8 (B3) Register
Reg–39H	Path BIP–8 (B3) Register
Reg–3AH	Path Far-End Block Error Register
Reg–3BH	Path Far-End Block Error Register
Reg–3CH	Path Far-End Block Error Register
Reg–40H	Transmit Path Overhead Processor Error Insertion Register
Reg–41H	Transmit Path Overhead Processor Pointer Control Register
Reg–45H	Transmit Path Overhead Processor Arbitrary Payload Pointer Register
Reg–46H	Transmit Path Overhead Processor Arbitrary Payload Pointer Register
Reg–48H	Transmit Path Overhead Processor Path Signal Label Register
Reg–49H	Transmit Path Overhead Processor Arbitrary Path Status Register
Reg–50H	Receive ATM Cell Processor Control and Status Register
Reg–51H	Receive ATM Cell Processor Interrupt Register
Reg–52H	Receive ATM Cell Processor Match Header Pattern Register
Reg–53H	Receive ATM Cell Processor Match Header Mask Register
Reg–54H	Receive ATM Cell Processor Correctable HCS Error Count Register

CY7C955 Register Map (continued)

Address	Register
Reg–55H	Receive ATM Cell Processor Uncorrectable HCS Error Count Register
Reg–56H	Receive ATM Cell Processor Receive Cell Counter Register
Reg–57H	Receive ATM Cell Processor Receive Cell Counter Register
Reg–58H	Receive ATM Cell Processor Receive Cell Counter Register
Reg–59H	Receive ATM Cell Processor Receive Configuration Register
Reg–60H	Transmit ATM Cell Processor Control and Status Register
Reg–61H	Transmit ATM Cell Processor Unassigned Cell Header Register
Reg–62H	Transmit ATM Cell Processor Unassigned Cell Payload Register
Reg–63H	Transmit ATM Cell Processor FIFO Control Register
Reg–64H	Transmit ATM Cell Processor Transmit Cell Counter Register
Reg–65H	Transmit ATM Cell Processor Transmit Cell Counter Register
Reg–66H	Transmit ATM Cell Processor Transmit Cell Counter Register
Reg–67H	Transmit ATM Cell Processor Transmit Configuration Register
Reg–80H	CY7C955 Test Control Register

REG–00H	**Master Reset / Type / Identity Register**		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	RESET	R/W	0
6	TYPE[2]	R	0
5	TYPE[1]	R	1
4	TYPE[0]	R	1
3	ID[3]	R	1
2	ID[2]	R	1
1	ID[1]	R	1
0	ID[0]	R	1

RESET

This is the master reset bit. Toggling this register has the same effect as toggling the RSTB pin, except that RSTB will reset all registers to their default values, while writing a 1 to this register will only reset all other registers (but not itself) to their default values. Leaving a 1 in this register puts the AX in power-down mode.

0: Normal mode.

1: Reset / Power Down Mode.

TYPE[2:0]

These bits differentiate the AX with other Cypress products.

ID[3:0]

These bits show the revision number of the CY7C955.

REG – 01H	Master Configuration Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	AUTOFEBE	R/W	1
5	AUTOLRDI	R/W	1
4	AUTOPRDI	R/W	1
3	TCAINV	R/W	0
2	RCAINV	R/W	0
1	RXDINV	R/W	0
0	Unused		

AUTOFEBE

This bit controls whether Far End Block Error (FEBE) is transmitted when line or path BIP error is being detected on the receive data stream.

0: Do not generate line or path FEBE error in response to incoming line or path BIP error.

1: Generate line or path FEBE error in response to incoming line or path BIP error.

AUTOLRDI

This bit controls whether Line Remote Defect Indication (LRDI) is transmitted when an incoming alarm is being detected.

0: Do not insert line RDI when line AIS, Loss of Frame (LOF) or Loss of Signal (LOS) is being detected.

1: Insert line RDI when line AIS, Loss of Frame (LOF) or Loss of Signal (LOS) is being detected.

AUTOPRDI

This bit controls whether STS Path Remote Defect Indication (PRDI) is transmitted when an incoming alarm is being detected.

0: Do not insert STS path RDI when Loss of Signal (LOS), Loss of Pointer (LOP), STS path AIS, Loss of Frame (LOF), line AIS, or Loss of Cell Delineation (LCD) is being detected.

1: Insert STS path RDI when Loss of Signal (LOS), Loss of Pointer (LOP), STS path AIS, Loss of Frame (LOF), line AIS, or Loss of Cell Delineation (LCD) is being detected.

TCAINV

This bit controls the polarity of TCA.

0: TCA is active HIGH.

1: TCA is active LOW.

RCAINV

This bit controls the polarity of RCA.

0: RCA is active HIGH.

1: RCA is active LOW.

RXDINV

This bit controls the interpretation of the differential pair RXD.

0: Logical 1 is represented by RXD+ HIGH and RXD– LOW.

1: Logical 0 is represented by RXD+ HIGH and RXD– LOW.

REG – 02H	Master Interrupt Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	TROOLI	R	
6	LCDI	R	
5	RDOOLI	R	
4	TACPI	R	
3	RACPI	R	
2	RPOPI	R	
1	RLOPI	R	
0	RSOPI	R	

TROOLI

This is the Transmit Reference Out Of Lock Interrupt. This bit resets when Reg–02H is being read.

1: TROOLV (Reg–06H, bit 3) has changed state since Reg–02H was last read.

0: TROOLV (Reg–06H, bit 3) has not changed state since Reg–02H was last read.

LCDI

This is the Loss of Cell Delineation Interrupt. It has to be enabled by bit 7 of Reg–05H. This bit resets when Reg–02H is being read.

1: Loss of cell delineation is entered or exited since Reg–02H was last read.

0: There is no change in the loss of cell delineation state.

RDOOLI

This is the Receive Data Out Of Lock Interrupt. This bit resets when Reg–02H is being read.

1: RDOOLV (Reg–07H, bit 3) has changed state since Reg–02H was last read.

0: RDOOLV (Reg–07H, bit 3) has not changed state since Reg–02H was last read.

TACPI

This is the Transmit ATM Cell Processor Interrupt. This bit resets when Reg–02H is being read. This register is a logical OR of all the Transmit ATM Cell Processor (TACP) interrupts Reg–60H and 63H.

1: FOVRI, TSOCI, or TXPRTYI is HIGH.

0: FOVRI, TSOCI, and TXPRTYI are all LOW.

RACPI

This is the Receive ATM Cell Processor Interrupt. This bit resets when Reg–02H is being read. This register is a logical OR of all the Receive ATM Cell Processor (RACP) interrupts of Reg–51H.

1: OOCDI, CHCSI, or UHCSI is HIGH.

0: OOCDI, CHCSI, and UHCSI are all LOW.

RPOPI

This is the Receive Path Overhead Processor Interrupt. This bit resets when Reg–02H is being read. This register is a logical OR of all the Receive Path Overhead Processor (RPOP) interrupts of Reg–31H.

1: PSLI, LOPI, PAISI, PRDII, BIPEI, or FEBEI is HIGH.

0: PSLI, LOPI, PAISI, PRDII, BIPEI, and FEBEI are all LOW.

RLOPI

This is the Receive Line Overhead Processor Interrupt. This bit resets when Reg–02H is being read. This register is a logical OR of all the Receive Line Overhead Processor (RLOP) interrupts of Reg–19H.

1: FEBEI, BIPEI, LAISI, or RDII is HIGH.

0: FEBEI, BIPEI, LAISI, and RDII are all LOW.

RSOPI

This is the Receive Section Overhead Processor Interrupt. This bit resets when Reg–02H is being read. This register is a logical OR or all the Receive Section Overhead Processor (RSOP) interrupts or Reg–11H.

1: BIPEI, LOSI, LOFI, or OOFI is HIGH.

0: BIPEI, LOSI, LOFI, and OOFI are all LOW.

REG – 04H	Master Clock Monitor Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	RXDOD	R/W	0
6	XORTXC	R/W	0
5	Unused		
4	Unused		
3	RRCLKA	R	
2	TRCLKA	R	
1	RCLKA	R	
0	TCLKA	R	

RXDOD

This bit is used to turn off the RXDO output in case it is not needed. This helps save power and reduce power supply noise.

1: RXDO output is disabled.

0: RXDO is the retimed buffered output of RXDXORTXC.

XORTXC is used to invert the default-on status of the TXC output.

1: TXC is disabled if RATE0 is LOW, and TXC is a 155.52-MHz clock if RATE0 is HIGH.

0: TXC is a 51.84-MHz clock if RATE0 is LOW, and TXC is disabled if RATE0 is HIGH.

RRCLKA

This bit can be read to check for RRCLK transitions; when HIGH, this bit stays HIGH until Reg–04H is being read.

1: RRCLK+ has a LOW to HIGH transition since this register was last read.

0: RRCLK+ has no LOW to HIGH transitions since this register was last read.

TRCLKA

This bit can be read to check for TRCLK transitions; when HIGH, this bit stays HIGH until Reg–04H is being read.

1: TRCLK+ has a LOW to HIGH transition since this register was last read.

0: TRCLK+ has no LOW to HIGH transitions since this register was last read.

RCLKA

This bit can be read to check for RCLK transitions; when HIGH, this bit stays HIGH until Reg–04H is being read.

1: RCLK has a LOW to HIGH transition since this register was last read.

0: RCLK has no LOW to HIGH transitions since this register was last read.

TCLKA

This bit can be read to check for TCLK transitions; when HIGH, this bit stays HIGH until Reg–04H is being read.

1: TRCLK+ has a LOW to HIGH transition since this register was last read.

0: TRCLK+ has no LOW to HIGH transitions since this register was last read.

REG – 05H	Master Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	LCDE	R/W	0
6	LCDV	R	
5	FIXPTR	R/W	1
4	Unused		
3	Unused		
2	LLE	R/W	0
1	DLE	R/W	0
0	LOOPT	R/W	0

LCDE

This bit enables a change in the Loss of Cell Delineation state to generate an interrupt on pin INTB.

0: INTB will not be affected by a transition in LCDV (Reg–05H, bit 6).

1: INTB will go LOW when there is a transition in LCDV (Reg–05H, bit 6).

LCDV

This bit shows the present loss of cell delineation state of the Receive ATM Cell overhead Processor (RACP).

0: RACP is in SYNC state for longer than 4 ms.

1: RACP is out of cell delineation for more than 4 ms and there are no detected LOS, LOP, Path AIS, and Line AIS.

FIXPTR

This bit controls the operation of the transmit payload pointer adjustment function.

0: The setting in Reg–41H can control the payload pointer adjustment operations.

1: The transmit payload pointer is fixed at 522.

LLE

This bit controls the line loop-back path of the CY7C955; DLE and LLE cannot be both set to 1.

0: Normal operation.

1: RXD+ and RXD– are connected to TXD+ and TXD– internally.

DLE

This bit controls the diagnostic loop-back path of the CY7C955; DLE and LLE cannot be both set to 1.

0: Normal operation.

1: The transmitted data steam is being looped back to the received data stream.

LOOPT

This bit enables loop timing.

0: The transmitted data stream derives its clock from TRCLK. The clock to use depends on the setting of TREFSEL (Reg–06H, bit 0) and on the level of pins TBYP and RATE0.

1: The transmitted data stream derives its clock from RRCLK if the clock and data recovery function of the receiver is not active and from RXD if the clock and data recovery function is active. Again, the clock to use in RRCLK depends on the setting of RREFSEL (Reg–07H), RBYP, and RATE0.

REG – 06H	Transmit Clock Synthesis Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	TROOLV	R	
2	Unused		
1	TROOLE	R/W	0
0	TREFSEL	R/W	0

TROOLV

This bit is the Transmit Reference Out Of Lock Status register.

0: The divided-down synthesized transmit clock is within 2930 ppm of TRCLK or RRCLK (in loop timing mode).

1: The divided-down synthesized transmit clock is not within 2930 ppm of TRCLK or RRCLK (in loop timing mode).

TROOLE

This bit is the Transmit Reference Out Of Lock Interrupt Enable register.

0: INTB, the interrupt pin, will not be affected by transmit out of lock.

1: INTB, the interrupt pin, will pull LOW when there is a state change of TROOLV.

TREFSEL

This bit is the Transmit Reference Select. This bit is ignored in transmit bypass mode (TBYP = 1).

0: TRCLK expects a 19.44-MHz reference clock. If RATE0 is HIGH (155.52 Mbps, STS–3c/STM–1), the transmit PLL will multiply the TRCLK frequency by 8 times. If RATE0 is LOW (51.84 Mbps, STS–1), the transmit PLL will multiply the TRCLK frequency by 8/3 times to clock the transmitter.

1: TRCLK expects a 6.48-MHz reference clock. If RATE0 is HIGH (155.52 Mbps, STS–3c/STM–1), the transmit PLL will multiply the TRCLK frequency by 24 times. If RATE0 is LOW (51.84 Mbps, STS–1), the transmit PLL will multiply the TRCLK frequency by 8 times to clock the transmitter.

REG – 07H	Receive Clock Synthesis Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	RROOLV	R	
2	Unused		
1	RROOLE	R/W	0
0	RREFSEL	R/W	0

RROOLV

This bit is the Receive Reference Out Of Lock Status register.

0: The divided-down recovered clock is within 2930 ppm of RRCLK, and there is at least one transition on RXD during the last 80 bit-periods.

1: The divided-down recovered clock is not within 2930 ppm of RRCLK, or there are no transitions on RXD within the last 80 bit-periods.

RROOLE

This bit is the Receive Reference Out Of Lock Interrupt Enable register.

0: INTB, the interrupt pin, will not be affected by receiver out of lock.

1: INTB, the interrupt pin, will go LOW when there is a state change of RROOLV.

RREFSEL

This bit is the Receiver Reference Select. This bit is ignored in receiver bypass mode (RBYP = 1).

0: RRCLK expects a 19.44-MHz reference clock. If RATE0 is HIGH (155.52 Mbps, STS–3c/STM–1), the recovered clock is divided down 8 times before comparing with RRCLK. If RATE0 is LOW (51.84 Mbps, STS–1), the recovered clock is divided down 3/8 times before comparing with RRCLK.

1: RRCLK expects a 6.480-MHz reference clock. If RATE0 is HIGH (155.52 Mbps, STS–3c/STM–1), the recovered clock is divided down 24 times before comparing with RRCLK. If RATE0 is LOW (51.84 Mbps, STS–1), the recovered clock is divided down 8 times before comparing with RRCLK.

REG – 10H	Receive Section Overhead Processor Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	DDS	R/W	0
5	FOOF	W	0
4	Unused		
3	BIPEE	R/W	0
2	LOSE	R/W	0
1	LOFE	R/W	0
0	OOFE	R/W	0

DDS

This bit controls whether SONET descrambling is done on the receive data stream.

0: Descrambling is performed.

1: Descrambling is not performed.

FOOF

This bit can be used to manually put the Receive Section Overhead Processor out of frame.

0: No action.

1: The Receive Section Overhead Processor will detect an out of frame alarm at the next frame boundary.

BIPEE

This bit controls whether a section BIP–8 error (B1) generates an interrupt.

0: The interrupt pin, INTB, is not affected by section BIP–8 errors.

1: The interrupt pin, INTB, will go LOW upon receiving a section BIP–8 error.

LOSE

This bit controls whether a Loss of Signal alarm generates an interrupt.

0: The interrupt pin, INTB, is not affected by the loss of signal alarm.

1: The interrupt pin, INTB, will go LOW upon receiving a loss of signal alarm.

LOFE

This bit controls whether a Loss of Frame alarm generates an interrupt.

0: The interrupt pin, INTB, is not affected by the loss of frame alarm.

1: The interrupt pin, INTB, will go LOW upon receiving a loss of frame alarm.

OOFE

This bit controls whether an Out of Frame alarm generates an interrupt.

0: The interrupt pin, INTB, is not affected by the out of frame alarm.

1: The interrupt pin, INTB, will go LOW upon receiving an out of frame alarm.

REG – 11H	Receive Section Overhead Processor Status Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	BIPEI	R	
5	LOSI	R	
4	LOFI	R	
3	OOFI	R	
2	LOSV	R	
1	LOFV	R	
0	OOFV	R	

BIPEI

This is the section BIP–8 interrupt bit. This bit resets when Reg–11H is being read.

0: No section BIP–8 error is detected since Reg–11H was last read.

1: Section BIP–8 error is detected since Reg–11H was last read.

LOSI

This is the Loss of Signal (LOS) interrupt bit. This bit resets when Reg–11H is being read.

0: No change in the LOS status.

1: There is a change in the LOS status since Reg–11H was last read.

LOFI

This is the Loss of Frame (LOF) interrupt bit. This bit resets when Reg–11H is being read.

0: No change in the LOF status.

1: There is a change in the LOF status since Reg–11H was last read.

OOFI

This is the Out of Frame (OOF) interrupt bit. This bit resets when Reg–11H is being read.

0: No change in the OOF status.

1: There is a change in the OOF status since Reg–11H was last read.

LOSV

This bit shows the Loss of Signal (LOS) status of the CY7C955.

0: The Receive Section Overhead Processor is not in a loss of signal state.

1: The Receive Section Overhead Processor is in a loss of signal state.

LOFV

This bit shows the Loss of Frame (LOF) status of the CY7C955.

0: The Receive Section Overhead Processor is not in a Loss of Frame state.

1: The Receive Section Overhead Processor is in a Loss of Frame state. LOF is declared when OOF has lasted for more than 3 ms. LOFV stays HIGH until the Receive Section Overhead Processor is in frame for more than 3 ms.

OOFV

This bit shows the Out of Frame (OOF) status of the CY7C955.

0: The Receive Section Overhead Processor is in frame.

1: The Receive Section Overhead Processor is in an out of frame state.

REG – 12H	LSB of the Receive Section Overhead Processor Status BIP–8 counter		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	SBE[7]	R	0
6	SBE[6]	R	0
5	SBE[5]	R	0
4	SBE[4]	R	0
3	SBE[3]	R	0
2	SBE[2]	R	0
1	SBE[1]	R	0
0	SBE[0]	R	0

SBE[15:0]

Reg–12H and Reg–13H will load the number of BIP–8 errors from an internal counter approximately 1 µs after a write operation is done to Reg–12H, Reg–13H, or Reg–00H. At that time (1 µs after the write operation), these two registers are updated and the internal BIP–8 error counter is reset to zero to begin another round of error accumulation. Reading Reg–12H and Reg–13H after the write yields the number of BIP–8 (B1) errors accumulated since the counter was last written to, if overflow has not occurred.

REG – 13H	MSB of the Receive Section Overhead Processor Status BIP–8 counter		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	SBE[15]	R	0
6	SBE[14]	R	0
5	SBE[13]	R	0
4	SBE[12]	R	0
3	SBE[11]	R	0
2	SBE[10]	R	0
1	SBE[9]	R	0
0	SBE[8]	R	0

SBE[15:0]

Reg–12H and Reg–13H will load the number of BIP–8 errors from an internal counter approximately 1 µs after a write operation is done to Reg–12H, Reg–13H, or Reg–00H. At that time (1 µs after the write operation), these two registers are updated and the internal BIP–8 error counter is reset to zero to begin another round of error accumulation. Reading Reg–12H and Reg–13H after the write yields the number of BIP–8 (B1) errors accumulated since the counter was last written to if overflow has not occurred.

REG – 14H	Transmit Section Overhead Processor Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	DS	R/W	0
5	Unused		
4	Unused		
3	Unused		
2	Unused		
1	Unused		
0	LAIS	R/W	0

DS

This bit controls whether SONET scrambling is done to the transmit data stream.

0: Scrambling is performed.

1: Scrambling is not performed.

LAIS

This bit controls whether line Alarm Indication Signal (AIS) is being inserted into the transmit data stream.

1: All bits in the SONET frame (excluding the section overhead) are converted to a 1 prior to SONET scrambling. This operation begins immediately at the next frame boundary.

0: No line AIS is transmitted.

REG – 15H	Transmit Section Overhead Processor Error Insertion Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	DLOS	R/W	0
1	DBIP8	R/W	0
0	DFP	R/W	0

DLOS

This bit generates a continuous loss of signal error in the transmit data stream.

0: Normal operation.

1: TXD transmits all zeros.

DBIP8

This bit generates a continuous section BIP–8 (B1) error in the transmit data stream.

0: Normal operation.

1: B1 byte is inverted.

DFP

This bit generates a framing byte error in the transmit data stream.

0: Normal operation.

1: The most significant bit of the section overhead framing byte is converted from 1 to 0. In other words, F6H becomes H in the first A1 byte of the section overhead.

REG – 18H	Receive LIne Overhead Processor Control and Status Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	BIPWORD	R/W	0
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	Unused		
1	LAISV	R	0
0	RDIV	R	0

BIPWORD

This bit controls how many times a B2 error is recorded.

0: The B2 error counter increments only once per frame on receiving B2 bit-errors.

1: The B2 error counter increments once for every bit error represented in the B2 word. Note that in STS–3c, there could be at most 24 B2 bit-errors per frame, and in STS–1, there could be, at most, 8 B2 bit-errors per frame.

LAISV

This bit is the Line Alarm Indication Signal (LAIS) status register.

0: No Line AIS detected.

1: Line AIS has been detected. Line AIS is triggered by LOS or LOF.

RDIV

This bit is the Remote Defect Indication status register.

0: No remote defect indication (RDI) detected.

1: Remote defect indication (RDI) has been detected.

REG – 19H	Receive Line Overhead Processor Interrupt Enable and Status Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	FEBEE	R/W	0
6	BIPEE	R/W	0
5	LAISE	R/W	0
4	RDIE	R/W	0
3	FEBEI	R	
2	BIPEI	R	
1	LAISI	R	
0	RDII	R	

FEBEE

This bit controls whether line far end block error generates an interrupt by asserting INTB LOW.

0: Line far-end block error will not generate an interrupt.

1: Line far-end block error will generate an interrupt.

BIPEE

This bit controls whether BIP–24 (B2) error generates an interrupt by asserting INTB LOW.

0: BIP–24 error will not generate an interrupt.

1: BIP–24 error will generate an interrupt.

LAISE

This bit controls whether line alarm indication signal (LAIS) error generates an interrupt by asserting INTB LOW.

0: LAIS error will not generate an interrupt.

1: LAIS error will generate an interrupt.

RDIE

This bit controls whether a remote defect indication alarm detection generates an interrupt by asserting INTB LOW.

0: A change in the RDIV state (Reg–18H, bit 0) will not generate an interrupt.

1: A change in the RDIV state (Reg–18H, bit 0) will generate an interrupt.

FEBEI

This is the line far-end block error interrupt bit. This bit resets when Reg–19H is being read.

0: No line far-end block error has been detected since Reg–19H was last read.

1: Line far-end block error has been detected since Reg–19H was last read.

BIPEI

This is the section BIP–24 (B2) interrupt bit. This bit resets when Reg–19H is being read.

0: No line BIP–24 (B2) error has been detected since Reg–19H was last read.

1: Line BIP–24 (B2) error has been detected since Reg–19H was last read.

LAISI

This is the Line Alarm Indication Signal (LAIS) interrupt bit. This bit resets when Reg–19H is being read.

0: No LAIS has been detected since Reg–19H was last read.

1: LAIS has been detected since Reg–19H was last read.

RDII

This is the Remote Defect Indication (RDI) interrupt bit. This bit resets when Reg–19H is being read.

0: No line remote defect indication has been detected since Reg–19H was last read.

1: Line remote defect indication has been detected since Reg–19H was last read.

REG – 1AH	Line BIP–8/24 Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	LBE[7]	R	0
6	LBE[6]	R	0
5	LBE[5]	R	0
4	LBE[4]	R	0
3	LBE[3]	R	0
2	LBE[2]	R	0
1	LBE[1]	R	0
0	LBE[0]	R	0

LBE[19:0]

Reg–1AH to Reg–1CH will be loaded with the number of BIP–8/24 (B2) errors from an internal counter approximately 1 µs after a write operation is done to Reg–1AH, Reg–1BH, Reg–1CH, Reg–1DH, Reg–1EH, Reg–1FH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal BIP–8/24 error counter reset to zero to begin another round of error accumulation. Reading Reg–1AH, Reg–1BH, and Reg–1CH after the write yields the number of BIP–8/24 (B2) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 1BH	Line BIP–8/24 Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	LBE[15]	R	0
6	LBE[14]	R	0
5	LBE[13]	R	0
4	LBE[12]	R	0
3	LBE[11]	R	0
2	LBE[10]	R	0
1	LBE[9]	R	0
0	LBE[8]	R	0

LBE[19:0]

Reg–1AH to Reg–1CH will be loaded with the number of BIP–8/24 (B2) errors from an internal counter approximately 1 µs after a write operation is done to Reg–1AH, Reg–1BH, Reg–1CH, Reg–1DH, Reg–1EH, Reg–1FH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal BIP–8/24 error counter is reset to zero to begin another round of error accumulation. Reading Reg–1AH, Reg–1BH, and Reg–1CH after the write yields the number of BIP–8/24 (B2) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 1CH	Line BIP–8/24 Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	LBE[19]	R	0
2	LBE[18]	R	0
1	LBE[17]	R	0
0	LBE[16]	R	0

LBE[19:0]

Reg–1AH to Reg–1CH will be loaded with the number of BIP–8/24 (B2) errors from an internal counter approximately 1 µs after a write operation is done to Reg–1AH, Reg–1BH, Reg–1CH, Reg–1DH, Reg–1EH, Reg–1FH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal BIP–8/24 error counter is reset to zero to begin another round of error accumulation. Reading Reg–1AH, Reg–1BH, and Reg–1CH after the write yields the number of BIP–8/24 (B2) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 1DH	Line Far End Block Error Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	LFE[7]	R	0
6	LFE[6]	R	0
5	LFE[5]	R	0
4	LFE[4]	R	0
3	LFE[3]	R	0
2	LFE[2]	R	0
1	LFE[1]	R	0
0	LFE[0]	R	0

LFE[19:0]

Reg–1DH, Reg–1EH, and Reg–1FH will be loaded with the number of line FEBE (Z2) errors from an internal counter approximately 1 µs after a write operation is done to Reg–1AH, Reg–1BH, Reg–1CH, Reg–1DH, Reg–1EH, Reg–1FH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal line FEBE error counter is reset to zero to begin another round of error accumulation. Reading Reg–1DH, Reg–1EH, and Reg–1FH after the write yields the number of line FEBE (Z2) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 1EH	Line Far End Block Error Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	LFE[15]	R	0
6	LFE[14]	R	0
5	LFE[13]	R	0
4	LFE[12]	R	0
3	LFE[11]	R	0
2	LFE[10]	R	0
1	LFE[9]	R	0
0	LFE[8]	R	0

LFE[19:0]

Reg–1DH, Reg–1EH, and Reg–1FH will be loaded with the number of line FEBE (Z2) errors from an internal counter approximately 1 µs after a write operation is done to Reg–1AH, Reg–1BH, Reg–1CH, Reg–1DH, Reg–1EH, Reg–1FH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal line FEBE error counter are reset to zero to begin another round of error accumulation. Reading Reg–1DH, Reg–1EH, and Reg–1FH after the write yields the number of line FEBE (Z2) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 1FH	Line Far End Block Error Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused	R	0
6	Unused	R	0
5	Unused	R	0
4	Unused	R	0
3	LFE[19]	R	0
2	LFE[18]	R	0
1	LFE[17]	R	0
0	LFE[16]	R	0

LFE[19:0]

Reg–1DH, Reg–1EH, and Reg–1FH will be loaded with the number of line FEBE (Z2) errors from an internal counter approximately 1 µs after a write operation is done to Reg–1AH, Reg–1BH, Reg–1CH, Reg–1DH, Reg–1EH, Reg–1FH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal line FEBE error counter are reset to zero to begin another round of error accumulation. Reading Reg–1DH, Reg–1EH, and Reg–1FH after the write yields the number of line FEBE (Z2) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 20H	Transmit Line Overhead Processor Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	Unused		
1	Unused		
0	RDI	R/W	0

RDI

This bit controls whether line far end receive failure (RDI) is being inserted into the transmit data stream.

0: Transmit 000 in bits 6, 7, and 8 of K2.

1: Transmit 110 in bits 6, 7, and 8 of K2.

REG – 21H	Transmit Line Overhead Processor Error Insertion Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	Unused		
1	Unused		
0	DBIP	R/W	0

DBIP

This bit generates a continuous line BIP–8/24 (B2) error in the transmit data stream.

0: Normal operation.

1: Insert BIP8/24 (B2) error by inverting the B2 byte.

REG – 30H	Receive Path Overhead Processor Interrupt Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	LOP	R	
4	Unused		
3	PAIS	R	
2	PRDI	R	
1	Unused		
0	Unused		

LOP

This bit is the Loss of Pointer (LOP) alarm register.

0: No loss of pointer alarm detected.

1: Loss of pointer alarm detected.

PAIS

This bit is the path Alarm Indication Signal (AIS) register.

0: No path alarm indication signal detected.

1: Path alarm indication signal detected.

PRDI

This bit is the path Far-End Receive Failure (RDI) alarm register.

0: No path far-end receive failure (RDI) alarm detected.

1: Path far-end receive failure (RDI) alarm detected.

REG – 31H	Receive Path Overhead Processor Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	PSLI	R	
6	Unused		
5	LOPI	R	
4	Unused		
3	PAISI	R	
2	PRDII	R	
1	BIPEI	R	
0	FEBEI	R	

PSLI

This is the Path Signal Label (PSL) register interrupt bit. This bit resets when Reg–31H is being read.

0: No change in the path signal label since Reg–31H was last read.

1: There is a change in the path signal label since Reg–31H was last read.

LOPI

This is the Loss of Pointer (LOP) interrupt bit. This bit resets when Reg–31H is being read.

0: No change in the loss of pointer state since Reg–31H was last read.

1: There is a change in the loss of pointer state since Reg–31H was last read.

PAISI

This is the path Alarm Indication Signal (AIS) interrupt bit. This bit resets when Reg–31H is being read.

0: No change in the path alarm indication signal since Reg–31H was last read.

1: There is a change in the path alarm indication signal since Reg–31H was last read.

PRDII

This is the path Far-End Receive Failure (RDI) alarm interrupt bit. This bit resets when Reg–31H is being read.

0: No change in the path far-end receive failure alarm since Reg–31H was last read.

1: There is a change in the path far-end receive failure alarm since Reg–31H was last read.

BIPEI

This is the BIP–8 (B3) error interrupt bit. This bit resets when Reg–31H is being read.

0: No BIP–8 (B3) error detected since Reg–31H was last read.

1: BIP–8 (B3) error has been detected since Reg–31H was last read.

FEBEI

This is the path Far-End Block Error (FEBE) interrupt bit. This bit resets when Reg–31H is being read.

0: No path far-end block error detected since Reg–31H was last read.

1: Path far-end block error has been detected since Reg–31H was last read.

REG – 33H	Receive Path Overhead Processor Interrupt Enable Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	PSLE	R/W	0
6	Unused		
5	LOPE	R/W	0
4	Unused		
3	PAISE	R/W	0
2	PRDIE	R/W	0
1	BIPEE	R/W	0
0	FEBEE	R/W	0

PSLE

This bit controls whether a change in the Path Signal Label (PSL) generates an interrupt by asserting INTB LOW.

0: A change in the path signal label (PSL) will not generate an interrupt.

1: An interrupt will be generated if more than two consecutive non-13H C3 bytes are being detected in the path overhead.

LOPE

This bit controls whether a loss of pointer generates an interrupt by asserting INTB LOW.

0: A change in the loss of pointer state will not generate an interrupt.

1: A change in the loss of pointer state will generate an interrupt.

PAISE

This bit controls whether Path Alarm Indication Signal (PAIS) error generates an interrupt by asserting INTB LOW.

0: PAIS error will not generate an interrupt.

1: PAIS error will generate an interrupt.

PRDIE

This bit controls whether a path Remote Defect Indication (RDI) generates an interrupt by asserting INTB LOW.

0: A change in the path remote defect indication state will not generate an interrupt.

1: A change in the path remote defect indication state will generate an interrupt.

BIPEE

This bit controls whether BIP–8 (B3) error generates an interrupt by asserting INTB LOW.

0: BIP–8 (B3) error will not generate an interrupt.

1: BIP–8 (B3) error will generate an interrupt.

FEBEE

This bit controls whether line far end block error generates an interrupt by asserting INTB LOW.

0: Line far-end block error will not generate an interrupt.

1: Line far-end block error will generate an interrupt.

REG – 37H	Receive Path Signal Label Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	PSL[7]	R	
6	PSL[6]	R	
5	PSL[5]	R	
4	PSL[4]	R	
3	PSL[3]	R	
2	PSL[2]	R	
1	PSL[1]	R	
0	PSL[0]	R	

PSL[7:0]

This is the path signal label (C2) register byte. This register is either 13H or the first non-13H value detected in the received SONET data stream.

REG – 38H	Path BIP–8 (B3) Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	PBE[7]	R	0
6	PBE[6]	R	0
5	PBE[5]	R	0
4	PBE[4]	R	0
3	PBE[3]	R	0
2	PBE[2]	R	0
1	PBE[1]	R	0
0	PBE[0]	R	0

PBE[15:0]

Reg–38H and Reg–39H will be loaded with the number of path BIP–8 (B3) errors from an internal counter approximately 1 µs after a write operation is done to Reg–38H, Reg–39H, Reg–3AH, Reg–3BH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal BIP–8 (B3) error counter is reset to zero to begin another round of error accumulation. Reading Reg–38H and Reg–39H after the write yields the number of BIP–8 (B3) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 39H	Path BIP–8 (B3) Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	PBE[15]	R	0
6	PBE[14]	R	0
5	PBE[13]	R	0
4	PBE[12]	R	0
3	PBE[11]	R	0
2	PBE[10]	R	0
1	PBE[9]	R	0
0	PBE[8]	R	0

PBE[15:0]

Reg–38H and Reg–39H will be loaded with the number of path BIP–8 (B3) errors from an internal counter approximately 1 µs after a write operation is done to Reg–38H, Reg–39H, Reg–3AH, Reg–3BH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal BIP–8 (B3) error counter is reset to zero to begin another round of error accumulation. Reading Reg–38H and Reg–39H after the write yields the number of BIP–8 (B3) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 3AH	Path Far-End Block Error Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	PFE[7]	R	0
6	PFE[6]	R	0
5	PFE[5]	R	0
4	PFE[4]	R	0
3	PFE[3]	R	0
2	PFE[2]	R	0
1	PFE[1]	R	0
0	PFE[0]	R	0

PFE[15:0]

Reg–3AH and Reg–3BH will be loaded with the number of path FEBE (G1) errors from an internal counter approximately 1 µs after a write operation is done to Reg–38H, Reg–39H, Reg–3AH, Reg–3BH, or Reg–00H. At that time (1 µs after the write operation), these three registers are updated and the internal path FEBE error counter is reset to zero to begin another round of error accumulation. Reading Reg–3AH and Reg–3BH after the write yields the number of path FEBE (G1) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 3BH	Path Far End Block Error Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	PFE[15]	R	0
6	PFE[14]	R	0
5	PFE[13]	R	0
4	PFE[12]	R	0
3	PFE[11]	R	0
2	PFE[10]	R	0
1	PFE[9]	R	0
0	PFE[8]	R	0

PFE[15:0]

Reg–3AH and Reg–3BH will be loaded with the number of path FEBE (G1) errors from an internal counter approximately 1 µs after a write operation is done to Reg–38H, Reg–39H, Reg–3AH, Reg–3BH, or Reg–00H. At that time (1 µs after the write operation), these three registers are update and the internal path FEBE error counter is reset to zero to begin another round of error accumulation. Reading Reg–3AH and Reg–3BH after the write yields the number of path FEBE (G1) errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 3DH	Path Far-End Block Error Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	BLKBIP	R/W	0
4	Unused		
3	Unused		
2	Unused		
1	Unused		
0	Unused		

BLKBIP

This bit controls how path BIP–8 (B3) errors are accumulated.

0: BIP–8 (B3) errors are accumulated and reported in a bit basis.

1: BIP–8 (B3) errors are accumulated and reported in a block basis. Only one BIP–8 error is reported to the upstream path even if more than one path BIP–8 (B3) errors are detected.

REG – 40H	Transmit Path Overhead Processor Error Insertion Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	Unused		
1	DB3	R/W	0
0	PAIS	R/W	0

DB3

This bit generates a path BIP–8 error in the transmit data stream.

0: Normal operation.

1: The path BIP–8 (B3) byte is inverted, eight BIP–8 (B3) errors are thus generated per frame PAIS.

PAIS

This bit generates a path Alarm Indication Signal (AIS) in the transmit data stream.

0: Normal operation.

1: The whole synchronous payload envelope (SPE) together with the H1, H2, and H3 bytes are converted to 1 before scrambling.

REG – 41H	Transmit Path Overhead Processor Pointer Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	FTPTR	R/W	0
5	SOS	R/W	0
4	PLD	R/W	0
3	NDF	R/W	0
2	NSE	R/W	0
1	PSE	R/W	0
0	Unused		

FTPTR

This bit enables the insertion of the arbitrary payload pointer value into the last 10 bits of H1, H2. The NDF flag is not automatically changed by this operation.

0: Normal operation.

1: The bits contained in Arbitrary Pointer Register (APTR[9:0]) are inserted into H1 and H2 of the transmitted data stream. This bit is provided for creating pointer byte errors to diagnose the downstream system.

SOS

This is the stuff opportunity spacing bit which controls how often stuff events can occur.

0: Stuff event can occur in every other frame. Insertion of positive pointer movement or negative pointer movement can be done through writing to NSE and PSE (bit 2 and 1 of Reg–41H)

1: Stuff event can occur only once in every four frames. Insertion of positive pointer movement or negative pointer movement can be done through writing to NSE and PSE (bit 2 and 1 of Reg–41H)

PLD

This bit enables the insertion of the arbitrary payload pointer value into the last 10 bits of H1 and H2 bytes. The value in NDF[3:0] (Reg–46H, bit 7 – bit 4) will also be loaded into the new data flag (NDF) position of the H1 byte. PLD should be used instead of FTPTR for non-diagnostic payload pointer adjustments.

0: Normal operation.

1: The bits contained in Arbitrary Pointer Register (APTR[9:0]) are inserted into H1 and H2 of the transmit data stream. This operation will not affect the interpretation of the pointer in the received data stream, and will only be performed if the value stored in APTR[9:0] is >0 and < 782.

NDF

This is the new data flag (NDF) insertion control bit. This bit is ignored if PLD is set to 1.

0: The normal NDF pattern (0110) is being transmitted in the first four bytes of H1.

1: The value stored in NDF[3:0] (Reg–46H, bit 7–bit 4) are inserted into the first four bytes of H1.

NSE

This bit can be used to generate a negative pointer movement. This bit has to be first enabled by setting FIXPTR (Reg–05H, bit 5) to 1. This bit resets to zero automatically after every write to it.

0: Default state.

1: A single negative pointer adjustment will be made on the outgoing data stream. This bit will be cleared to zero immediately

PSE

This bit can be used to generate a positive pointer movement. This bit has to be first enabled by setting FIXPTR (Reg–05H, bit 5) to 1. This bit resets to zero automatically after every write to it.

0: Default state.

1: A single positive pointer adjustment will be made on the outgoing data stream. This bit will be cleared to zero immediately.

REG – 45H	Transmit Path Overhead Processor Arbitrary Payload Pointer Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	APTR[7]	R/W	0
6	APTR[6]	R/W	0
5	APTR[5]	R/W	0
4	APTR[4]	R/W	0
3	APTR[3]	R/W	0
2	APTR[2]	R/W	0
1	APTR[1]	R/W	0
0	APTR[0]	R/W	0

APTR[9:0]

Reg–45H and Reg–46H are the arbitrary payload pointer registers. This two registers are used to store the new payload pointer value to be loaded into H1and H2 of the transmitted data stream. The value loaded into these 10 bits has to be greater than or equal to zero and smaller than 782. A legal value stored in APTR[9:0] is not loaded into the data stream until PLD or FTPTR is toggled HIGH.

REG – 46H	Transmit Path Overhead Processor Arbitrary Payload Pointer Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	NDF[3]	R/W	1
6	NDF[2]	R/W	0
5	NDF[1]	R/W	0
4	NDF[0]	R/W	1
3	S[1]	R/W	0
2	S[2]	R/W	0
1	APTR[9]	R/W	0
0	APTR[8]	R/W	0

NDF[3:0]

These bits are used to store the arbitrary new data flag to be loaded into the transmit data stream. These bits are loaded when NDF is toggled HIGH or when PLD is toggled HIGH.

S[1:0]

These 2 bits are inserted into the 2 unused bits of H1 whenever PLD, NDF, or FTPTR are toggled HIGH.

APTR[9:0]

Reg–45H and Reg–46H are the arbitrary payload pointer registers. This two registers are used to store the new payload pointer value to be loaded into H1 and H2 of the transmitted data stream. The value loaded into these 10 bits has to be greater than or equal to zero and smaller than 782. A legal value stored in APTR[9:0] is not loaded into the data stream until PLD or FTPTR is toggled HIGH.

REG – 48H	Transmit Path Overhead Processor Signal Label Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	C2[7]	R/W	0
6	C2[6]	R/W	0
5	C2[5]	R/W	0
4	C2[4]	R/W	1
3	C2[3]	R/W	0
2	C2[2]	R/W	0
1	C2[1]	R/W	1
0	C2[0]	R/W	1

C2[7:0]

These bits are inserted in the C2 byte position in the transmit stream.

REG – 49H	Transmit Path Overhead Processor Path Status Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	FEBE[3]	R/W	0
6	FEBE[2]	R/W	0
5	FEBE[1]	R/W	0
4	FEBE[0]	R/W	0
3	PRDI	R/W	0
2	G1[2]	R/W	0
1	G1[1]	R/W	0
0	G1[0]	R/W	0

FEBE[3:0]

These bits are used to hold the FEBE value to be inserted into the transmitted data stream. After insertion of these bits into the FEBE location of the next possible frame, FEBE[3:0] will be reset. If the value written to these register bits can still be read back, it just mean that the insertion has not taken place yet.

PRDI

This bit is used to insert remote defect indication (RDI) into the transmitted data stream.

0: Normal operation. With the PRDI bit of G1 only affected by the setting of AUTOPRDI (Reg–01H, Bit 4) and the alarm conditions.

1: The PRDI bit of G1 is set to 1.

G1[2:0]

These bits are inserted into the unused bit positions of G1 of every frame.

REG – 50H	Receive ATM Cell Processor Control and Status Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	OOCDV	R	
6	RXPTYP	R/W	0
5	PASS	R/W	0
4	DISCOR	R/W	0
3	HCSPASS	R/W	0
2	HCSADD	R/W	1
1	DDSCR	R/W	0
0	FIFORST	R/W	0

OOCDV

This bit is the cell delineation status register.

0: This indicates that the cell delineation state machine is in the 'SYNC' state and ATM cells are passing though to the receive FIFO.

1: This indicates that the cell delineation state machine is in the 'PRESYNC' or 'HUNT' state.

RXPTYP

This bit controls whether odd or even parity is used for RXPRTY.

0: Odd parity is generated for RDAT[7:0].

1: Even parity is generated for RDAT[7:0].

PASS

This bit controls whether cells with VPI = 0 and VCI = 0 are dropped.

0: All cells with VPI = 0, VCI = 0 and header matching all the unmasked bits of Reg–52H are dropped.

1: No cell filtering is performed.

DISCOR

This bit controls whether header error (HCS) correction is performed.

0: Header error correction is performed. Single bit-errors detected in the header are corrected automatically.

1: Header error correction is not performed. Any HCS error detected is considered uncorrectable.

HCSPASS

This bit controls whether cells with HCS error are dropped.

0: All cells with an uncorrectable HCS error are dropped.

1: No cells are dropped if the cell delineation state machine is in SYNC state.

HCSADD

This bit controls whether the coset polynomial $x^6+x^4+x^2+1$ is added to the HCS byte before HCS comparison is performed.

0: No coset polynomial is added.

1: The coset polynomial $x^6+x^4+x^2+1$ is added to the HCS byte.

DDSCR

This bit controls whether cell payload descrambling is performed.

0: Cell payload descrambling is performed.

1: Cell payload descrambling is not performed.

FIFORST

This bit is the receive FIFO reset bit.

0: Normal receive FIFO operation.

1: All receive FIFO locations are reset and the receive FIFO will ignore all writes.

REG – 51H	Receive ATM Cell Processor Interrupt Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	OOCDE	R/W	0
6	HCSE	R/W	0
5	FIFOE	R/W	0
4	OOCDI	R	
3	CHCSI	R	
2	UHCSI	R	
1	FOVRI	R	
0	Unused		

OOCDE

This bit controls whether a change in cell delineation state generates an interrupt by asserting INTB LOW.

0: A change in the cell delineation state will not generate an interrupt.

1: A change in the cell delineation state will generate an interrupt.

HCSE

This bit controls whether an HCS error generates an interrupt by asserting INTB LOW.

0: HCS errors will not generate an interrupt.

1: A correctable or uncorrectable HCS error will both generate an interrupt.

FIFOE

This bit controls whether receive FIFO overflow will generate an interrupt by asserting INTB LOW.

0: Receive FIFO overflow will not generate an interrupt.

1: Receive FIFO overflow will generate an interrupt.

OOCDI

This is the change of cell delineation interrupt bit. This bit resets as Reg–51H is being read.

0: There is no change in the loss of cell delineation state.

1: There is a change from the PRESYNC state to SYNC state or from the SYNC state to the HUNT state.

CHCSI

This is the correctable HCS error detection bit. This bit resets as Reg–51H is being read.

0: No correctable HCS error has been detected since Reg–51H was last read.

1: One or more than one correctable HCS errors have been detected since Reg–51H was last read.

UHCSI

This is the uncorrectable HCS error detection bit. This bit resets as Reg–51H is being read.

0: No uncorrectable HCS error has been detected since Reg–51H was last read.

1: One or more than one uncorrectable HCS errors have been detected since Reg–51H was last read.

FOVRI

This is the receive FIFO overflow interrupt bit. This bit resets as Reg–51H is being read.

0: No receive FIFO overflow has occurred since Reg–51H was last read.

1: Receive FIFO overflow has occurred since Reg–51H was last read.

REG – 52H	Receive ATM Cell Processor Match Header Pattern Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	GFC[3]	R/W	0
6	GFC[2]	R/W	0
5	GFC[1]	R/W	0
4	GFC[0]	R/W	0
3	PTI[2]	R/W	0
2	PTI[1]	R/W	0
1	PTI[0]	R/W	0
0	CLP	R/W	0

GFC[3:0]

These are the Generic Flow Control (GFC) register bits. If the PASS bit (Reg–50H, bit 5) is LOW, ATM cells with VPI = 0, VCI = 0, and with other parts of their header matching all the unmasked bits of this register will be dropped. Each bit of this register can be masked by its corresponding bit in Reg–53H. Masked bits are not compared.

PTI[2:0]

These are the Payload Type Indicator (PTI) register bits. If the PASS bit (Reg–50H, bit 5) is LOW, ATM cells with VPI = 0, VCI = 0, and with other parts of their header matching all the unmasked bits of this register will be dropped. Each bit of this register can be masked by its corresponding bit in Reg–53H. Masked bits are not compared.

CLP

This is the Cell Loss Priority (CLP) register bit. If the PASS bit (Reg–50H, bit 5) is LOW, ATM cells with VPI = 0, VCI = 0,and with other parts of their header matching all the unmasked bits of this register will be dropped. Each bit of this register can be masked bits corresponding bit in Reg–53H. Masked bits are not compared.

REG – 53H	Receive ATM Cell Processor Match Header Mask Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	MGFC[3]	R/W	0
6	MGFC[2]	R/W	0
5	MGFC[1]	R/W	0
4	MGFC[0]	R/W	0
3	MPTI[2]	R/W	0
2	MPTI[1]	R/W	0
1	MPTI[0]	R/W	0
0	MCLP	R/W	0

MGFC[3:0]

This is the mask for the Generic Flow Control register. A HIGH in any bit of this register unmasks the corresponding bit of Reg–52H and allows it to be compared with the current ATM cell. If PASS (Reg–50H, bit 5) is LOW, ATM cells with VPI = 0, VCI = 0, and other parts of their header matching all the unmasked bits of Reg–52H are dropped.

MPTI[2:0]

This is the mask for the Payload Type Indicator register. A HIGH in any bit of this register unmasks the corresponding bit of Reg–52H and allows it to be compared with the current ATM cell. If PASS (Reg–50H, bit 5) is LOW, ATM cells with VPI = 0, VCI = 0, and other parts of their header matching all the unmasked bits of Reg–52H are dropped.

MCLP

This is the mask for the Cell Loss Priority (CLP) register. A HIGH in any bit of this register unmasks the corresponding bit of Reg–52H and allows it to be compared with the current ATM cell. If PASS (Reg–50H, bit 5) is LOW, ATM cells with VPI = 0, VCI = 0, and other parts of their header matching all the unmasked bits of Reg–52H are dropped.

REG – 54H	Receive ATM Cell Processor Correctable HCS Error Count Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	CHCS[7]	R	
6	CHCS[6]	R	
5	CHCS[5]	R	
4	CHCS[4]	R	
3	CHCS[3]	R	
2	CHCS[2]	R	
1	CHCS[1]	R	
0	CHCS[0]	R	

CHCS[7:0]

Reg–54H and Reg–55H will load the number of correctable HCS errors from an internal counter approximately 200 ns after a write operation is done to Reg–54H, Reg–55H, or Reg–00H. At that time (200 ns after the write operation), this register is updated and the internal correctable HCS error counter is reset to zero to begin another round of error accumulation. Reading Reg–54H and Reg–55H after the write yields the number of correctable HCS errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 55H	Receive ATM Cell Processor Uncorrectable HCS Error Count Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	UHCS[7]	R	
6	UHCS[6]	R	
5	UHCS[5]	R	
4	UHCS[4]	R	
3	UHCS[3]	R	
2	UHCS[2]	R	
1	UHCS[1]	R	
0	UHCS[0]	R	

UHCS[7:0]

Reg–54H and Reg–55H will load the number of uncorrectable HCS errors from an internal counter approximately 200 ns after a write operation is done to Reg–54H, Reg–55H, or Reg–00H. At that time (200 ns after the write operation), this register is updated and the internal uncorrectable HCS error counter is reset to zero to begin another round of error accumulation. Reading Reg–54H and Reg.–55H after the write yields the number of uncorrectable HCS errors accumulated since the counter was last reset, if overflow has not occurred.

REG – 56H	Receive ATM Cell Processor Receive Cell Counter Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	RCELL[7]	R	
6	RCELL[6]	R	
5	RCELL[5]	R	
4	RCELL[4]	R	
3	RCELL[3]	R	
2	RCELL[2]	R	
1	RCELL[1]	R	
0	RCELL[0]	R	

RCELL[18:0]

Reg–56H, Reg–57H, and Reg–58H will load the number of cells received from an internal counter approximately 200ns after a write operation is done to Reg–54H, Reg–55H, Reg–56H, Reg–57H, Reg–58H, or Reg–00H. At that time (200ns after the write operation), this register is updated and the internal receive cell counter is reset to zero to begin another round of accumulation. Reading Reg–56H, Reg–57H, and Reg–58H after the write yields the number of cells received since the counter was last reset, if overflow has not occurred.

REG – 57H	Receive ATM Cell Processor Receive Cell Counter Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	RCELL[15]	R	
6	RCELL[14]	R	
5	RCELL[13]	R	
4	RCELL[12]	R	
3	RCELL[11]	R	
2	RCELL[10]	R	
1	RCELL[9]	R	
0	RCELL[8]	R	

RCELL[18:0]

Reg–56H, Reg–57H, and Reg–58H will load the number of cells received from an internal counter approximately 200 ns after a write operation is done to Reg–54H, Reg–55H, Reg–56H, Reg–57H, Reg–58H, or Reg–00H. At that time (200 ns after the write operation), this register is updated and the internal receive cell counter is reset to zero to begin another round of accumulation. Reading Reg–56H, Reg–57H, and Reg–58H after the write yields the number of cells received since the counter was last reset, if overflow has not occurred.

REG – 58H	Receive ATM Cell Processor Receive Cell Counter Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	RCELL[18]	R	
1	RCELL[17]	R	
0	RCELL[16]	R	

RCELL[18:0]

Reg–56H, Reg–57H, and Reg–58H will load the number of cells received from an internal counter approximately 200 ns after a write operation is done to Reg–54H, Reg–55H, Reg–56H, Reg–57H, Reg–58H, or Reg–00H. At that time (200 ns after the write operation), this register is updated and the internal receive cell counter is reset to zero to begin another round of accumulation. Reading Reg–56H, Reg–57H, and Reg–58H after the write yields the number of cells received since the counter was last reset, if overflow has not occurred.

REG – 59H	Receive ATM Cell Processor Receive Configuration Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	RGFCE[3]	R/W	1
6	RGFCE[2]	R/W	1
5	RGFCE[1]	R/W	1
4	RGFCE[0]	R/W	1
3	FSEN	R/W	1
2	RCALEVEL0	R/W	1
1	HCSFTR[1]	R/W	0
0	HCSFTR[0]	R/W	0

RGFCE[3:0]

This is the Receive Generic Flow Control Enable register. Each bit is logical ANDed with its corresponding bit in the ATM cell header. RGFCE[3] corresponds to the most significant bit of the GFC header. If RGFC[x] is set LOW, then bit x of the serial RGFC output (pin 59) will appear LOW.

FSEN

This is the fix stuff expectation bit. This command only affects STS–1 frames.

0: No fix stuff bytes are expected in the STS–1 payload.

1: Fix stuff bytes are expected in Column 30 and 59 of the received STS–1 frame.

RCALEVEL0

This is the receive cell available (RCA) pin empty definition control register.

0: RCA is an active LOW indication for the receive FIFO being 4 bytes from empty.

1: RCA is an active LOW indication for the receive FIFO being empty.

HCSFTR[1:0]

This is the HCS cell acceptance threshold register. These bits control how many consecutive error-free cells are needed for the Receive ATM cell processor to convert from detection mode to correction mode.

11: 7 cells with no HCS error is needed before the 8th cell is accepted. Correction mode is entered immediately after that.

10: 3 cells with no HCS error is needed before the 4th cell is accepted. Correction mode is entered immediately after that.

01: 1 cell with no HCS error is needed before the 2nd cell is accepted. Correction mode is entered immediately after that.

00: All cell with no HCS error is accepted. Correction mode is entered immediately after that.

REG – 60H	Transmit ATM Cell Processor Control and Status Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	FIFOE	R/W	0
6	TSOCI	R	
5	FOVRI	R	
4	DHCS	R/W	0
3	Unused		
2	HCSADD	R/W	1
1	DDSCR	R/W	0
0	FIFORST	R/W	0

FIFOE

This bit controls whether transmit FIFO overflow or misplaced transmit start of cell (TSOC) will generate an interrupt.

0: Transmit FIFO overflow and misplaced TSOC will not generate an interrupt.

1: Transmit FIFO overflow or misplaced TSOC (TSOC appearing not with the first byte of an ATM cell) will generate an interrupt.

TSOCI

This is the transmit start of cell interrupt bit. This bit resets as Reg–60H is being read.

0: No TSOC error has occurred since Reg–60H was last read.

1: TSOC has occurred at times other than at the beginning of an ATM cell. The internal 53-byte cell length counter is reset to zero immediately if such an error occurs and the incomplete ATM cell is discarded.

FOVRI

This is the transmit FIFO overflow interrupt bit. This bit resets as Reg–60H is being read.

0: No transmit FIFO overflow has occurred since Reg–60H was last read.

1: Transmit FIFO overflow has occurred since Reg–60H was last read.

HCSADD

This bit controls whether the coset polynomial $x^6+x^4+x^2+1$ is added to the HCS byte before the ATM cell is inserted into the Synchronous Payload Envelope (before SONET scrambling if enabled).

0: No coset polynomial is added.

1: The coset polynomial $x^6+x^4+x^2+1$ is added to the HCS byte. This is equivalent to substituting the HCS byte with (HCS byte XOR 01010101).

DDSCR

This bit controls whether cell payload scrambling is performed.

0: Cell payload scrambling is performed.

1: Cell payload scrambling is not performed.

FIFORST

This bit is the transmit FIFO reset bit.

0: Normal transmit FIFO operation.

1: All transmit FIFO locations are reset and the transmit FIFO will ignore all writes.

REG – 61H	Transmit ATM Cell Processor Unassigned Cell Header Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	GFC[3]	R/W	0
6	GFC[2]	R/W	0
5	GFC[1]	R/W	0
4	GFC[0]	R/W	0
3	PTI[2]	R/W	0
2	PTI[1]	R/W	0
1	PTI[0]	R/W	0
0	CLP	R/W	0

GFC[3:0]

These are the transmit Generic Flow Control (GFC) register bits. The bits in this register are appended to VPI = 0, and VCI = 0 before adding to the transmit data stream as idle cells. Idle cells are transmitted whenever there are no complete ATM cells in the transmit FIFO.

PTI[2:0]

These are the transmit Payload Type Indicator (PTI) register bits. The bits in this register are appended to VPI = 0, and VCI = 0 before adding to the transmit data stream as idle cells. Idle cells are transmitted whenever there are no complete ATM cells in the transmit FIFO.

CLP

This is the transmit Cell Loss Priority (CLP) register bit. The bits in this register are appended to VPI = 0, and VCI = 0 before adding to the transmit data stream as idle cells. Idle cells are transmitted whenever there are no complete ATM cells in the transmit FIFO.

REG – 62H	Transmit ATM Cell Processor Unassigned Cell Payload Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	ICP[7]	R/W	0
6	ICP[6]	R/W	1
5	ICP[5]	R/W	1
4	ICP[4]	R/W	0
3	ICP[3]	R/W	1
2	ICP[2]	R/W	0
1	ICP[1]	R/W	1
0	ICP[0]	R/W	0

ICP[7:0]

This register contains the octet to be placed in each byte of the transmitted idle cells. When there are no user ATM cells available for transmission, the Transmit ATM Cell Processor generates its own idle cells based on setting in Reg–61H and 62H. Idle cells allow CY7C955 to perform cell rate decoupling.

REG – 63H	Transmit ATM Cell Processor FIFO Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	TXPTYP	R/W	0
6	TXPRTYE	R/W	0
5	Unused		
4	TXPRTYI	R	
3	FIFODP[1]	R/W	0
2	FIFODP[0]	R/W	0
1	TCALEVEL0	R/W	0
0	Unused		0

TXPTYP

This is the polarity control bit for the interpretation of TXPRTY.

0: TXPRTY is the odd parity input for TDAT[7:0].

1: TXPRTY is the even parity input for TDAT[7:0].

TXPRTYE

This is the transmit parity error interrupt enable register.

0: Transmit parity error will not pull INTB (pin 108) LOW but will still be indicated on TXPRTYI.

1: Transmit parity error will pull INTB (pin 108) LOW as well as setting TXPRTYI.

TXPRTYI

This is the transmit parity error interrupt register. This bit resets when Reg–63H is being read.

0: No transmit parity error has been detected since Reg–63H was last read.

1: Transmit parity error has been detected since Reg–63H was last read.

FIFODP[1:0]

This bit controls the transmit cell available (TCA) pin definition. Note that this register only determines when TCA (pin 86) is to be deasserted. The transmit FIFO is always 4 cells deep regardless of the setting of this register. This means that interrupt for FIFO overflow, if enabled by FIFOE (Reg–60H, bit 7), will only occur if a write is attempted on a FIFO that is already filled up with all 4 cells.

11: TCA will go LOW when transmit FIFO is 1 cell full (if TCALEVEL = 1) or 4 bytes away from 1 cell full (if TCALEVEL = 0).

10: TCA will go LOW when transmit FIFO is 2 cells full (if TCALEVEL = 1) or 4 bytes away from 2 cells full (if TCALEVEL = 0).

01: TCA will go LOW when transmit FIFO is 3 cells full (if TCALEVEL = 1) or 4 bytes away from 3 cells full (if TCALEVEL = 0).

00: TCA will go LOW when transmit FIFO is 4 cells full (if TCALEVEL = 1) or 4 bytes away from 4 cells full (if TCALEVEL = 0).

TCALEVEL0

This is the transmit cell available (TCA) pin transition definition control register.

0: TCA will go LOW when transmit FIFO is N cells full. N is determined by value in FIFODP[1:0] (Reg–63H, bit 2–3).

1: TCA will stay LOW when transmit FIFO is within 4 bytes from N cells full. N is determined by value in FIFODP[1:0] (Reg–63H, bit 2–3).

REG – 64H	Transmit ATM Cell Processor Transmit Cell Counter Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	TCELL[7]	R	0
6	TCELL[6]	R	0
5	TCELL[5]	R	0
4	TCELL[4]	R	0
3	TCELL[3]	R	0
2	TCELL[2]	R	0
1	TCELL[1]	R	0
0	TCELL[0]	R	0

TCELL[18:0]

Reg–64H, Reg–65H, and Reg–66H will load the number of cells transmitted from an internal counter approximately 200 ns after a write operation is done to Reg–64H, Reg–65H, Reg–66H, or Reg–00H. At that time (200 ns after the write operation), this register is updated and the internal transmit cell counter is reset to zero or one (depending on whether a cell transmission has occurred while the write occurs) to begin another round of accumulation. Reading Reg–64H, Reg–65H, and Reg–66H after the write yields the number of cell transmitted since the counter was last reset, if overflow has not occurred. TCELL[18:0] should be polled once a second to prevent the register from being saturated.

REG – 65H	Transmit ATM Cell Processor Transmit Cell Counter Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	TCELL[15]	R	0
6	TCELL[14]	R	0
5	TCELL[13]	R	0
4	TCELL[12]	R	0
3	TCELL[11]	R	0
2	TCELL[10]	R	0
1	TCELL[9]	R	0
0	TCELL[8]	R	0

TCELL[18:0]

Reg–64H, Reg–65H, and Reg–66H will load the number of cells transmitted from an internal counter approximately 200 ns after a write operation is done to Reg–64H, Reg–65H, Reg–66H, or Reg–00H. At that time (200 ns after the write operation), this register is updated and the internal transmit cell counter is reset to zero or one (depending on whether a cell transmission has occurred while the write occurs) to begin another round of accumulation. Reading Reg–64H, Reg–65H, and Reg–66H after the write yields the number of cell transmitted since the counter was last reset, if overflow has not occurred. TCELL[18:0] should be polled once a second to prevent the register from being saturated.

REG – 66H	Transmit ATM Cell Processor Transmit Cell Counter Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	TCELL[18]	R	0
1	TCELL[17]	R	0
0	TCELL[16]	R	0

TCELL[18:0]

Reg–64H, Reg–65H, and Reg–66H will load the number of cells transmitted from an internal counter approximately 200 ns after a write operation is done to Reg–64H, Reg–65H, Reg–66H, or Reg–00H. At that time (200 ns after the write operation), this register is updated and the internal transmit cell counter is reset to zero or one (depending on whether a cell transmission has occurred while the write occurs) to begin another round of accumulation. Reading Reg–64H, Reg–65H, and Reg–66H after the write yields the number of cells transmitted since the counter was last reset, if overflow has not occurred. TCELL[18:0] should be polled once a second to prevent the register from being saturated.

REG – 67H	Transmit ATM Cell Processor Transmit Configuration Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	TGFCE[3]	R/W	0
6	TGFCE[2]	R/W	0
5	TGFCE[1]	R/W	0
4	TGFCE[0]	R/W	0
3	FSEN	R/W	1
2	H4INSB	R/W	0
1	FIXBYTE[1]	R/W	0
0	FIXBYTE[0]	R/W	0

TGFCE[3:0]

This is the Transmit Generic Flow Control Enable register. Each bit of this register corresponds to a bit in the GFC field of the transmitted ATM cell headers. If TGFCE[x] is set HIGH, bit x of the GFC field in the transmitted ATM cell headers will be using the bit value collected from the TGFC (pin 52) pin (see description of Drop Side Transmit Interface). If TGFCE[x] is LOW, bit x will be derived from either TDAT (if transmit FIFO has at least one cell available) or from the Idle/Unassigned header register (if transmit FIFO has less than 1 cell available).

FSEN

This is the fix stuff enable bit. This bit will only affect the STS–1 frame.

0: No stuffing is performed.

1: Column 30 and 59 of the STS–1 frame contains fix stuff bytes. The contents for the fix stuff byte is controlled by FIXBYTE[1:0] (Reg–67H, bit 0 –1).

H4INSB

This bit controls the contents of H4 byte.

0: H4 byte represents the cell indicator offset value.

1: H4 byte is set to 00H.

FIXBYTE[1:0]

This register holds the number to be used in the fixed byte columns.

11: FFH is inserted into the fixed byte columns.

10: AAH is inserted into the fixed byte columns.

01: 55H is inserted into the fixed byte columns.

00: 00H is inserted into the fixed byte columns.

REG – 80H	CY7C955 Test Control Register		
BIT POSITION	NAME	READ/WRITE	DEFAULT
7	Unused		
6	Unused		
5	Unused		
4	Unused		
3	Unused		
2	Unused		
1	HIZDATA	W	
0	HIZIO	R/W	0

HIZDATA

This is the data bus three-state control bit.

0: Normal operation.

1: This data bus is held at HIGH impedance. Register reading is disabled but writing is still possible.

HIZIO

This is the input output three-state control bit.

0: Normal operation.

1: All I/Os except the data bus are being held at the HIGH impedance state. The CY7C955 read/write is still possible.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –40°C to +125°C

Ambient Temperature under Bias ..... –40°C to +85°C

Supply Voltage to Ground Potential ..... –0.5V to +6.0V

DC Input Voltage..... –0.5V to +7.0V

DC Input Current .....±20 mA

Static Discharge Voltage.....± 2000V (per MIL-STD-883, Method 3015)

Latch-Up Current.....±100 mA

Lead Temperature .....300°C

Maximum Junction Temperature .....155°C

Maximum Power Dissipation ..... 1.5 W

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

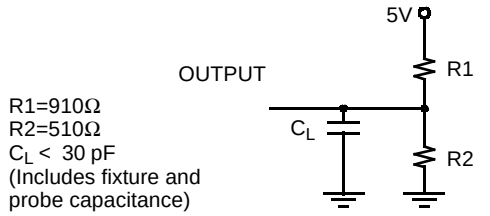
Parameter	Description	Test Conditions	Min.	Max.	Unit
PECL compatible Input Pins (RXD±, RRCLK±, ALOS± TRCLK±)					
V_{IHP}	Input HIGH Voltage			V_{CC}[1]	V
V_{ILP}	Input LOW Voltage		2.5		V
V_{IDIFF}	Input Differential Voltage		200	2500	mV
I_{IHP}	PECL Input HIGH Current[3]	$V_{IN} = V_{CC}$[2]		500	µA
I_{ILP}	PECL Input LOW Current[3]	V_{IN} = 2.5	–200		µA
PECL compatible Output Pins (RXDO±, TXD±, TXC±)					
V_{OHP}	Output HIGH Voltage	Terminated by 50Ω to V_{CC}[2] –1.33V	V_{CC}[2] –1.03	V_{CC}[2] –0.7	V
V_{OLP}	Output LOW Voltage		V_{CC}[2] –1.92	V_{CC}[2] –1.62	V
V_{ODIFF}	Output Differential Voltage	$0.75V_{AVG}$	0.6[6]		V
PECL compatible Input Pin (ALOS–) When ALOS+ is grounded					
V_{SIHP}	Input HIGH Voltage		V_{CC}[2] –1.03		V
V_{AILP}	Input LOW Voltage			V_{CC}[2] –1.62	V
TTL compatible Input Pins					
V_{IHT}	Input HIGH Voltage		2.0	V_{DD} +0.3	V
V_{ILT}	Input LOW Voltage		–0.3	0.8	V
I_{IHPU}	Input HIGH Current for Internal Pull-Up Pins	$V_{IH} = V_{DD}$	–10	10	µA
I_{ILPU}	Input LOW Current for Internal Pull-Up Pins[3]	V_{IL} = 0V	–200	–20	µA
I_{IHPD}	Input HIGH Current for Internal Pull-Down Pins[3]	$V_{IH} = V_{DD}$	20	200	µA
I_{ILPD}	Input LOW Current for Internal Pull-Down Pins[3]	V_{IL} = 0V	–10	10	µA
I_{IH}	Input HIGH Current for Pins Without Pull-Up or Pull-Down Resistors[3]	$V_{IH} = V_{DD}$	–10	10	µA
I_{IL}	Input LOW Current for Pins Without Pull-Up or Pull-Down Resistors[3]	V_{IL} = 0V	–10	10	µA
TTL compatible Output Pins					
V_{OLT}	Output LOW Voltage	V_{DD} = 4.75V, I_{OL} = 12 mA for INTB and TCLK and 8 mA for all others		0.4	V
V_{OHT}	Output HIGH Voltage[4]	V_{DD} = 4.75V, I_{OH} = 12 mA for TCLK and 8 mA for all others	2.4		V
I_{OZ}	Three-state Leakage	DATA[0:7]	–10	10	µA
I_{OST}	Output Short Circuit Current[4]	V_{OUT}=0V[5]	–15	–90	mA
Operating Current					
I_{DD}	Operational Current	Rate 0 = 0 (51.84 Mbps, STS–1) Rate 0 = 1 (155.52 Mbps, STS–3c/ STM–1)		210[7]	mA
I_{DDS}	Standby Current	RSTB = 0, or RESET (Reg–00H, bit 7) = 1		75	mA

Notes:
2. RXVDD for RXD±, RRCLK±, and ALOS±, RXDO±; TXVDD for TRCLK±, TXD± and TXC±.
3. Current flowing out of the chip has a positive value, current flowing into the chip has a negative value.
4. Maximum leakage current of INTB output at V_{OHT} = 900 µA.
5. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
6. Typical is $0.75V_{AVG}$.
7. Conditions: Outputs unloaded; V_{DD} = 5.5V; TXD ± = RXD ± = OPEN.

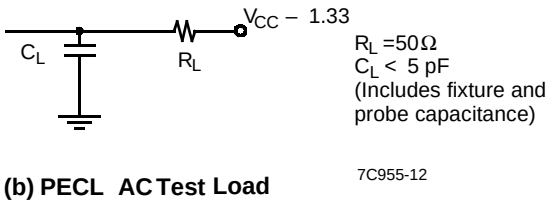
Capacitance

Parameter	Description	Max.	Unit
C_{IN}	Input pin capacitance	7	pF
C_{OUT}	Output pin capacitance	7	pF
C_{IO}	Input / Output pin capacitance	7	pF

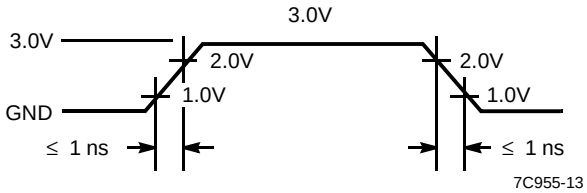
AC Test Loads and Waveforms



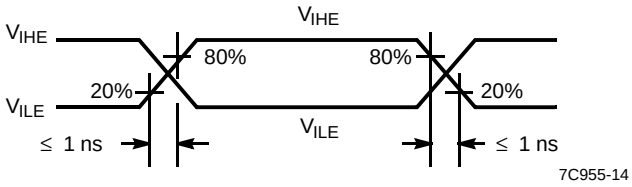
(a) TTL AC Test Load



(b) PECL AC Test Load



(c) TTL Input Test Waveform



(d) PECL Input Test Waveform

Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
Microprocessor Interface Read Cycle				
t_{SAR}	Valid Address to Read Set-Up	25		ns
t_{HRA}	Read to Address Invalid Hold	5		ns
t_{SAL}	Valid Address to Address Latch Enable Set-Up	20		ns
t_{HLA}	Address Latch Enable to Address Invalid Hold	10		ns
t_{PL}	Address Latch Enable Pulse Width	20		ns
t_{SLR}	Address Latch Enable to Read Set-Up	0		ns
t_{HRL}	Read to Address Latch Enable Hold	5		ns
t_{SRD}	Read to Valid Data Set-Up		80	ns
t_{HRD}	Read to Data Invalid Hold		20	ns
t_{SRI}	Read to Interrupt Inactive		50	ns
Microprocessor Interface Write Cycle				
t_{SAW}	Valid Address to Write Set-Up	25		ns
t_{SDW}	Valid Data to Write Set-Up	20		ns
t_{SAL}	Valid Address to Address Latch Enable Set-Up	20		ns
t_{HLA}	Address Latch Enable to Address Invalid Hold	10		ns
t_{PL}	Address Latch Enable Pulse Width	20		ns
t_{SLW}	Address Latch Enable to Write Set-Up	0		ns

Switching Characteristics Over the Operating Range (continued)

Parameter	Description		Min.	Max.	Unit
t_{HWL}	Write to Address Latch Enable Hold		5		ns
t_{HWD}	Write to Data Invalid Hold		5		ns
t_{HWA}	Write to Address Invalid Hold		5		ns
t_{PW}	Write Pulse Width		40		ns
Line Interface (Receive Side) Timing					
t_R	RRCLK± Duty Cycle	19.44 MHz or 6.48 MHz (RBYP = 0)	30	70	%
f_R	RRCLK± Frequency Tolerance[8, 9]		–250	250	ppm
t_{SDC}	RXD± Stable to RRCLK± Rising Edge Setup Time. R_{BYP} = 1		2		ns
t_{HCD}	RRCLK± State Change to RXD Unstable Hold Time. R_{BYP} = 1		1		ns
Receive Side Alarm Timing					
t_{DCR}	RCLK HIGH to RALM or RFP Valid Delay		2	20	ns
Line Interface (Transmit Side) Timing					
t_T	TRCLK± Duty Cycle	19.44 MHz or 6.48 MHz (TBYP = 0)	30	70	%
f_T	TRCLK± Frequency Tolerance		–250	250	ppm
t_{DTO}	TCLK HIGH to TFPO Valid Delay		3	20	ns
t_{DTD}	TXC± LOW to TXD± Valid Delay		–2	2	ns
UTOPIA Interface (Receive Side) Timing [TSEN = 0]					
f_{RF}	RFCLK Frequency			33	MHz
t_{RF}	RFCLK Duty Cycle		40	60	%
t_{SRC}	RRDENB Stable to RFCLK HIGH Set-Up		10		ns
t_{HCR}	RFCLK HIGH to RRDENB Unstable Hold		1		ns
t_{DCD}	RFCLK HIGH to RSOC / RCA / RXPRTY / RDAT [7:0] Valid Delay		2	20	ns
UTOPIA Interface (Receive Side) Timing [TSEN = 1]					
f_{RF}	RFCLK Frequency			33	MHz
t_{RF}	RFCLK Duty Cycle		40	60	%
t_{SRC}	RRDENB Stable to RFCLK HIGH Set-Up		10		ns
t_{HCR}	RFCLK HIGH to RRDENB Unstable Hold		1		ns
t_{DCA}	RFCLK HIGH to RCA Valid Delay		2	20	ns
t_{DCD}	RFCLK HIGH to RSOC / RXPRTY / RDAT [7:0] Valid Delay		2	20	ns
t_{DCT}	RFCLK HIGH to RSOC / RXPRTY / RDAT [7:0] Three-state Delay		2	20	ns
GFC (RECEIVE SIDE) TIMING					
t_{DCG}	RCLK HIGH to RGFC / RCP Valid Delay		–1	10	ns
UTOPIA INTERFACE (TRANSMIT SIDE) TIMING					
f_{TF}	TFCLK Frequency			33	MHz
t_{TF}	TFCLK Duty Cycle		40	60	%
t_{STC}	TWRENB / TDAT[7:0] / TXPRTY / TSOC Stable to TFCLK HIGH Set-Up		10		ns

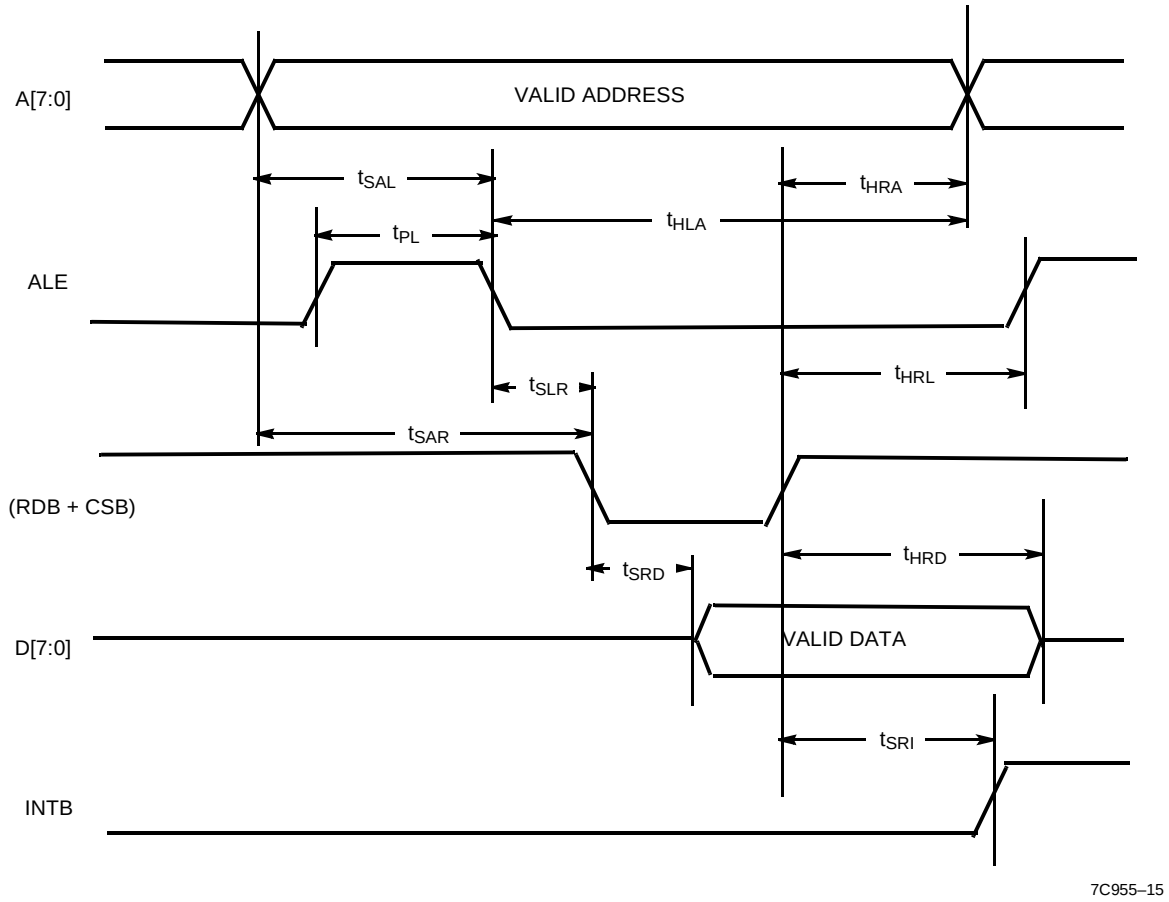
Notes:
8. Not Tested.
9. See description on Receive Clock Recovery (RCR) page 10

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	Min.	Max.	Unit
t_{HCT}	TFCLK HIGH to TWRENB / TDAT[7:0] / TXPRTY / TSOC Unstable Hold	1		ns
t_{DTT}	TFCLK HIGH to TCA Valid Delay	2	20	ns
GFC (Transmit Side) Timing				
t_{SGT}	TGFC Stable to TCLK High Set-Up	10		ns
t_{HTG}	TCLK High to TGFC Unstable Hold	1		ns
t_{DTP}	TCLK High to TCP Valid Delay	–1	10	ns

Switching Waveforms

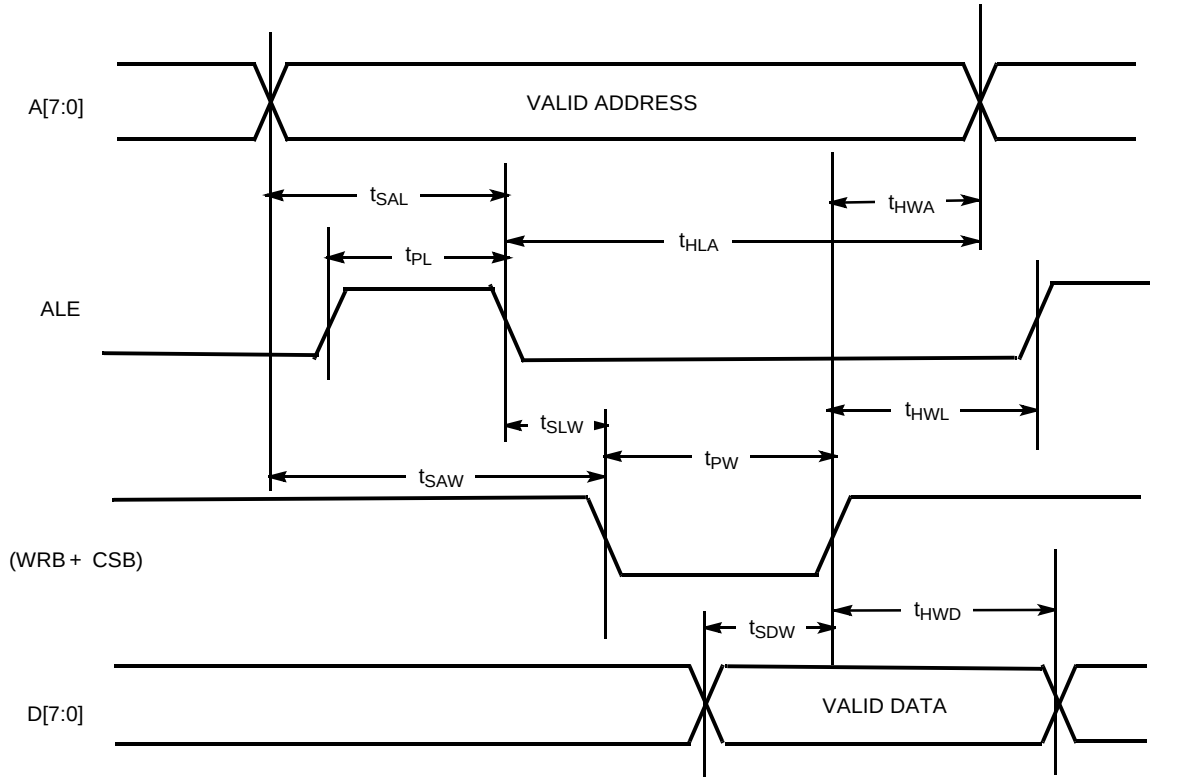
Microprocessor Interface Read Cycle



7C955–15

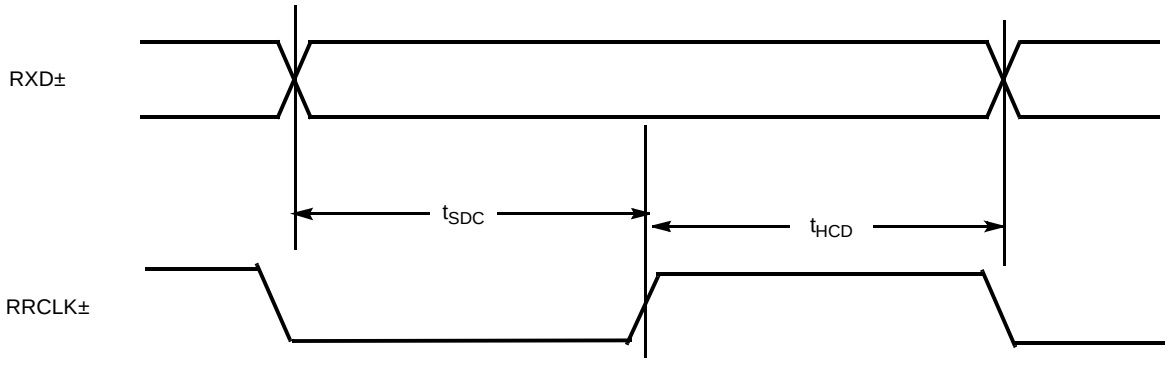
Switching Waveforms (continued)

Microprocessor Interface Write Cycle



7C955–16

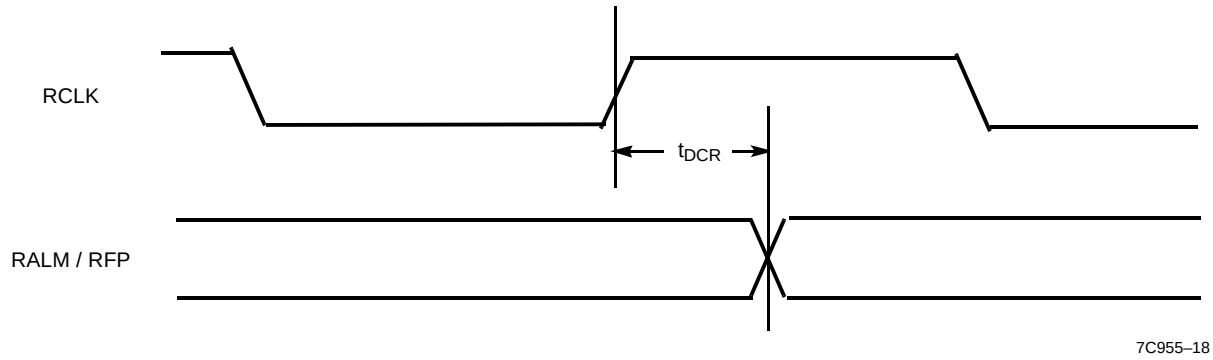
Receive Side Line Interface Timing



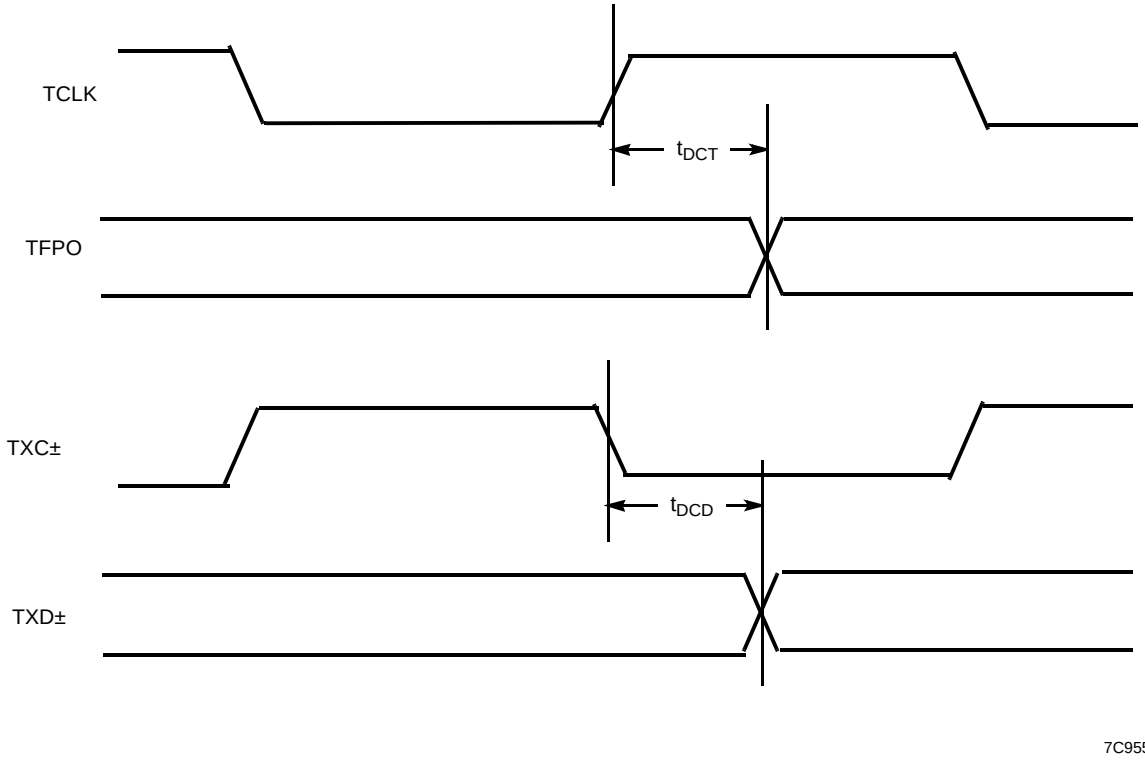
7C955–17

Switching Waveforms (continued)

Receiver Alarm Interface Timing

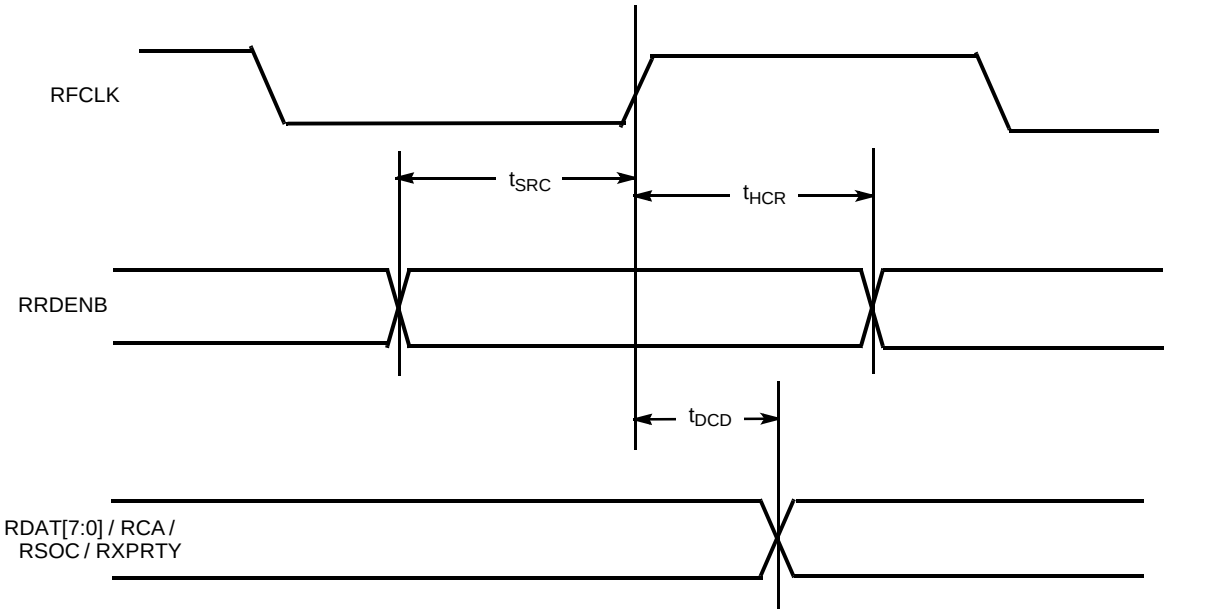


Transmit Side Line Interface Timing



Switching Waveforms (continued)

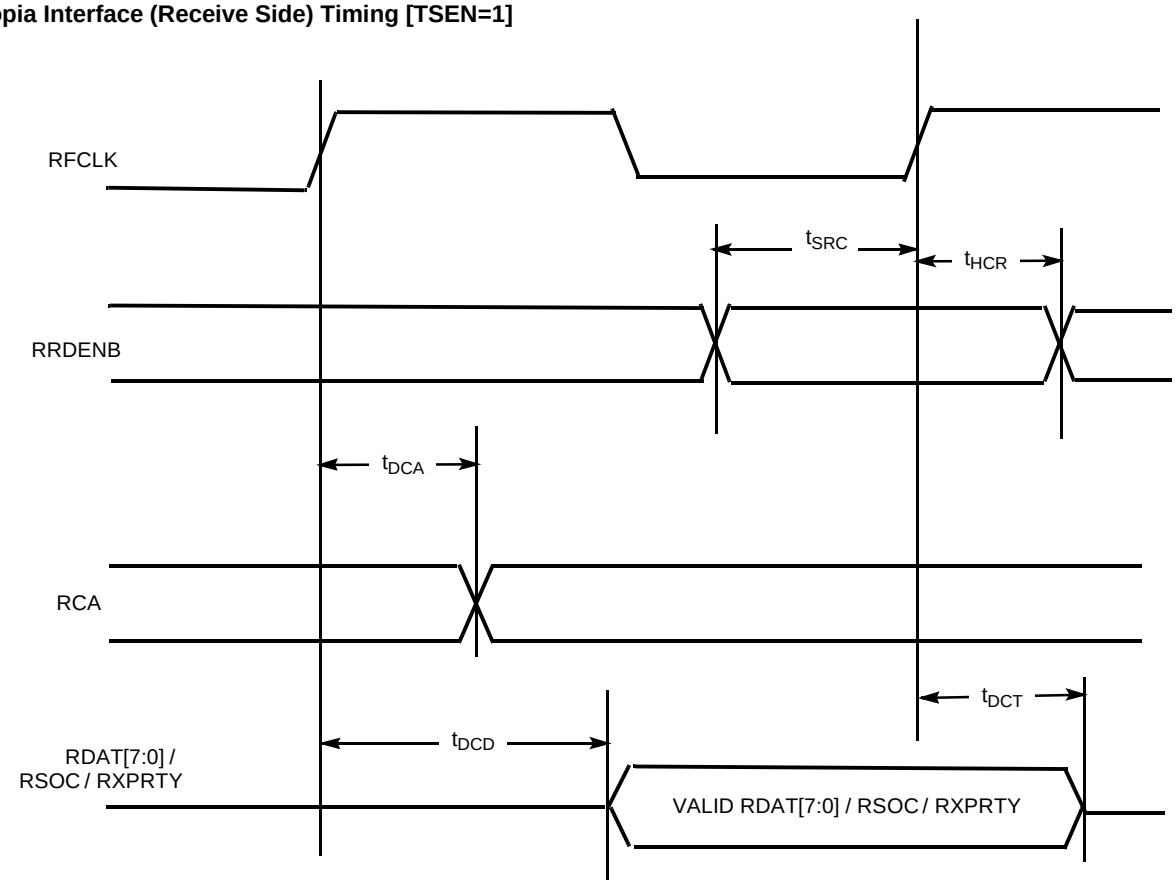
Utopia Interface (Receive Side) Timing [TSEN = 0]



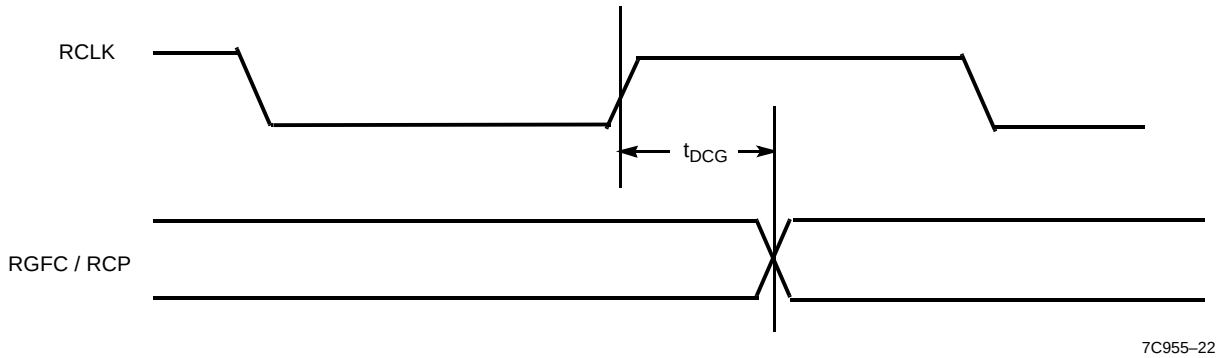
7C955–20

Switching Waveforms (continued)

Utopia Interface (Receive Side) Timing [TSEN=1]

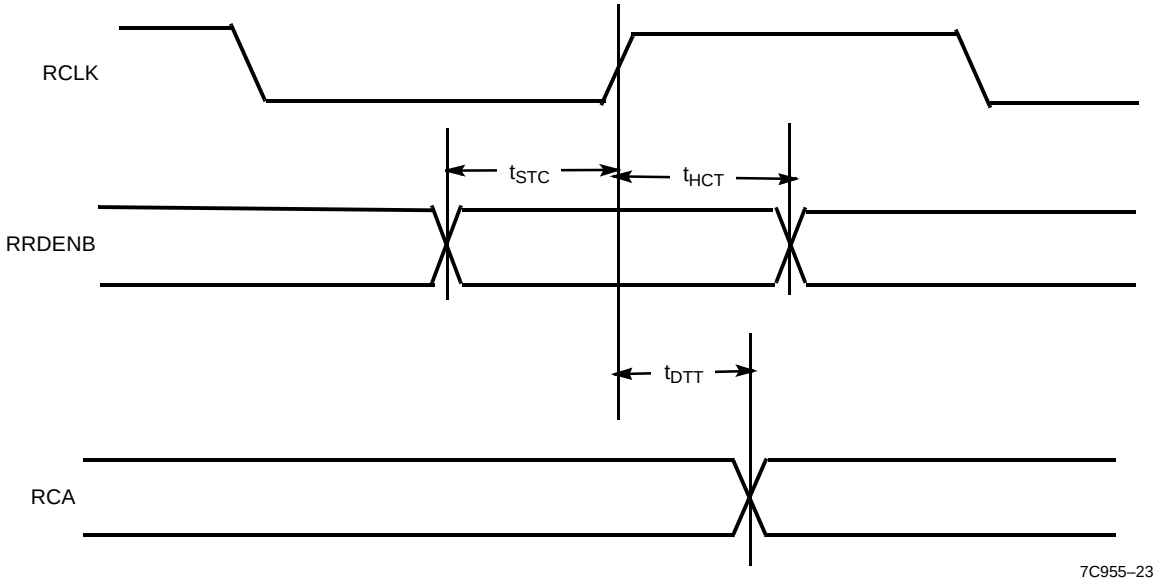


GFC Interface (Receive Side) Timing

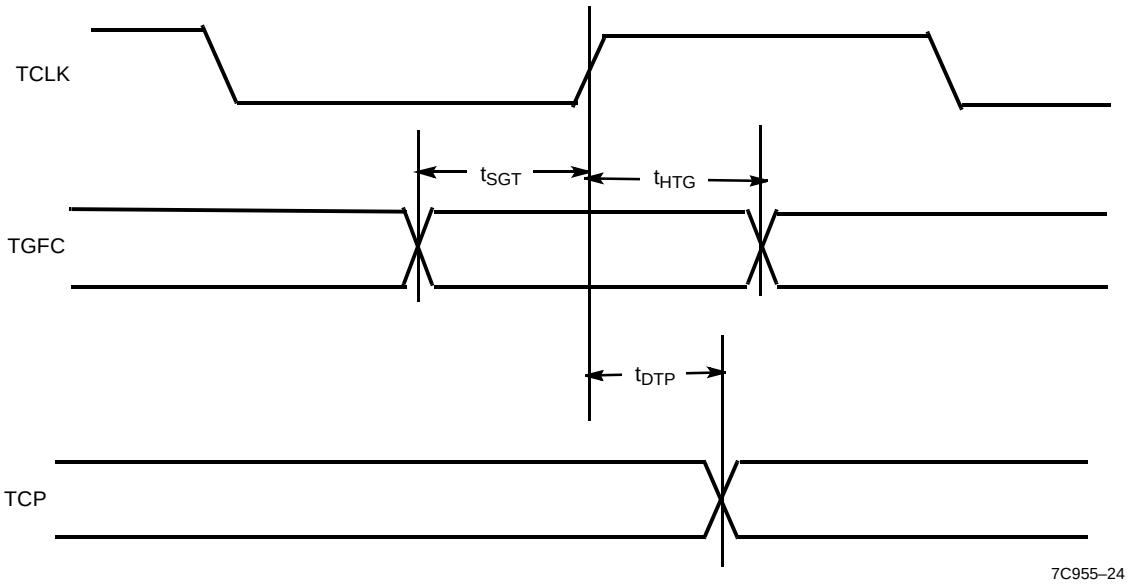


Switching Waveforms (continued)

Utopia Interface (Transmit Side) Timing



GFC Interface (TransmitSide)Timing



Functional Timing Diagram

Utopia Interface (Transmit Side) Functional Timing

Figure 8 shows, in a nutshell, all the functional timing requirements of the Transmit Side Utopia Interface. The Transmit Side Utopia Interface consists of TDAT[7:0], TXPRTY, TSOC, TWRENB, TCA, and TFCLK.

TDAT[7:0]

ATM cells are expected to be clocked into the Utopia FIFO interface through TDAT[7:0] with the 1st header byte first followed by the remaining 52 bytes of headers and payload. The fifth header byte (HEC) is required but is being ignored and replaced by the HCS octet generated by the Transmit ATM Cell Processor.

TXPRTY

The TXPTYP (Reg–63, bit 7) and TXPRTYE (Reg–63H, bit 6) can be set to make the Transmit Side Utopia Interface accept odd, even, or no parity TXPRTY inputs.

TSOC

A HIGH TSOC input is expected along with the first header byte of an ATM cell. If TSOC is absent, the Transmit ATM Cell Processor will automatically generate a TSOC based on previous TSOC positions, no interrupt will be sent. However, if TSOC is misplaced, the previously stored incomplete ATM cell will be discarded and the transmit FIFO pointer will be set back to the beginning of the same cell. A misplaced event will cause TSOCI (Reg–60H, bit 6) to go HIGH, and causes an interrupt also if FIFOE (Reg–60H, bit 7) is enabled.

TWRENB

This transmit FIFO write enable bit (TWRENB) should be pulled LOW whenever there is an ATM byte to send. It can be deactivated at any time to pause the writing process—not necessarily at cell boundaries.

TCA

The transmit cell available (TCA) is affected by TCAINV (Reg–01H, bit 3) and TCALEVEL0 (Reg–63H, bit 94). TCAINV determines the active polarity of the TCA signal, and TCALEVEL0 controls the meaning of TCA going active. If TCALEVEL0 = 0, TCA will be deasserted when the transmit FIFO is 4 writes from full. If TCALEVEL0 = 1, TCA will be deasserted when the FIFO is full and can accept no more writes.

TFCLK

TFCLK has to be a clock of 33 MHz or less. Although it can be stopped if necessary, it is not recommended because some registers and pins synchronized by this clock will not be updated. If this clock is stopped, the line side interface will still be able to transmit the cells already stored into the FIFO. After that, idle cells will be transmitted.

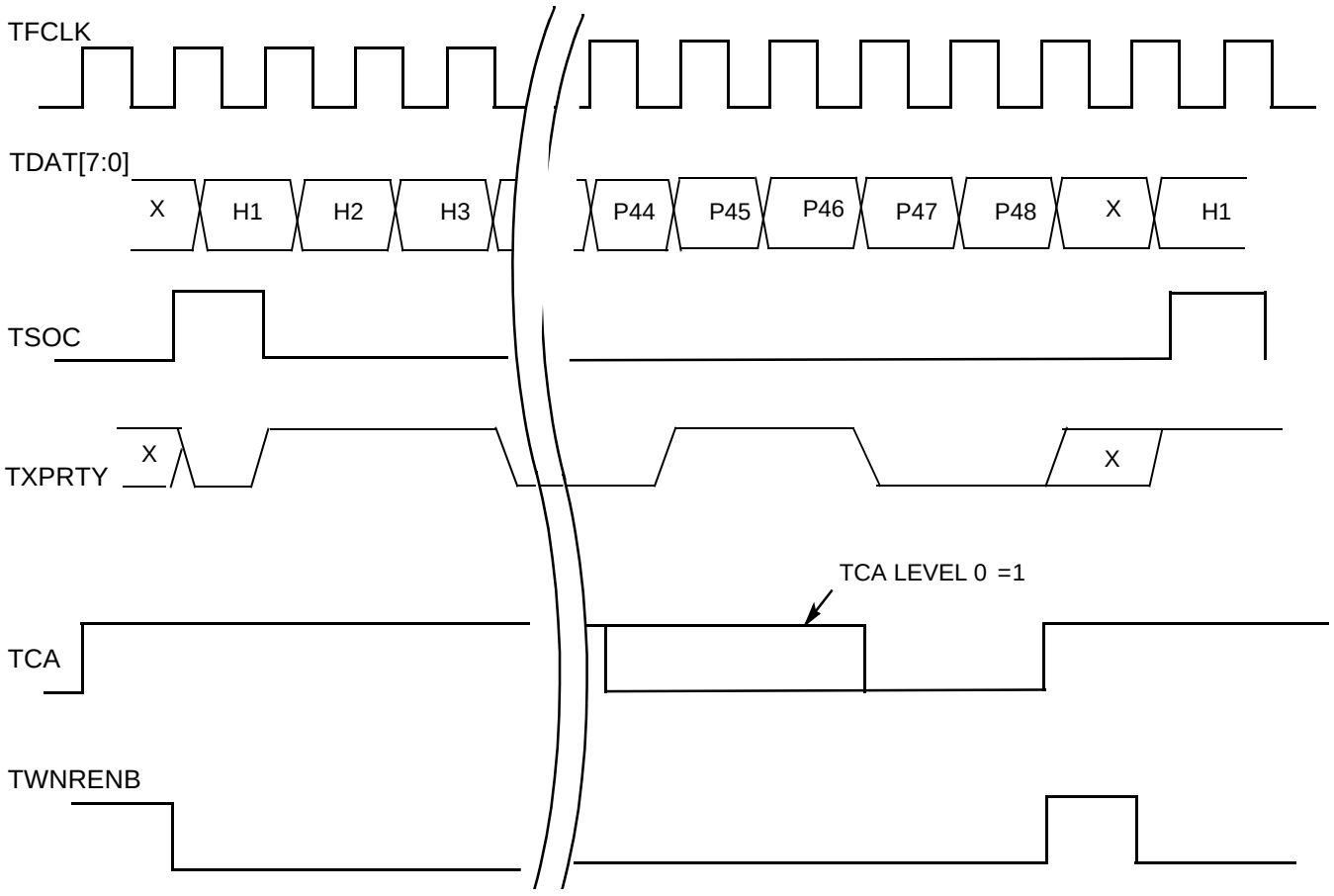


Figure 8. Transmit FIFO

Functional Timing Diagram (continued)

Utopia Interface (Receive Side) Functional Timing

Figure 9 shows, in a nutshell, all the functional timing requirements of the Receive Side Utopia Interface. The Receive Side Utopia Interface consists of TSEN, RDAT[7:0], RXPRTY, RSOC, RRDENB, RCA, and RFCLK.

TSEN

This three-state enable pin can be used to implement shared Utopia bus architecture for Multi-PHY operation. If TSEN is tied HIGH, RDAT[7:0], RXPRTY, and RSOC will be three-stated if RRDENB is HIGH. If TSEN is pulled LOW, RDAT[7:0], RXPRTY, and RSOC will always assume a logic 1 or logic 0. TSEN has an integrated pull down resistor.

RDAT[7:0]

ATM cells are clocked out of the Utopia FIFO interface through RDAT[7:0] with the 1st header byte first followed by the remaining 52 bytes of headers and payload. The cell stream can be stopped at anytime by pulling RRDENB HIGH.

RXPRTY

The RXPTYP (Reg–50, bit 6) can be set to make the receive side Utopia interface produce odd or even parity RXPRTY outputs.

RSOC

RSOC will go HIGH when RDAT[7:0] contains the first header byte of an ATM cell.

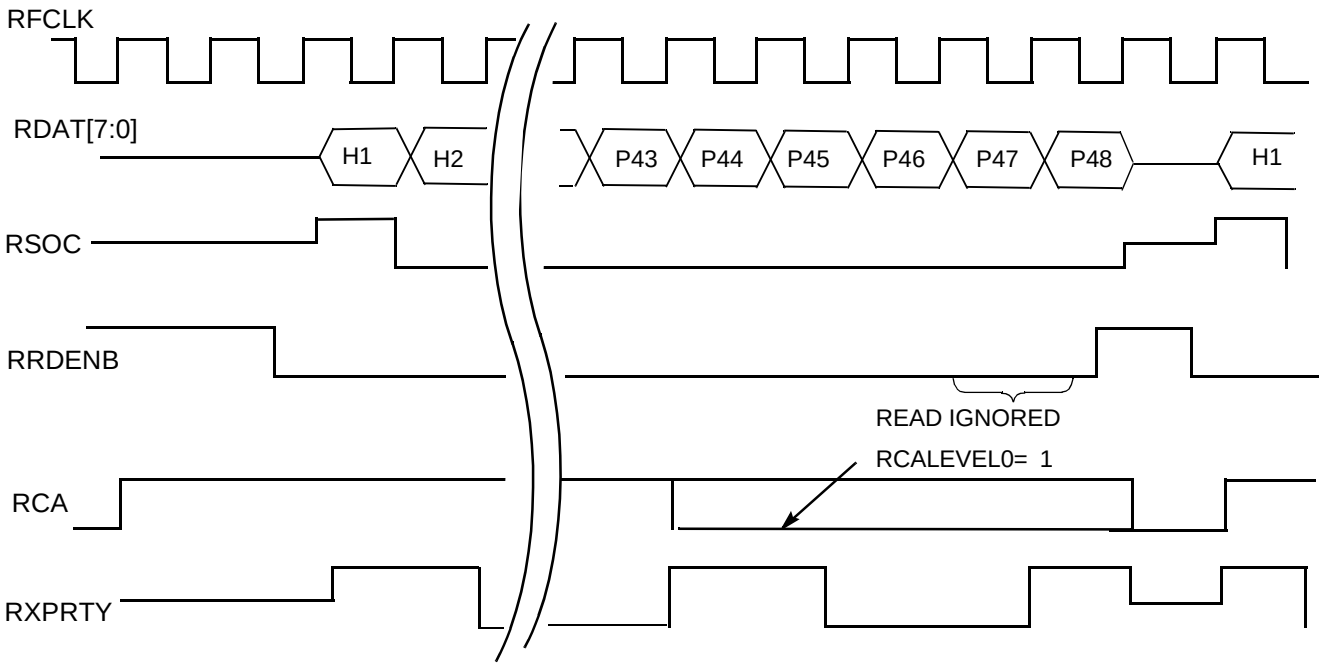


Figure 9. Receive FIFO

Functional Timing Diagram (continued)

GFC Interface (Transmit Side) Functional Timing

Figure 10 shows the functional timing for the TGFC input with respect to TCLK and TCP.

TCP

Transmit Cell Pulse toggles HIGH for one clock cycle 6 TCLK periods before the first octet of the next ATM cell is read from the transmit FIFO.

TGFC

If enabled by TGFCE (Reg-67, bit 4–7), a stable TGFC[3] is expected on the next rising edge of the TCLK after TCP goes HIGH (see *Figure 10*). All enabled TGFC bits will replace the corresponding GFC bit of the next transmitted assigned ATM cell. Unassigned/ Idle cells will maintain its default content and will not be affected by the TGFC input.

GFC Interface (Receive Side) Functional Timing

Figure 11 shows the functional timing for the RGFC input with respect to RCLK and RCP.

RCP

Receive Cell Pulse toggles HIGH whenever the most significant GFC bit (GFC[3]) of an assigned ATM cell header is presented on the RGFC pin. GFC[3] can be present for as long as 1 to 14 RCLK cycles on the RGFC pin, and so RCP can also be HIGH for anywhere between 1 to 14 RCLK cycles.

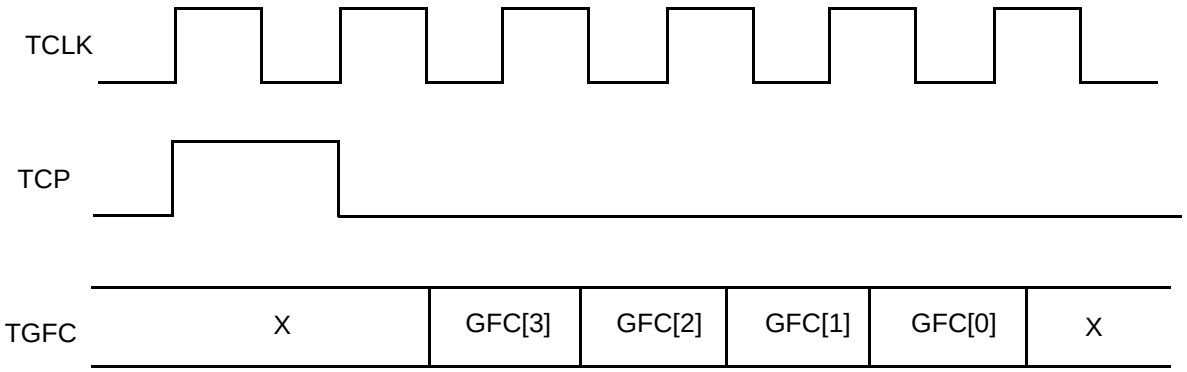


Figure 10. Transmit GFC Serial Link

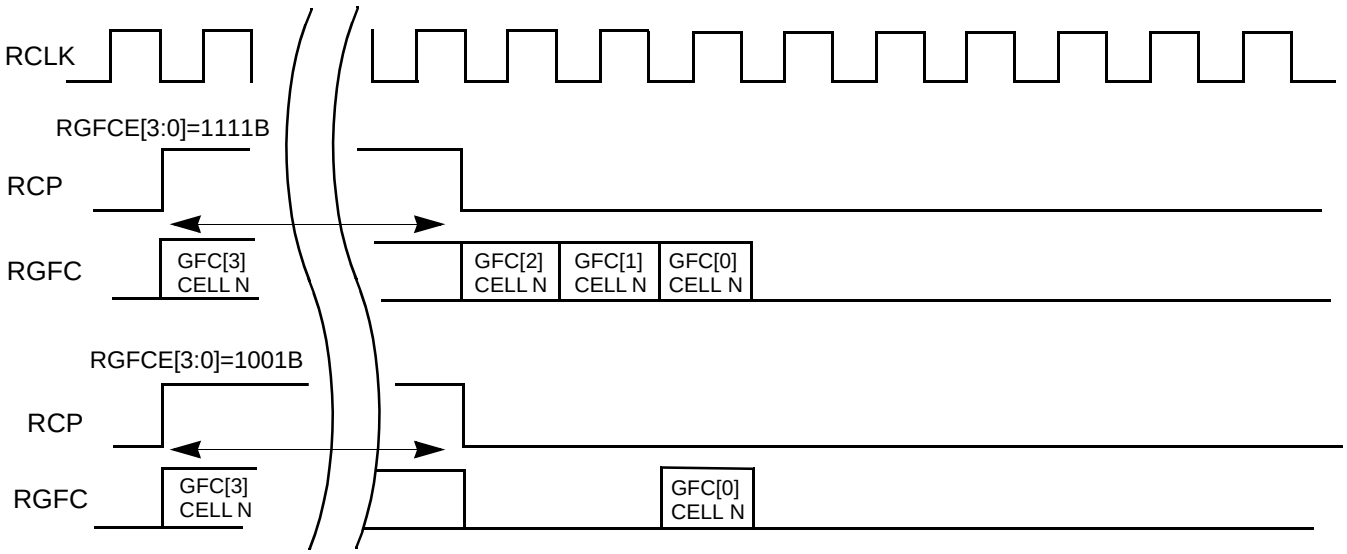


Figure 11. Receive GFC Serial Link

Functional Timing Diagram (continued)

Timing Modes

Figure 12, 13, and 14 shows how to connect the clock reference for different applications.

In the presence of a 155.52 MHz/51.84 MHz primary reference source (PRS). The configuration described in *Figure 12* should be used. TBYP is HIGH and RBYP is LOW. The primary reference clock source provides the accurate bit synchronization needed for the transmit data stream.

If the application is a LAN termination equipment, the configuration described in *Figure 13* should be used. LOOPT (Reg–5H, bit 0) is HIGH to enable loop timing mode. In loop timing mode, The clock recovered from the received data stream is being used to synchronize the transmit datastream. If that clock is lost, RRCLK x 8 will be used as the clock reference. The clocking architecture of the CY7C955 is shown in *Figure 14*.

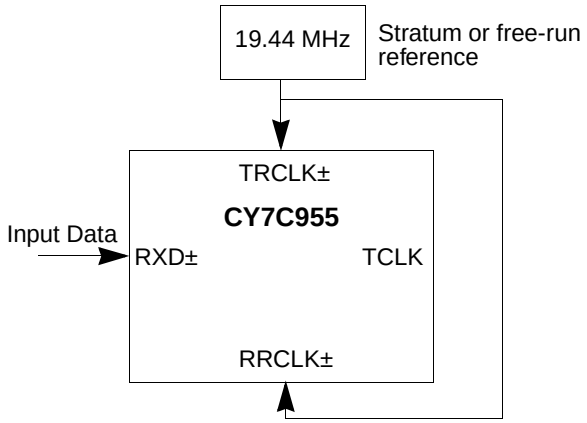


Figure 12. Clock Synthesis

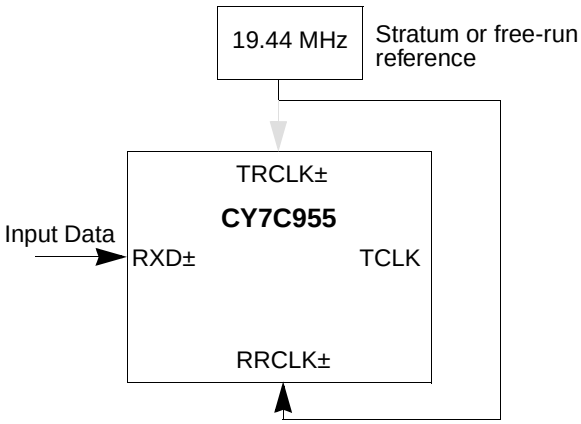


Figure 13. Loop Timing

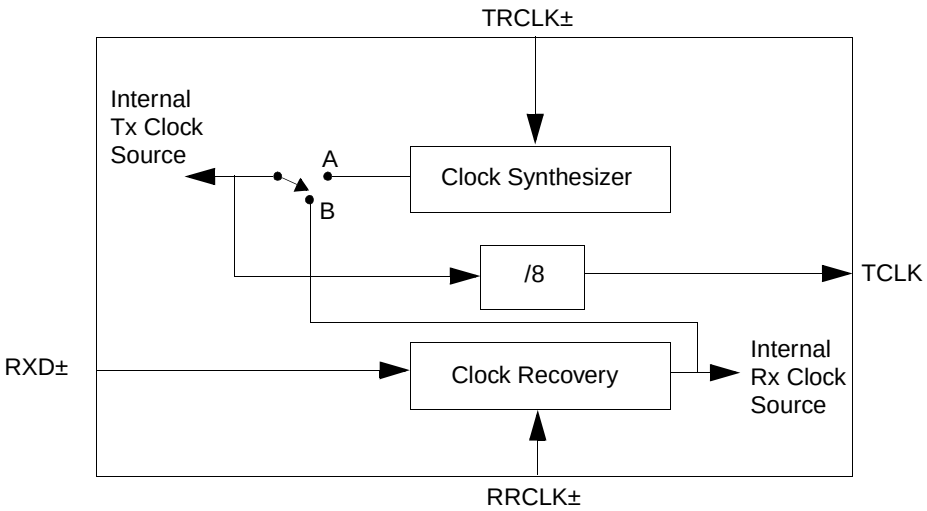


Figure 14. Conceptual Clocking Structure

Interface Termination and Biasing Schemes

PECL Input Termination and Biasing Recommendations

Figures 15–19 show how to connect different output types to the CY7C955 PECL inputs. Differential termination and biasing (*Figure 15*) is required for RXD, and is highly recommended for RRCLK, and TRCLK. Nevertheless it is also possible for the input to accept single-ended signals. If the positive end of a PECL input pair is tied to GND (with or without a pull-down resistor), the negative input will become a single-ended input. This input is self-biased to its threshold at $V_{CC}/2$. Notice that because the negative input is used, the signal entering the chip through the input are inverted.

Figure 15 shows a differential PECL connection. Whenever possible, this differential PECL connection scheme should be used. Differential signals are less susceptible to common-mode noise.

Figure 16 shows another possible type of a differential PECL connection. Although this connection is allowed, the method suggested in *Figure 15* will give better switching characteristics.

Figure 17 shows a CMOS connection; no termination is needed if the trace is kept short. If the trace is long, follow common transmission line termination practices.

Figure 18 shows a TTL connection. The 0.01µF AC-coupling capacitor allows the CY7C955 inputs to self-bias itself to $V_{CC}/2$. This connection scheme is not suitable for the ALOS input because the signal is close to static.

Figure 19 shows how to connect a single-ended PECL connection to the ALOS– input. ALOS is almost a static signal, so the connection must be DC-coupled. A 330Ω resistor to GND is needed, as a current sink is needed for the PECL output to operate correctly.

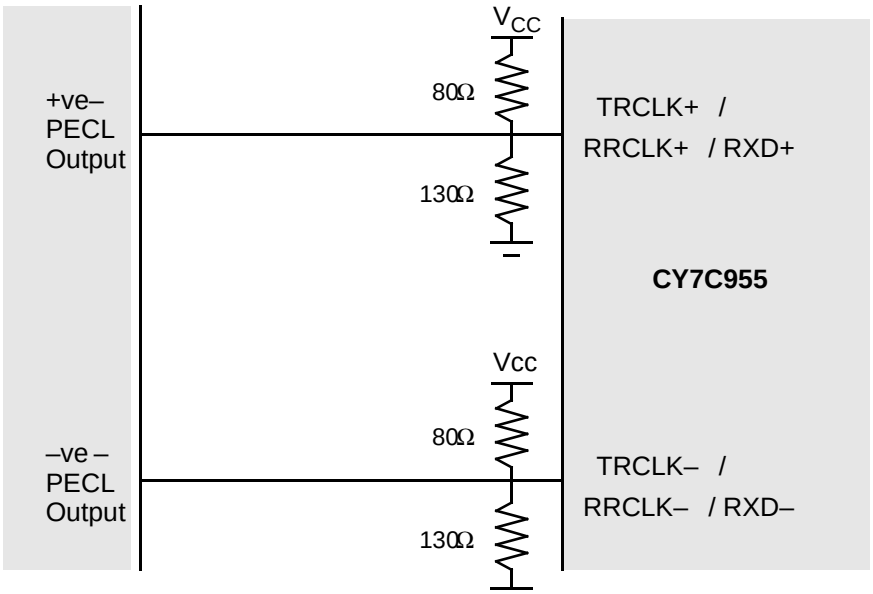


Figure 15. Differential PECL Termination (High Performance)

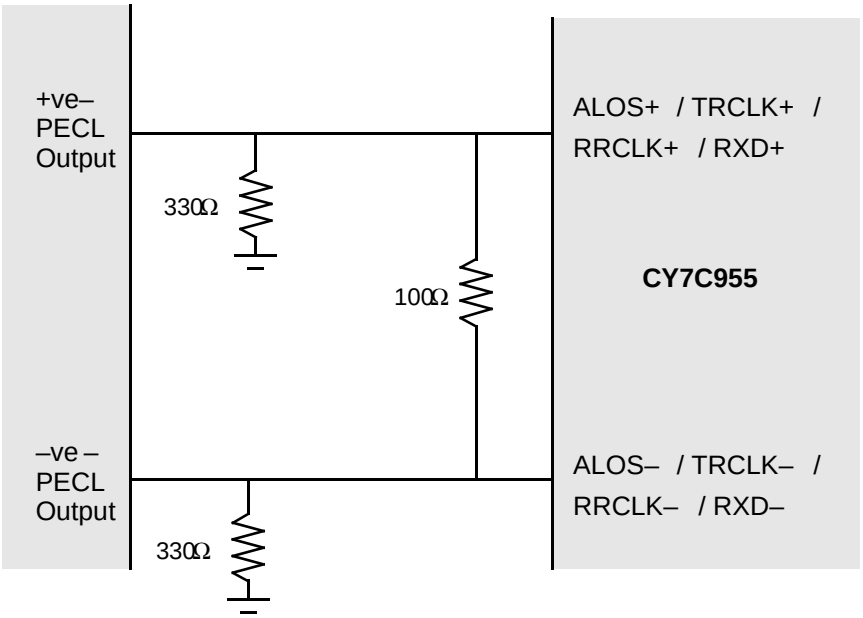


Figure 16. Differential PECL Termination (Low Power)

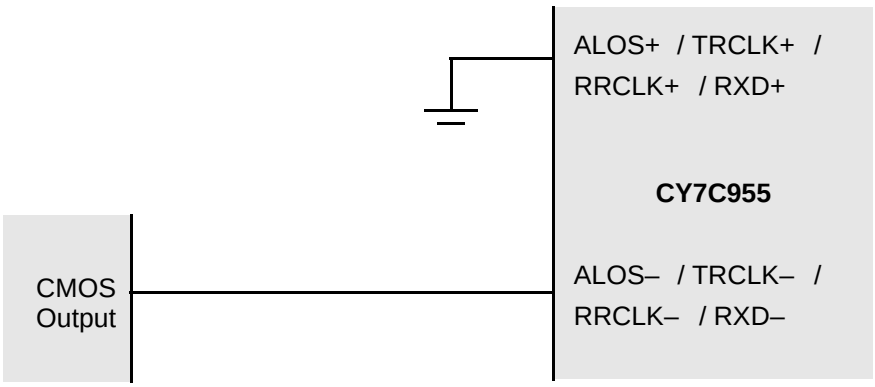


Figure 17. CMOS Connection

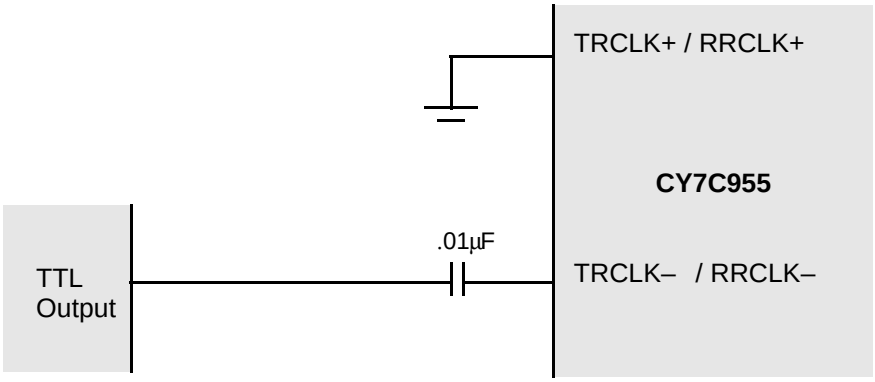


Figure 18. TTL Connection

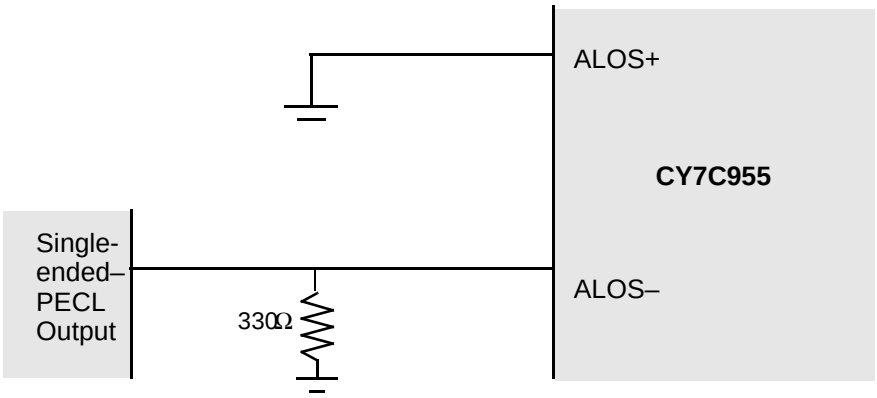


Figure 19. Single-ended PECL Connection for ALOS

Filter Pin Configuration

The CY7C955 Phase-locked Loop is designed to meet the Bellcore specifications on jitter generation, jitter transfer, and jitter tolerance. The highly integrated charge pump design drastically reduces the complexity of external filter components. Only a single 0.47-µF non-polar capacitor is needed to provide the damping factor needed to meet the jitter ceiling defined in GR-253. *Figure 14* describes how to connect the capacitor across the LF– and LFO pins of the CY7C955. The LF+ pin is to be left unconnected.

The 1.0-µF capacitor should have the following characteristics:	
Breakdown Voltage:	16V or higher
Tolerance:	±10% or better
Dielectric:	X7R or better
Polarity:	Non-polar or Bipolar
Size:	1206 or 1210 (0805 is not available commercially yet)
Example Part Number:	
Size: 1206	Part Number: 1206YC474JAT1A
Breakdown: 16V	AVX Corporation
Capacitance: 0.47µF	Tel: 360 699 8746

The 1.0-μF capacitor should have the following characteristics:	
Breakdown Voltage:	16V or higher
Tolerance:	±10% or better
Dielectric:	X7R or better
Polarity:	Non-polar or Bipolar
Size:	1206 or 1210 (0805 is not available commercially yet)
Dielectric: X7R	
Tolerance: ± 5%	
Size: 1206	Part Number: EMK316BJ474K
Breakdown: 16V	Anderson Electronics Component Distribution
Capacitance: 0.47μF	Tel: 408 577 1323
Dielectric: X7R	
Tolerance: ±10%	

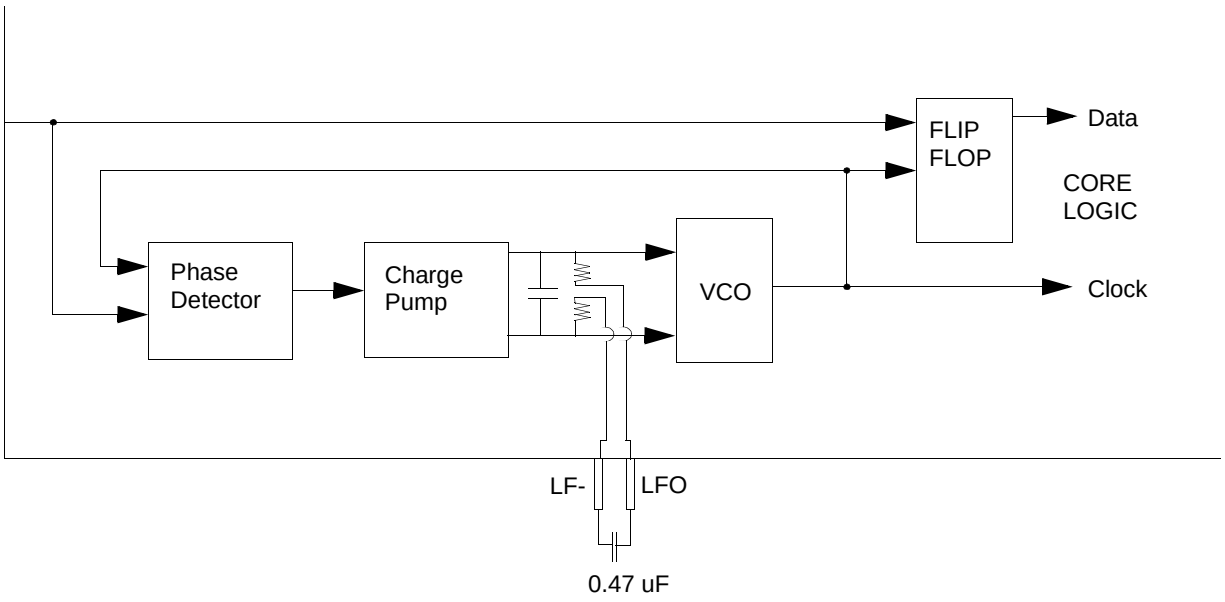


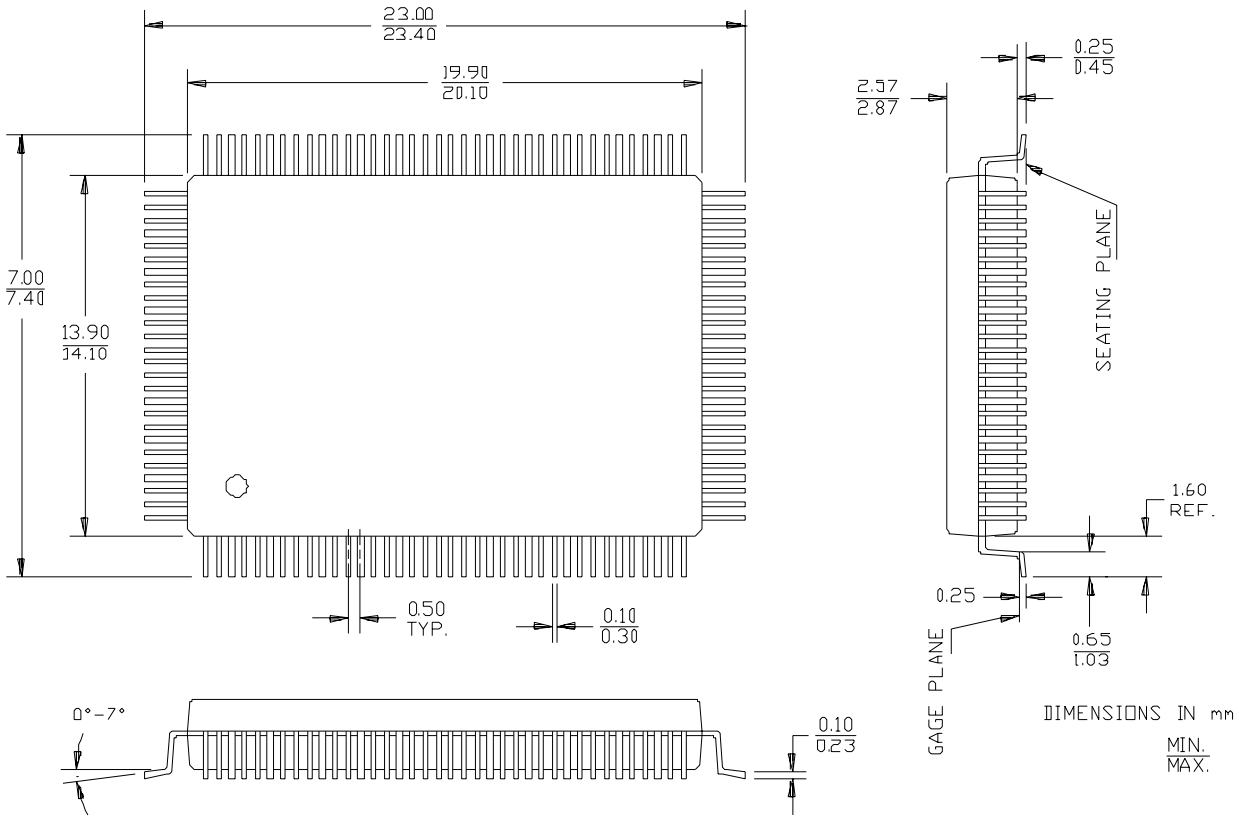
Figure 20. Phase-Locked Loop Capacitor Placement

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C955-NC	N128	128-Lead Plastic Quad Flat Package	Commercial
CY7C955-NI	N128	128-Lead Plastic Quad Flat Package	Industrial

Package Diagram

128-Lead Plastic Quad Flatpack



ADDENDUM - Design Considerations for the CY7C955

This memo outlines current design considerations for the CY7C955 - ATM PHY in reference to the ATM Forum UTOPIA Level 1 specification.

Receive FIFO Reset

The Receive four-cell FIFO is reset by programming register 0x50(RACP)[0] to a logic '1'.

Under this condition the CY7C955 RCA output is not deasserted immediately and the RDATA[7:0] output is not 0x00. The CY7C955 RCA output is held asserted until the end of the current transmission of the cell on the RxUTOPIA bus. The RDATA is hold immediately after the RxFIFO Reset is recognized, while the RCA output is still asserted (indicating a valid cell).

54-Byte Cell on RxUTOPIA Bus

Received ATM cells in the RXFIFO can be read out from the RxUTOPIA bus at various throughput. The throughput can be throttled by two ways; one way is by changing the RFCLK frequency; another way is using the RRDENB input and a fixed RFCLK (for more information on the Rx UTOPIA bus operation, refer to the pin description, "Receive UTOPIA Interface" section of the data sheet and the UTOPIA spec Level 1). When the throughput writing into the RxFIFO is greater than the throughput reading out, then, intermittently, the CY7C955 outputs a cell with 54bytes

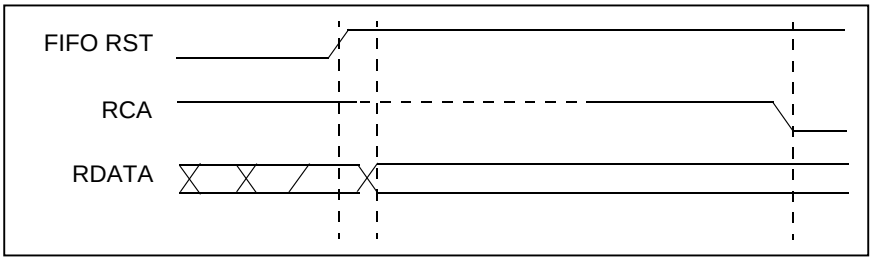


Figure 21. CY7C955 Receive FIFO Reset Behavior

Document Title: CY7C955 AX™ ATM-SONET/SDH Transceiver Document Number: 38-02006				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	105844	3/23/01	SZV	Change from Spec number 38-00417 to 38-02006