Using the CY7B923 as an ECL Clock Source

Abstract

This application note details the use of an inexpensive data communications transmitter device as a high-precision, flexible, and programmable Emitter-Coupled-Logic (ECL) or Positive-Emitter-Coupled Logic (PECL) clock source. Issues concerning clock characteristics, stability, distribution, and design techniques are discussed in detail. Information is provided to allow the user to configure the device for a variety of applications.

The Ideal Clock Circuit

An ideal clock source provides several attributes beneficial to a design or product.

- Operates over a broad range of frequencies
- Stable cycle-to-cycle period over time and temperature
- Stable duty cycle over time and temperature
- Fast rise and fall time into various loads
- Single-ended or differential drive
- Minimum output-to-output skew
- Relatively low power consumption
- Low cost per performance ratio
- Operable in commercial, industrial, and military environments

The Cypress CY7B923 HOTLink™ transmitter, although not specifically designed as an ECL clock source, provides all of these characteristics (when coupled to a standard inexpensive TTL oscillator).

HOTLink Transmitter Features and Specifications

The HOTLink chip set is comprised of a pair of high-speed point-to-point communications building blocks that operate over high-speed serial data links (fiber-optic, coaxial cable, and twisted/parallel pair) at 150 to 400 Mbits/second. The HOTLink pair consists of the CY7B923 Transmitter and the CY7B933 Receiver. The transmitter features a set of three positive 100K (referenced to +5) ECL differential output buffers, a data input register, an encoder to encode 8-bit data into 10-bit characters, a built-in self-test (BIST) pattern generator, a serializer to convert parallel data to serial data, and a clock generator to produce a bit-rate clock from the incoming character-rate clock input. These features of the CY7B923, with the exception of the encoder and built-in self-test circuits, make it ideal for use as a clock generator device.

CY7B923 Block Diagram Description

The HOTLink Transmitter is designed to transform information from a character-rate or byte-rate parallel format into a high-speed serial format. A block diagram of the CY7B923 HOTLink Transmitter is shown in *Figure 1* and a description of each module follows.

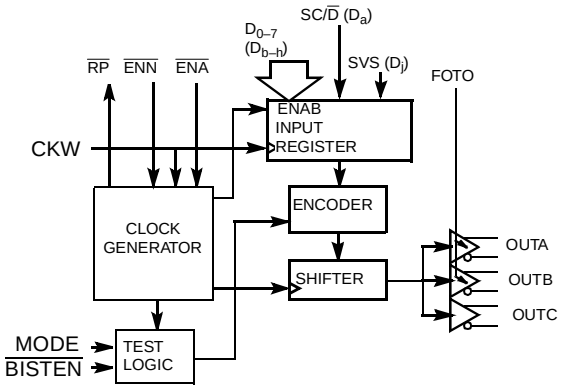


Figure 1. CY7B923 HOTLink Transmitter Logic Block Diagram

Clock Generator

The clock generator contains a phase-locked loop (PLL) that multiplies a character-rate reference clock (CKW) by a factor of ten to produce the serial bit-rate. Data is clocked into the input register on the rising edge of CKW. The duty cycle of CKW does not affect the outgoing serial-bit stream since the PLL is capable of maintaining proper phase and duty cycle on its own. The clock generator also produces a signal called $\overline{RP}$ (Read Pulse) that is used to read new data from a FIFO in a data communications application. $\overline{RP}$ is not used when the HOTLink Transmitter is used as a clock source.

Input Register

The input register captures the data present at the Da–j inputs at the rising edge of the CKW clock. This parallel data is then loaded directly into the shifter for serialization if the encoder is disabled.

Encoder

The encoder is used to encoded the incoming data from the input register into an 8B/10B format for ANSI T11 (Fibre Channel), IBM® ESCON™, and other applications. In unencoded mode, the data passes directly from the input register into the shifter. This application of the HOTLink Transmitter as an ECL clock source uses the CY7B923 in unencoded mode.

Shifter

The shifter accepts the 10-bit character which was loaded into the input register. With the encoder disabled, the data is converted from parallel to serial with the data present on input pin Da (pin 19) shifted out first.

Output

The CY7B923 has three PECL (100K referenced to +5V) outputs. These outputs provide differential (true and complement) capability, offer an enable pin (the FOTO pin for output

pairs A and B) and the ability to directly drive transmission lines impedances as low as 25Ω.

Test Logic

The test logic is not used in the ECL clock source application. It contains the logic to generate the built-in self-test pattern that is used to test the integrity of a data communications interface and link.

Fulfilling the Requirements

Frequency Range

Since the HOTLink transmitter was designed to communicate or send data at a rate of 150–400 Mbits/second, it is ideally suited for the application of generating precise transitions or clock edges over a broad range of frequencies. As the transmitter operates, 10-bit characters are loaded into the CY7B923 serializer at the character clock-rate. The internal PLL takes the character-rate clock and multiplies it by ten to generate the rate at which the individual bit transitions are shifted out of the serializer. The encoder function is disabled when the transmitter is used as a clock source to provide maximum control of the data patterns being shifted out. The two primary factors that affect clock output frequency are character-rate clock frequency and the number of bit transitions within the 10-bit character. This relationship is shown in Equation 1.

$$clock\ out = (character\text{-}rate\ clock)((\#\ of\ transitions)/2) \quad \text{Eq. 1}$$

Where:

clock out = clock frequency present at the outputs of the transmitter

character-rate clock = rate at which the 10-bit characters are loaded into the serializer

# of transitions = the number of transitions between one logic level and another

Assume a 20-MHz character rate clock and a data pattern of 0101010101.

clock out = (20 MHz) (10 transitions) / 2 = 100 MHz

The duty cycle, or relationship of clock HIGH time to clock LOW time, can also be affected by the data pattern loaded into the serializer. The duty cycle is controlled by the ratio of consecutive ones to consecutive zeros. If there are six consecutive ones and four consecutive zeros in the data pattern, the duty cycle would be 60%. If the pattern was 0001100011 the duty cycle would be 40% but the number of bit transitions would double and so would the clock out frequency.

Table 1 shows examples of clock out frequencies and duty cycles that can be obtained using the data patterns and source frequencies given.

Test Circuit

A typical test circuit is shown in *Figure 2*, detailing the HOTLink Transmitter in a PECL clock generator application. The circuit uses the CY7B923 with a 10-position DIP switch to select the desired data pattern (e.g., *Table 1* patterns). The $\overline{\text{BISTEN}}$, and MODE pins are pulled to a logic HIGH while $\overline{\text{ENA}}$ or $\overline{\text{ENN}}$ are tied to a logic LOW. This configures the device to operate with built-in self-test and 8B/10B Encoding disabled, and data at Da to Dj.

The FOTO input is used as a clock output enable for output pairs OUTA and OUTB. When FOTO is LOW, transmit data will continuously be driven on output pairs A and B. When FOTO is HIGH, the output pairs A and B will remain at a logic zero state. Output pair OUTC is always enabled and will reflect the current state of the transmitter shifter output.

The $\overline{\text{RP}}$ or Read Pulse output is typically used to indicate new data can be read from a FIFO or other storage device into the transmitter. It is not used in the clock generator application.

In the test circuit shown, the character-rate clock could be any stable TTL clock source operating between 15 MHz and 40 MHz. As described previously, the resultant output clock frequency is dependent on character clock frequency (CKW) and the number of 0-to-1 or 1-to-0 bit-transitions present in the 10-bit character loaded into the input register of the HOTLink transmitter.

Table 1.

Data Pattern	Character Rate	Duty Cycle	Bit Transitions	Clock Frequency
0000011111	15 MHz	50%	2	15 MHz (Min. Rate)
0000001111	25 MHz	40%	2	25 MHz
0011100111	16 MHz	60%	4	30 MHz
0000011111	40 MHz	50%	2	40 MHz
0000100001	25 MHz	20%	4	50 MHz
0001100011	40 MHz	40%	4	80 MHz
0101010101	16 MHz	50%	10	75 MHz
0101010101	25 MHz	50%	10	125 MHz
0101010101	40 MHz	50%	10	200 MHz (Max. Rate)

NOTE: The minimum duty cycle is 10% and the maximum duty cycle is 90%. The minimum clock out is 15 MHz and the maximum clock out is 200 MHz.

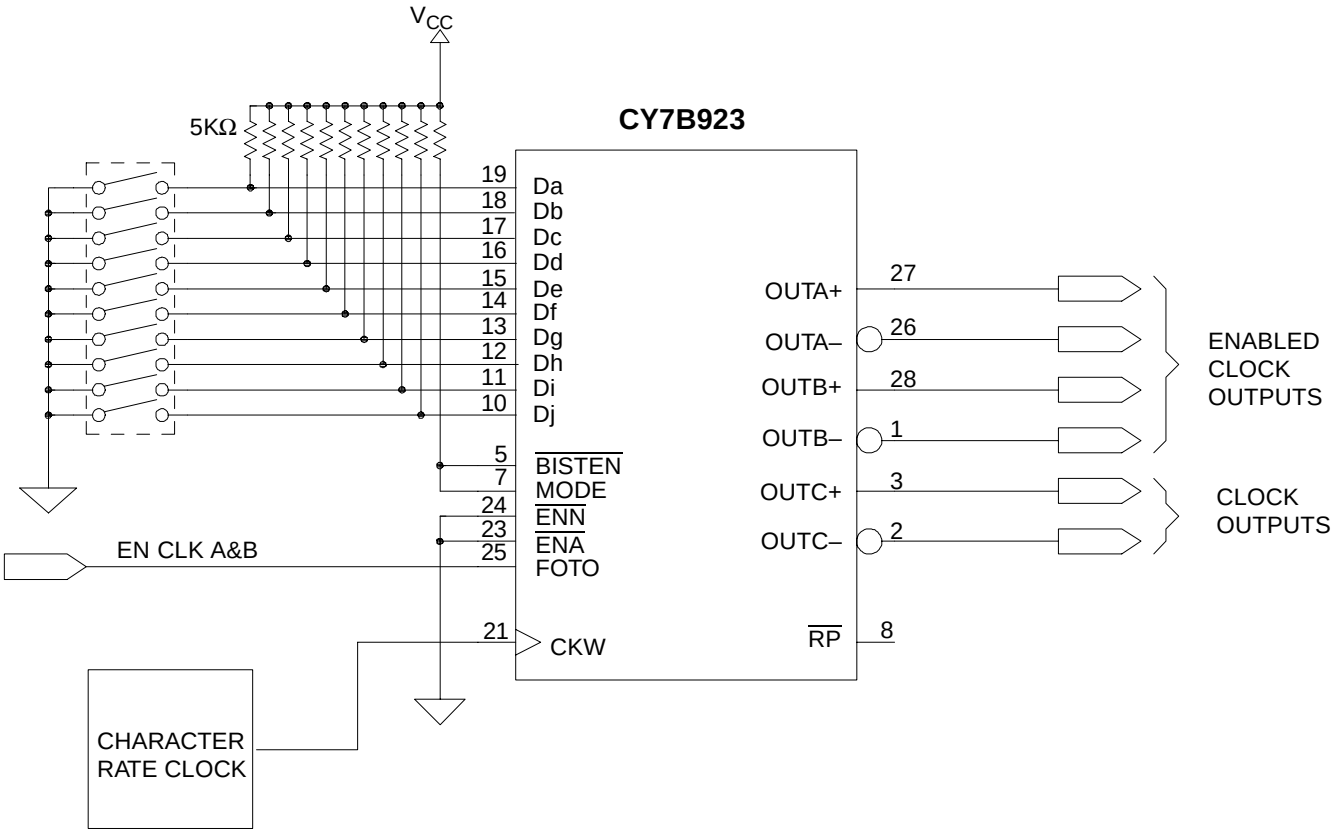


Figure 2. CY7B923 Clock Generator Test Circuit

Clock Issues

Since the CY7B923 was originally intended for very high-speed communications, its inherent stability allows it to meet the rigid requirements of the standards imposed by industry. These same principles relating to clock stability also apply when the device is used as a PECL/ECL clock source. In general, the most critical factors relating to clock performance are jitter, duty cycle stability, rise and fall times, and output skew.

Jitter

Jitter is typically defined as the variation of one clock edge with respect to another. One source of jitter can be caused by noise-induced variations in the PLL, often known as random jitter. An additional form of jitter can result from the data patterns fed to the transmitter. This data dependent jitter is not relevant in the case of the clock generator because the pattern is constant and repeating. Jitter can also have an effect on the duty cycle of a clock waveform, generally referred to as duty cycle distortion. Refer to the CY7B923 data sheet for more specifications on jitter.

Duty Cycle Stability

For the clock generator application, the duty cycle, or relationship of a logic HIGH time period to a logic LOW time period, is dependent on three factors: random jitter, transmit data pattern, and rise and fall times. Random jitter has an affect on duty cycle based on the fact that it varies the placement of one clock edge with respect to another. Another factor relating to duty cycle stems from the variation of the data pattern presented to the inputs of the transmitter. This is considered a very coarse adjustment as it can only be varied by a minimum of a single serial bit-time. The last factor is rise and fall time, and is largely dependent on the load the outputs are driving.

Rise and Fall Time

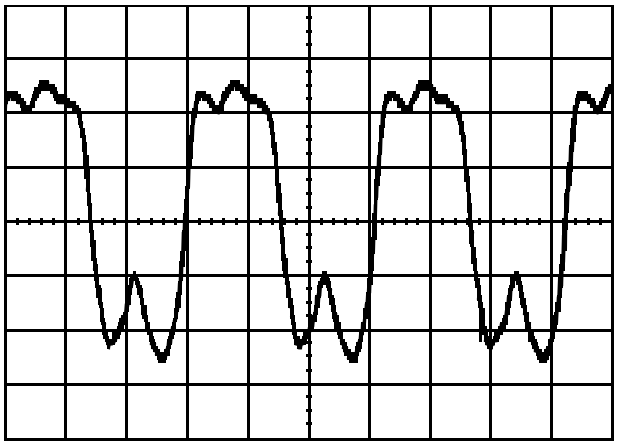
Rise and fall times are defined as the period of time required for a signal to transition from a logic LOW to a logic HIGH or a logic HIGH to a logic LOW. The rise time of an ECL output is mainly determined by internal parameters such as the internal driver impedance and the parasitic capacitance of the output and is generally fixed. The fall time, however, is generally based on the biasing of the output, the load capacitance, and the termination of the clock circuit. If each of the outputs are properly biased and treated as a transmission line, the driver can provide matched rise and fall times. A proper biasing technique is to tie the PECL output to V_{CC} – 2.0V through a 50Ω resistor. Since ECL outputs switch at such high speeds, typically in the 1-ns range, most ECL circuit board traces greater than 2.5 cm (1 inch) in length should be treated as transmission lines and require termination (Reference 3). When a circuit board trace acts as a transmission line and is unterminated, it reflects a portion of the signal energy from the unterminated end of the transmission line back to the source. If this reflection is significant, it can cause erroneous triggering of digital logic circuits. The CY7B923 data sheet indicates a maximum rise time and fall time of 1.2 ns mea-

sured at the 80% and 20% voltage points when driving an ECL load of 5 pF and 50Ω terminated to V_{CC} – 2.0 Volts. This is specified as a guaranteed maximum. Typical rise and fall times are less than the maximum.

Termination

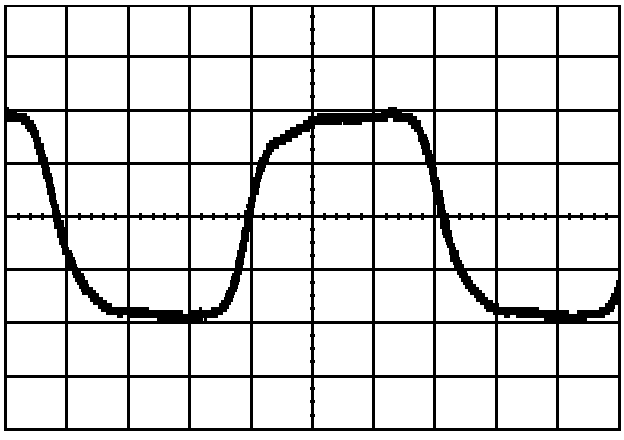
The two types of termination techniques generally used to control transmission line effects are series and parallel termination. A series (source) termination is designed to match the impedance of the source driver to the characteristic impedance of the line being driven. This termination approach is not recommended for the HOTLink Transmitter. A parallel termination, on the other hand, both biases and matches the characteristic impedance of the transmission line. This termination network, also called a Thévenin Termination, consists of a pull-up resistor to the positive supply and a pull-down resistor to the negative supply.

An example of an improperly terminated ECL waveform is shown in *Figure 3*. Notice the excessive ringing on the logic LOW level. *Figure 4* shows what a properly terminated ECL signal should look like. Notice the symmetrical rise and fall times and the absence of any ringing on the waveform.



Ch. 1 = 200.0 mvolts/div Offset = –1.332 volts
Timebase = 2.00 nsec/div Delay = 0.00000 sec

Figure 3. Improperly Terminated Waveform



Ch. 2 = 200.0 mvolts/div Offset = –1.320 volts
Timebase = 1.00 nsec/div Fall Time = 880 psec
Rise Time = 830 psec

Figure 4. Properly Terminated ECL Waveform

Refer to the Cypress Semiconductor “HOTLink Design Considerations” application note for more information on transmission line termination techniques.

Clock Skew

Clock skew is introduced into a digital system in two ways. The first is called output skew and is defined as the difference in time between clock edges being driven from the OUTA, OUTB, and OUTC transmitter output pairs. Output skew is caused internally by the clock driver circuit itself. It can result from the differences in output driver characteristics between output pairs or even in layout and placement differences of the physical driver structures on the die. The second source of clock skew is related to the printed circuit board layout and placement. Trace length, capacitive loading, termination components, printed circuit board characteristics, supply voltages, and many other factors affect these external delays. It is important that the designer understand the issues affecting clock skew because one must be able to accurately predict when clock edges will arrive at a load or destination for proper synchronization of a digital system.

Drive Capability

The HOTLink transmitter features three sets of differential PECL/ECL outputs. Each output of the differential drivers is capable of driving a 25Ω load (50Ω differential) with a maximum output current of 50 mA.

Power Supply Current

The HOTLink Transmitter has a maximum I_{CCT} specification of 85 mA for commercial and 95 mA for military temperature devices. Additionally, each enabled output pair contributes 35 mA to I_{CCT} when loaded to 50Ω. Unused outputs may be left open or tied to V_{CC} to minimize the power dissipated by the output circuit and reduce a source of unwanted noise. A 5-mA power savings can be obtained by disabling the output current source in this manner.

HOTLink Transmitter Printed Circuit Layout

Care must be taken when laying out a printed circuit board for the HOTLink Transmitter and when designing any clock circuit in general. Proper power supply filtering and bypassing, using the proper components, must be employed to ensure proper operation. Everything from the oscillator used to feed the CKW input to the type and placement of the bypass capacitors used is critical. Refer to the Cypress Semiconductor “HOTLink Design Considerations” application note for specific details on circuit layout and bypassing.

Device Packaging

Like virtually all Cypress devices, the CY7B923 HOTLink Transmitter is available in commercial (0 to 70 degrees C), industrial (–40 to +85 degrees C) and military (–55 to +125 degrees C) temperature ranges at V_{CC} ± 10%. The device comes packaged in a 28-pin PLCC, 28-pin LCC, or a 28-pin 300-mil-wide SOIC to suit a broad range of packaging requirements. The device is not available in Dual-In-Line (DIP) or through-hole packages due to the excessive lead-frame inductance and its effect on device performance.

Conclusion

The HOTLink Transmitter offers designers of pseudo ECL systems an alternative to the expensive, high-power clock sources currently available on the market. The combination of BiCMOS process technology and robust feature set makes the CY7B923 suitable for many PECL and ECL clock references where cost, power, flexibility, and performance are of prime concern.

References

1. *MECL System Design Handbook*, Blood Jr., William R., Fourth Edition, 1988
2. *Data Communications Data Book*, Cypress Semiconductor Corporation, 1996
3. HOTLink Design Considerations, Cypress Semiconductor Corporation Application Note
4. *HOTLink User's Guide*, Cypress Semiconductor Corporation, 1999