Converting to CY7C955 from S/UNI-LITE™

The CY7C955 is a pin-for-pin compatible part to the PMC Sierra S/UNI-LITE PM5346. The CY7C955 also provides improved performance and intergration. There are two major areas of improvements in the CY7C955: PECL compatible serial transmit interface, and reduction in external PLL components. This results in some difference in board components used for the serial receive side termination, serial transmit side termination, and external PLL filter components. This application note discusses how to convert a socket designed for the S/UNI-LITE to use the CY7C955.

Serial Receive Side Termination

The receive side signals RXD±, RRCLK±, TRCLK± and ALOS± are differential PECL signals which require proper termination in order for the CY7C955 to interpret the signals at the correct voltage level. The S/UNI-LITE serial side inputs are not true PECL. A 0.01-µF capacitor in series with each of its serial inputs is required for them to self bias to 2.5V. Unlike the S/UNI-LITE, the CY7C955 receive side inputs are PECL compatible inputs. Therefore the 0.01-µF capacitors are not needed. The space for the 0.01-µF capacitor must be replaced by a 0Ω resistor. Incoming PECL signals need to be terminated to a voltage of V_{CC} – 2V. To do so, connect an 80Ω pull-up resistor and a 130Ω pull-down resistor to each of the PECL inputs at the load. The differential signals are always complements of each other, therefore, a single 0.01-µF capacitor can be used to decouple the 80Ω and 130Ω resistors across the power supply terminals as shown in *Figure 1*.

Driving the PECL signals differentially is recommended for optimal symmetry of rising/falling edge rate and common mode noise immunity. For other driving schemes please refer to Interface Termination and Biasing Schemes section of the datasheet.

Serial Transmit Side Termination

The transmit side signals TXD±, TXC± and RXDO± are also PECL compatible differential outputs. Again, the S/UNI-LITE differential outputs are not PECL compatible but TTL outputs. Therefore they require a 0.01-µF capacitor in series with a 237Ω resistor to AC couple and potential divide the TTL outputs of the S/UNI-LITE to PECL level. Such TTL outputs are not suitable to drive low-impedance transmission lines. Since the CY7C955 transmit side outputs signals are PECL compatible, the two passive components, 0.01-µF capacitor and 237Ω resistor, are not needed. 0Ω resistors must be used in place of the 0.01-µF capacitor and 237Ω resistor. The PECL compatible outputs are suitable to drive low-impedance transmission lines, such as twisted pair or coaxial cable.

Typically, the transmit side outputs TXD± will be connected to the input of the optical modules. These differential PECL outputs must terminate to V_{CC} – 1.33V. The recommended terminating resistors are a 68Ω pull-up and a 187Ω pull-down. A 0.01-µF capacitor is required to decouple the termination resistors as described in the Serial Receive Side Termination section above. See *Figure 2*.

Phase Lock Loop (PLL) Filter

The S/UNI-LITE requires eight external components for its PLL filter, which includes three resistors, four capacitors and one transistor. The CY7C955 PLL filter only requires a single 0.47-µF non-polarized capacitor connected across the LF– and LFO pins. The LF+ pin is not used in the CY7C955 PLL filter, and it should be left unconnected as shown in *Figure 3*.

No Connect (NC) Pins

The S/UNI-LITE has five No Connect pins, pin 45–49. For the CY7C955, these NC pins must be connected to ground.

Considerations for open drain outputs

The INTB pin is an open drain output. This output requires an 1kΩ pull-up resistor to supply enough current for the output driver.

Conclusion

Minor changes are required to convert from the S/UNI-LITE to the CY7C955. The CY7C955 offers the advantage of PECL compatible interfaces, which saves four components per output pair, and two components per input pair. The highly integrated PLL also saves seven external components.

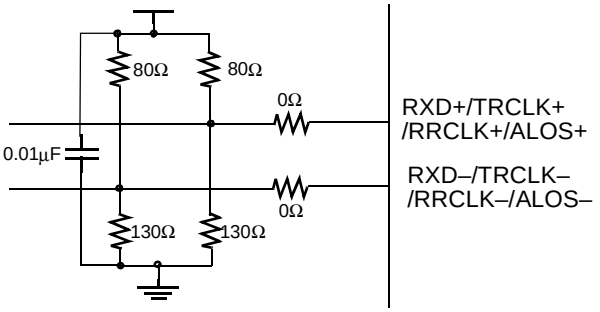

Figure 1. Receive Side Termination Network

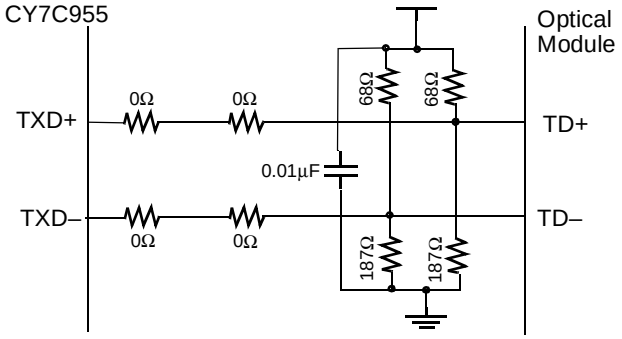

Figure 2. Transmit Side Termination Network

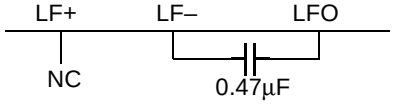

Figure 3. PLL Filter Component