Frequently Asked Questions About the CY7C9689

The following questions are frequently asked by customers who are evaluating the CY7C9689. These cursory answers serve as an introduction for each topic. Separate application notes are available or planned to cover most topics in more complete detail.

1. How are the CY7C9689 features similar to the Am7968/Am7969 TAXI™ chips?

The similarities of key features between the CY7C9689 and TAXIchip™ are summarized in *Table 1*. This table also indicates some of the CY7C9689 enhancements.

Table 1. CY7C9689 and Am7968/Am7969 TAXIchip Similarities and Enhanced Features

Feature	Am7968/Am7968	CY7C9689
Parallel I/O signal level	TTL	TTL
Parallel data character I/O widths	8, 9, or 10 bits	8 or 10 bits
Parallel command character I/O widths	4, 3, or 2 bits	4 or 2 bits
Input interface method	Asynchronous using STRB/ACK	Synchronous or asynchronous using independent clocks
Serial I/O type	Single differential PECL for transmit and receive	Dual TAXI-compatible differential PECL for transmit and receive
Serial data throughput	40–175 MBaud 32–140 Mbps	50–200 MBaud 40–160 Mbps
Supply voltage	5.0V ± 10%	5.0V ± 10%
Power dissipation	Approximately 3.4W	Typically under 1W
Packaging	Two 28-pin DIPs or PLCCs	Single 100-pin TQFP (14 mm x 14 mm)
Serial line encoding/decoding	NRZI 4B/5B or 5B/6B	NRZI 4B/5B or 5B/6B
Number of serial bits per input data or command character	10 bits per 8-bit character, 11 bits per 9-bit character, 12 bits per 10-bit character	10 bits per 8-bit character, 12 bits per 10-bit character
FIFO interface	External only	Optional internal and/or external

2. Which pin on the CY7C9689 is equivalent to which pin on the Am7968 TAXI Transmitter? Which pin on the CY7C9689 is equivalent to which pin on the Am7969 TAXI Receiver?

While the CY7C9689 is not a pin-for-pin TAXI replacement, it is a TAXI-compatible device. This means that the typical operational functions of TAXI devices are available in the CY7C9689, and that these devices can intercommunicate in mixed TAXI and CY7C9689 systems. Many of the CY7C9689 signals are equivalent (or very similar to) signals in the TAXI devices. These similarities are summarized in *Table 2* for the Am7968 Transmitter and in *Table 3* for the Am7969 Receiver.

3. How far can the CY7C9689 communicate over various media?

The CY7C9689 has no intrinsic distance limit. The two issues that determine the distances over which data can be sent using the CY7C9689 are: (1) the choice of interconnect media (plastic or glass fiber-optic cable, coaxial cable, twisted-pair cable, etc.), and (2) the jitter that accumulates or is injected while the data is in transit over the selected media.

CY7C9689 can drive all standard fiber-optic interface modules that support standard PECL interface signals. These electro-optical modules are suitable for communicating over distances from a few meters to several kilometers. Fiber-optic interconnect offers the longest distances and the lowest interference potential of all transmission media.

Table 2. CY7C9689 and Am7968 TAXIchip Signal Functional Similarities

CY7C9689	Am7968	Comments
TXDATA[7:0]	DI7–DI0	Functionally equivalent.
TXDATA[9:8]/ TXCMD[2:3]	DI9, DI8/ CI2, CI3	Functionally equivalent.
TXCMD[1:0]	CI1–CI0	Functionally equivalent.
BYTE8/$\overline{10}$	DMS	CY7C9689 only supports 8- and 10-bit data-bus widths. The Am7968 also supports a 9-bit data bus configuration.
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Resets all CY7C9689 internal logic. Resets TAXI PLL only.
OUTA± OUTB±	SEROUT±	CY7C9689 provides two differential PECL-compatible serial drivers for links terminated to V_{DD}-1.3V. The Am7968 has one differential PECL serial driver for a link terminated to V_{CC}-2.0V.
REFCLK	X1	Functional equivalent when the X1 pin of the Am7968 is driven by an external TTL frequency source.
TXEN & TXCLK or TXEN & REFCLK	STRB	When internal FIFOs are enabled, TXEN and TXCLK in combination can emulate the STRB signal. When internal FIFOs are bypassed, TXEN and REFCLK in combination can emulate the STRB signal.
TXSC/$\overline{D}$	CI0–CI3	TXSC/$\overline{D}$ = HIGH is equivalent to one or more command bits on CI0–CI3 being a logic-1 (denotes a command character). TXSC/$\overline{D}$ asserted LOW is equivalent to all of the command bits on CI0–CI3 being a logic-0 (denotes a data character). TXSC/D can be generated by OR-ing the command bits together.

Table 3. CY7C9689 and Am7969 TAXIchip Signal Functional Similarities

CY7C9689	Am7969	Comments
RXDATA[7:0]	DO7–DO0	Functionally equivalent.
RXDATA[9:8]/ RXCMD[2:3]	DO9, DO8/ CO2, CO3	Functionally equivalent.
RXCMD[1:0]	CO1-CO0	Functionally equivalent.
BYTE8/$\overline{10}$	DMS	CY7C9689 supports 8-bit and 10-bit data bus widths only. The Am7969 also supports a 9-bit data bus configuration.
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Resets all CY7C9689 internal logic. Resets TAXI PLL only.
INA±, INB± A/$\overline{B}$	SERIN±	CY7C9689 provides two differential PECL-compatible serial receivers. A/$\overline{B}$ selects one input or the other. The Am7969 provides one differential PECL serial receiver.
RXSC/$\overline{D}$	DSTRB, CSTRB	The RXSC/$\overline{D}$ output of the CY7C9689 is HIGH when the received character is a command character, and LOW when the received character is a data character. RXSC/$\overline{D}$ may be gated with RXCLK to generate the equivalent DSTRB and CSTRB signals.
RXCLK	CLK	Functional equivalence in the CY7C9689 when $\overline{\text{FIFOBYP}}$ is LOW.
REFCLK	X1	Functionally equivalent when the X1 pin of the Am7969 is driven by an external TTL frequency source.
VLTN	VLTN	Functionally equivalent. Additional functionality in CY7C9689 BIST mode.

For lower-cost applications, CY7C9689 can directly drive wire transmission lines. The main distance-determining factors when using wire links are related to the characteristics of the cable. Wire transmission lines have significant frequency-dependent attenuation that causes jitter as a direct function of the data-rate and the media length. Uncompensated transmission line lengths are limited much more by jitter (and the jitter tolerance of the receiver) than by actual signal attenuation. The detrimental effect of jitter can be lessened with the addition of a suitable attenuation-compensation filter that matches the attenuation characteristics of the cable. This filter trades low-frequency receiver differential voltage amplitude for jitter reduction and increases the possible transmission distance. When using wire transmission lines, other issues beyond transmission distance often determine transmission line suitability. These issues include both radiated emissions and susceptibility to external disturbance that must be examined prior to selection of a media type for the link.

A simple compensation filter, built from passive components, can often increase reliable transmission distance to more than twice that of typical uncompensated distances. For more information see the application note “HOTLink Copper Interconnect—Maximum Length vs. Frequency.”

4. Can the PECL inputs and outputs of CY7C9689 products be connected to ECL (–5.2V) devices?

The +5.0V PECL-compatible inputs and outputs are directly compatible with true ECL (10K, 10KH, 100K, etc.) running on +5V power supplies. Connections between the CY7C9689 PECL-compatible I/O and ECL running on –5.2V is easily accomplished by capacitor-coupling the serial data lines. For those few areas that require a DC connection, PECL-to-ECL and ECL-to-PECL translators are available from a number of manufacturers. Details on these coupling techniques are included in the Cypress application note “HOTLink Design Considerations.”

When connecting the PECL-compatible serial outputs of the CY7C9689 to any load, the outputs must be biased to operate into V_{DD}–1.33V instead of the V_{DD}–2V found on true ECL outputs.

5. What happens when the PECL inputs of the CY7C9689 Receiver are left open?

The single-ended PECL input on the CY7C9689 Receiver is implemented using a high-impedance CMOS input driver. While the input does include ESD protection circuitry, it does not apply bias to the input. If the single-ended CARDET input is left unconnected, it remains indeterminate and can float anywhere between V_{DD} and V_{SS}. If CARDET floats to a voltage level corresponding to a logic LOW, then the Receiver $\overline{LFI}$ output signal will assert LOW, indicating a link fault. To prevent this fault indication, CARDET can be connected to V_{DD} through a 1-kΩ to 5-kΩ resistor.

The differential PECL line receivers are internally biased to approximately $V_{DD}/2$. If both inputs of a differential line receiver are left unconnected, the receiver output is undefined.

If the A/$\overline{B}$ select input is biased to select an unconnected differential line receiver, the non-differential noise that appears on the floating inputs is amplified and interpreted as serial data. This may cause random parallel data output changes to be observed on the RXDATA or RXCMD buses. If the internal decoder is enabled, the VLTN output will assert if any decode errors are found in the random data. When VLTN reports an invalid character, the RXDATA and RXCMD buses do not change, but continue to present the last valid character output.

During normal operation, the A/$\overline{B}$ select pin should be biased to only select active inputs. For unused differential inputs, the unused line receiver should be externally biased to prevent noise from coupling into the device. This is best accomplished by connecting one of the unused inputs (either one) to V_{DD} or V_{SS} through a 1-kΩ to 5-kΩ resistor, while leaving the other input of the differential pair unconnected (self biased to $V_{DD}/2$).

6. What special power-supply bypassing is required for CY7C9689?

CY7C9689 requires no special considerations for power-supply bypassing beyond that normally associated with high-speed logic. This typically includes the use of a ground plane, a V_{DD} plane, and bypassing using multiple RF-quality chip capacitors. Each of the ground pins of a CY7C9689 should connect directly to the ground plane using short (<6 mm) traces and vias. All of the V_{DD} pins should connect to a V_{DD} area under the CY7C9689, which is then connect to the board V_{DD} through a single via. Connect one 10- to 22-nF capacitor (based on operating character clock rate) between each V_{DD} pin and GND. For more information see the “Using Decoupling Capacitors” application note and the *Printed Circuit Board Layout Suggestions* in the CY7C9689 data sheet.

7. If the connection between the CY7C9689 Transmitter and Receiver is briefly interrupted, how long does it take for the PLL to relock?

The exact behavior of the CY7C9689 Receiver depends on the length and cause of the interruption. If the interruption is synchronous with the data (i.e., data bits disappear without any significant disturbance to the placement of the final few data transitions), and lasts for less than a few dozen characters, it is probable that the PLL will relock on the very first bit. If the interruption is asynchronous (i.e., the timing of the final few transitions is disturbed) or if the synchronous interruption lasts longer than a few dozen characters, the PLL should relock within the first one or two characters after resumption of the data

stream. If a long interruption occurs that is not synchronous to character boundaries, the receiver may lose character synchronization when the PLL relocks. In this case, the data will need to be reframed to a 10-bit JK or 12-bit LM sync character.

If the interruption is asynchronous, and the link interface allows noise to be injected into the serial inputs of the CY7C9689 Receiver, the time to relock the PLL becomes much harder to predict. If the injected noise causes the PLL to track within its frequency offset limits (approximately ±1300 ppm of the REFCLK frequency) the PLL will reacquire in a few characters (typically less than 30) after a good data stream reappears. If the PLL frequency has been moved to its offset limits by the input noise, it may take more than 250–300 characters before the PLL locks to the good data. When the PLL hits the frequency offset limit, it recenters itself at the REFCLK frequency and then attempts to lock to the data. While the PLL is out of lock (after experiencing a data stream interruption) the frequency of RXCLK does not wander beyond the offset limits.

8. If the connection between CY7C9689 Transmitter and Receiver is broken, what comes out of the receiver?

The exact behavior of CY7C9689 Receiver is difficult to predict when the serial data link is broken, since there are so many ways that the link itself can behave. The following behaviors are typical under certain input conditions:

a) Clean link break with no extraneous noise input into serial inputs (non AC-coupled or optical interface).
Encoder Bypassed, Reframe–OFF, FIFOs Bypassed ($\overline{\text{ENCBYP}}$ = $\overline{\text{FIFOBYP}}$ = RFEN = LOW):

- RXCLK runs at REFCLK frequency.
- $\overline{\text{LFI}}$ is asserted LOW.
- $\overline{\text{RXEMPTY}}$ is deasserted.
- VLTN is deasserted LOW.
- RXDATA[7:0] and RXCMD[3:0] (8-bit mode) and RXDATA[9:0] and RXCMD[1:0] (10-bit mode), typically go LOW. If the terminations are exactly matched, then they may all be indeterminate but continue to change relative to RXCLK↑.

b) Clean link break with no extraneous noise input into serial inputs (AC-coupled or optical interface).
Encoder Bypassed, Reframe–OFF, FIFOs Bypassed ($\overline{\text{ENCBYP}}$ = $\overline{\text{FIFOBYP}}$ = RFEN = LOW):

- RXCLK runs at REFCLK frequency.
- $\overline{\text{LFI}}$ is asserted LOW.
- $\overline{\text{RXEMPTY}}$ is deasserted.
- VLTN is deasserted LOW.
- RXDATA[7:0] and RXCMD[3:0] (8-bit mode) and RXDATA[9:0] and RXCMD[1:0] (10-bit mode) typically are indeterminate, but continue to change relative to RXCLK↑.

c) Noise injection into serial inputs.
Encoder Bypassed, Reframe–OFF, FIFOs Bypassed ($\overline{\text{ENCBYP}}$ = $\overline{\text{FIFOBYP}}$ = RFEN = LOW):

- RXCLK runs at REFCLK frequency ±0.2% and may wander between its range limits and the center frequency, as the receive PLL responds to the input transitions in the injected noise.
- $\overline{\text{LFI}}$ is asserted LOW.
- $\overline{\text{RXEMPTY}}$ is deasserted.
- VLTN is deasserted LOW.
- RXDATA[7:0] and RXCMD[3:0] (8-bit mode) and RXDATA[9:0] and RXCMD[1:0] (10-bit mode), are indeterminate but continue to change relative to RXCLK↑.

d) Clean break with no extraneous noise input into serial inputs (non AC-coupled or optical interface).
Encoded Mode, **Reframe–OFF, FIFOs Bypassed ($\overline{\text{ENCBYP}}$ = HIGH, $\overline{\text{FIFOBYP}}$ = RFEN = LOW):**

- RXCLK runs at REFCLK frequency.
- $\overline{\text{LFI}}$ is asserted LOW.
- $\overline{\text{RXEMPTY}}$ may toggle occasionally when a JK or LM is received if RXMODE9[1:0] is not 00; otherwise, $\overline{\text{RXEMPTY}}$ is deasserted.
- VLTN may assert HIGH to indicate decode errors.

- RXDATA[7:0] and RXCMD[3:0] (8-bit mode) and RXDATA[9:0] and RXCMD[1:0] (10-bit mode), typically go LOW. If the terminations are exactly matched, and they may be indeterminate but continue to change relative to RXCLK↑.

e) Noise injection into serial inputs.
Encoded Mode, **Reframe–OFF, FIFOs Bypassed ($\overline{\text{ENCBYP}}$ = HIGH, $\overline{\text{FIFOBYP}}$ = RFEN = LOW):**

- RXCLK runs at REFCLK frequency ±0.2% and may wander between its range limits and the center frequency randomly controlled by the injected noise.
- $\overline{\text{RXEMPTY}}$ may toggle occasionally when a JK or LM is received if RXMODE9[1:0] is not 00; otherwise, $\overline{\text{RXEMPTY}}$ is deasserted.
- VLTN may assert HIGH to indicate decode errors.
- RXDATA[7:0] and RXCMD[3:0] (8-bit mode) and RXDATA[9:0] and RXCMD[1:0] (10-bit mode), may toggle HIGH and LOW. If the terminations are exactly matched, they may be indeterminate but continue to change relative to RXCLK↑.

f) Noise injection into serial inputs.
Either Mode, **Reframe–ON, FIFOs Bypassed ($\overline{\text{FIFOBYP}}$ = LOW, RFEN = HIGH)**

- RXCLK runs at REFCLK frequency ±0.2% and may wander between its range limits and the center frequency randomly controlled by the injected noise.
- $\overline{\text{RXEMPTY}}$ may toggle occasionally when a JK or LM is received if RXMODE9[1:0] is not 00; otherwise, $\overline{\text{RXEMPTY}}$ is deasserted.
- VLTN is deasserted (LOW) when the decoder is bypassed, but may assert HIGH to indicate decode errors when the decoder is enabled.
- RXDATA[7:0] and RXCMD[3:0] (8-bit mode) and RXDATA[9:0] and RXCMD[1:0] (10-bit mode), may toggle HIGH and LOW. If the terminations are exactly matched, they may be indeterminate but continue to change relative to RXCLK↑.

g) Noise injection into serial inputs.
FIFOs Enabled, Encoded Mode, **Reframe–ON ($\overline{\text{ENCBYP}}$ = $\overline{\text{FIFOBYP}}$ = RFEN = HIGH)**

- RXCLK is externally generated (input).
- $\overline{\text{RXEMPTY}}$ is asserted if the Receiver FIFO is empty, otherwise it will deassert relative to RXCLK↑.
- $\overline{\text{RXFULL}}$ is asserted if the Receiver FIFO is full; then as characters are read out relative to RXCLK↑, $\overline{\text{RXFULL}}$ will deassert. If RXMODE[1:0] is 00 and RXCLK is slower than the serial character reception rate, the Receiver FIFO will eventually overflow (as the random noise is interpreted as serial data), and decoded characters are written to the Receive FIFO as dictated by the RXMODE[1:0] setting. In this scenario $\overline{\text{RXFULL}}$ stays asserted.
- VLTN may assert HIGH to indicate decode errors. The corresponding invalid character is not written to the Receive FIFO, instead the most recent valid character is written to the FIFO to prevent the data bus from changing.
- RXDATA[7:0] and RXCMD[3:0] (when in 8-bit mode) or RXDATA[9:0] and RXCMD[1:0] (when in 10-bit mode), will output the characters previously stored in the Receive FIFO relative to RXCLK↑. When the previously stored FIFO contents are drained, then data and command bus signals may toggle HIGH and LOW as new characters are detected in the link noise. If the serial line terminations are exactly matched, they may be indeterminate but continue to change relative to RXCLK↑.

9. What is the correct operation of the RFEN input in the receiver section? What is the minimum number of SYNC characters required to ensure proper framing? How can I tell if the receiver is framed properly?

Recovery of information from a serial data stream requires recovery of a bit clock (accomplished by the receiver PLL) and character synchronization (accomplished by the receiver framer). The CY7C9689 framer is enabled or disabled by the RFEN input. In well behaved, standardized, point-to-point protocols that are seldom switched, the control of the character framer may be managed as a service in the protocol controller. This service monitors the VLTN pin for specific error criteria, and enters a framing subroutine. This framer-service sets RFEN=HIGH while framing and LOW during normal message transactions.

In less well behaved systems, or systems that switch data sources often, it may be necessary to leave RFEN=HIGH for long periods (or permanently). Leaving RFEN HIGH opens the system to potential misframing caused by corrupted bit sequences that happen to match the SYNC character. Since this Alias SYNC is unlikely to be aligned to the normal character boundaries, it causes the framer to align the parallel data to the wrong character boundary resulting in invalid decoding of the

following characters. In the CY7C9689, when RFEN is set HIGH, the receiver searches the received data stream for the bit pattern matching the 10-bit JK character (11000 10001) when in 8-bit mode, or the 12-bit LM character (011000 100011) when in 10-bit mode. When the JK or LM is found, the framer changes the character boundaries to match that of the received SYNC character.

In addition to upper-level protocol error detection mechanisms (common in communication links), the CY7C9689 Receiver offers several indications that a link is misframed. For example, in FIFO Bypass mode with the encoder enabled and RXMODE[1] = HIGH, the $\overline{\text{RXEMPTY}}$ output asserts for every JK or LM detected. If RFEN is LOW, the only JK or LM that can be detected is one that is properly framed, and all others are passed through as violations in the received data. If the protocol in use has a maximum packet size or a minimum number of JKs or LMs, a simple retriggerable-one-shot can be used to detect when framing has been lost. In this example, if the one-shot is retriggered by the properly spaced JKs or LMs, then the data is properly framed. If the one-shot times-out (indicating that too much time had elapsed between SYNC characters), the data would automatically be reframed by raising RFEN until the next JK or LM indication.

Another indication of a misframed link occurs when the Decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH). In this mode, the VLTN output indicates decoder errors. If these errors occur frequently, it is typically the result of character misframing. Normal data sent over typical data links has a very low error rate (e.g., bit-error-rates of better than $1x10^{-12}$ are quite common, where BER=$1x10^{-12}$ ≈ one error per one hour and 23 minutes at 200 MBaud). Therefore, if VLTN is frequently asserted it can be assumed that the cause is misframing. Another retriggerable-one-shot could be used to detect this condition, or it could be detected by a simple synchronous state machine constructed in a PLD.

10. What happens to the receiver's clock and parallel outputs when it reframes with the FIFOs bypassed?

The CY7C9689 implements a parallel framer. Internally, a barrel shifter is used to align the recovered data bits with a continuous character-rate clock. With the Receive FIFO bypassed, when the receiver frames upon detection of the 10-bit JK (when in 8-bit mode) or the 12-bit LM character (when in 10-bit mode), the framer shifts the offset data to align with the character clock. The output RXCLK is not affected. In this way, RXDATA and RXCMD always remains synchronous to the output clock. Because RXCLK remains continuous even during framing operations, it can be buffered and replicated externally using PLL-based circuits like the CY7B991 RoboClock.

11. What does BIST do? How can I add BIST to my system without redoing all calculations for my critical interface timing? What functionality does the BIST test and guarantee?

The CY7C9689 Built-In Self-Test (BIST) allows a clear and unambiguous check of the CY7C9689 Transmitter section (excluding the Transmit FIFO), Receiver section (excluding the Receive FIFO), and the serial link connecting them. As part of an off-line or on-line diagnostic, this feature allows the user to ensure that the interconnect link is fully operational and that any other diagnostic failure indications are caused by system blocks above the physical layer. BIST allows the CY7C9689 adapter card manufacturer to do a quick link-quality test without the necessity of bringing up a fully functional system to do link testing.

BIST is controlled by the $\overline{\text{TXBISTEN}}$ and $\overline{\text{RXBISTEN}}$ inputs. Only a few connections and minimal external logic are necessary to add BIST to an otherwise complete system (see the Cypress application notes "HOTLink Built-In Self-Test"). BIST status indications appear on the $\overline{\text{RXFULL}}$ and VLTN outputs which are easily monitored by logic internal or external to the data-flow controller.

In BIST mode, the CY7C9689 Transmitter generates a $2^9 - 1$ (511 character) pseudo-random pattern using an internal pipeline register configured as a Linear Feedback Shift Register (LFSR). The CY7C9689 Receiver section compares the serial BIST data stream received with identical BIST patterns generated in its corresponding LFSR. Nearly all of the logic in the transmitter section (except the input pins and Transmit FIFO) and receiver section (excluding the Receive FIFO and output register) are checked by BIST. All of the serial link interconnect components are exercised with normal data and command patterns, which are checked character-by-character in real time and at full link operating speed.

12. What fiber-optic components are compatible with CY7C9689 products?

Standard fiber-optic interface components capable of operation at HOTLink data rates are all compatible with the CY7C9689. The following is a representative but not comprehensive list of optical interface manufacturers. A more complete list of vendors and products is included in the "HOTLink Support Component Vendors" list.

AMP/Lytel Division
61 Chubb Way
P.O. Box 1300
Somerville, NJ 08876
(908) 685-2000

Hewlett-Packard
Components Division
370 West Trimble Road
San Jose, CA 95131
(800) 535-7449 or (408) 435-6342

Sumitomo Electric
Fiber Optics Corporation
777 Old Sawmill River Road
Tarrytown, NY 10591-6725
(914) 347-3770
http://www.sel-rtp.com/

CTS Corp
1201 Cumberland Ave.
West Lafayette, IN 47906-1388
(317) 463-2565
http://www.ctscorp.com/

Siemens Fiber Optic Components
19000 Homestead Road
Cupertino, CA 95014
(408) 725-3436

Optical Communications Products
9736 Eton Avenue
Chatsworth, CA 91311
(818) 701-0164
http://www.ocp-inc.com/

13. What is the significance of the CY7C9689 claim of "no external PLL components"?

CY7C9689 Transceiver has completely integrated the PLL clock multiplier and data separator functions. These functions are implemented with high-performance phase-locked loops (PLLs) that have been tuned for maximum performance and minimum system noise sensitivity. In competitive products that purport to offer similar functions, these PLLs are often implemented with external filter and frequency setting components with the goal of achieving maximum performance. But these very same external components are the largest cause of end-user complaints and random system failures because they expose the most critical analog signals in the circuit to the external noises that abound in normal systems. External components require critical, costly, and time consuming printed circuit board layout as well as high-speed analog and digital design techniques that are unfamiliar to many system integrators. CY7C9689 product is designed and built using fully differential analog and digital circuits to give the lowest possible output jitter and highest possible jitter tolerance. There are no external components to compromise system performance in unexpected and unpredictable ways. For more information, refer to the HOTLink Transmitter Jitter section of the "HOTLink Jitter Characteristics" application note.

14. What is the intrinsic Bit-Error-Rate of CY7C9689 Transceiver?

CY7C9689 BER = Zero. The CY7C9689 Transceiver has no intrinsic failure modes. If the power is maintained and the link connecting a CY7C9689 Transmitter to a CY7C9689 Receiver has reasonable design margin, the total error rate is exactly that of the interconnect media. Link error rates of $<<1x10^{-15}$ are common and easily achieved. Even with worst-case design and end-of-life derating, BER $<<1x10^{-12}$ presents no significant challenge.

The real question being asked is, "What will my link BER be when using CY7C9689?" The answer to this question involves the design of the serial transmission link and the margins designed into it. CY7C9689 does not significantly degrade the BER of the link. For more information, refer to the "Understanding Bit-Error-Rate with HOTLink" application note.

15. How much jitter is created by the transmitter? How much jitter is created by the receiver? What is the significance of the CY7C9689 Transmitter requirement for a crystal-stable clock source?

The phase-locked loops (PLLs) in the CY7C9689 Transmitter and Receiver act like low-pass filters to jitter that is embedded in the data or clock signal source. For the transceiver, the signal source is the REFCLK input. Jitter frequency components that appear at REFCLK that are below the natural frequency of the PLL filter (approximately 400 kHz) are passed unattenuated. Spectral components above the natural frequency are attenuated at about 6 dB/octave. Frequency components that fall very near the natural frequency of the filter are slightly amplified (typically 1.5 dB). These are the normal characteristics of a Type-2, second-order PLL filter. When the transmitter is fed by a low-jitter clock source, typical output jitter is less than 25 ps RMS and 240 ps peak-to-peak.

It is possible to measure significantly more jitter than that which is actually present if the complete system is not well understood. A few hundred millivolts of V_{DD} noise, while insignificant to the logic of a normal system board, adds imaginary jitter to the measured output. This imaginary jitter appears because a single ended oscilloscope sees the waveform as if it were measured against a fixed threshold, while the differential serial interface sees V_{DD} noise as a common mode signal to be ignored (e.g., 100 mV of V_{DD} noise could create 100–200 ps of imaginary jitter). Likewise, the normal method of measuring peak-to-peak jitter (an infinite persistence scope trace), shows larger jitter than that contributed by the CY7C9689 Transmitter. Low frequency jitter (wander) in the oscillator, scope trigger, temperature, and voltage related delay variations all contribute to the width of the displayed scope trace. Delay variations include TTL threshold variations that cause apparent delay variation (e.g., 100 mV of TTL threshold change can cause 100–200 ps of apparent jitter).

The signal source for the receiver is the serial data stream and, like the transmitter, it passes the spectral components of received jitter that fall below the natural frequency of its filter (approximately 300 kHz to 1000 kHz depending on actual data transition density being received). Frequency components above the natural frequency are attenuated and there is minor

jitter peaking at about the natural frequency of the PLL. Since the characteristics of the input jitter determine the jitter content on the RXCLK output (the only place to directly measure Rx-PLL jitter), it is somewhat difficult to predict the output jitter. Jitter from normal data is wide-bandwidth, has significant high-frequency content, and can have peak-to-peak amplitude of up to about 75% of a bit time. If the serial data contains a significant low-frequency jitter component (typical in crystal oscillators and some pulse generators) the output jitter measured on the RXCLK pin could be much higher. Jitter measurements at the receiver output can be more misleading than those associated with the transmitter serial outputs, since all measurements are made on a single-ended TTL output.

The jitter characteristics mentioned here affect system performance in multiple ways. Low-frequency jitter (below the bandwidth of either transmitter or receiver PLL) is treated as wander. For purposes of the PLLs, wander (usually caused by low-frequency power supply variations or temperature fluctuations within the timing ICs) does not reduce the system timing margins and does not contribute to bit-error-rate. Wander can affect system timing at interfaces where the transmitter clock source is used to clock information received from a receiver tracking data from another clock source. The variation in clock frequencies may violate set-up and hold times, the exact problems usually solved by FIFO memories in typical communication systems.

High-frequency jitter (at or above the natural frequency of the PLL filters) may contribute to BER. High-frequency jitter can be caused by the clock source, media transfer characteristics, or external noise. The recovered internal bit-rate clock does not track high-frequency jitter above the PLL natural frequency. High-frequency jitter, therefore, may cause a bit edge to move into the receiver sampling window causing the bit to be erroneously sampled; i.e., a bit error.

A suitable clock source should be selected with the above effects in mind. The only clock source guaranteed to offer the required stability and high-frequency specifications is a crystal oscillator. With a crystal oscillator, high-frequency jitter is minimal, and low-frequency wander is usually small and very low frequency. Frequency accuracy is easily guaranteed by mechanical means, and high-accuracy devices are relatively low-cost. Free-running resistor-capacitor (RC) oscillators, logic-gate ring oscillators, or inductor-capacitor (LC) oscillators generally include too much high-frequency jitter, and experience wide frequency variation as a function of process and environmental conditions and are unsuitable for this application.

16. What is the latency through a CY7C9689 Transmitter and Receiver?

When the internal FIFOs are disabled ($\overline{\text{FIFOBYP}}$ is LOW), the input data is stored in the transmitter input register on the rising edge of REFCLK, making this time-zero. When configured for 8-bit mode, approximately 31 bit-times (i.e., 31 times the period of REFCLK÷10) following this, the first encoded bit of that character will emerge from the OUTA± and OUTB± pins. After the transit time of the serial link (which can be significant), that bit will appear at the receiver. Transit times for typical serial links include the propagation delay of the optical modules (typically 5–10 ns for the pair), if any, and the propagation rate in the link media (i.e., approximately 1 ns/ft in copper, and 2 ns/ft in multi-mode optical cable). Due to clocking variations in the high-speed PLL circuitry and framer logic, a best case minimum latency bound and worst case maximum latency bound is possible within the Receiver. For the best case scenario, approximately 35 bit-times after the first data bit is presented at the input of the receiver plus a minimum delay of 2 ns through the parallel output drivers, data appears at the RXDATA or RXCMD outputs relative to RXCLK↑. For the worst case scenario, approximately 46 bit-times after the first data bit is received at the input of the receiver plus a maximum delay of 15 ns through the output driver circuitry, data appears at the RXDATA or RXCMD outputs relative to RXCLK↑. In 8-bit mode, the total latency of a CY7C9689 Tx/Rx pair is approximately the link delay plus 66 bit-times and 2 ns best case, or the link delay plus 77 bit-times and 15 ns worst case.

In 10-bit mode the latency through the transmitter is approximately 34 bit-times (i.e., 34 times the period of REFCLK÷12). In the Receiver a similar best case minimum latency bound and worst case maximum latency bound is possible. For the best case scenario, approximately 41 bit-times after the first data bit is received at the input of the receiver plus a minimum delay of 2 ns through the output driver circuitry, data appears at the RXDATA or RXCMD outputs relative to RXCLK↑. For the worst case scenario, approximately 54 bit-times after the first data bit is received at the input of the receiver plus a maximum delay of 15 ns through the output driver circuitry, data appears at the RXDATA or RXCMD outputs relative to RXCLK↑. Correspondingly in 10-bit mode, the total latency of a CY7C9689 Tx/Rx pair is approximately the link delay plus 75 bit-times plus 2 ns best case, or the link delay plus 88 bit-times plus 15 ns worst case.

When the FIFOs are enabled ($\overline{\text{FIFOBYP}}$ is HIGH) additional FIFO latency is encountered in the Transmit and Receive data paths. Both transmit and receive FIFOs achieve minimal latency when the TXCLK and RXCLK rates are slower than the REFCLK rate; otherwise, the time it takes to transmit a new character is lengthened by the additional time needed to transmit the previously stored characters. In 8-bit mode, with an initial empty transmit and receive FIFO, the transmit FIFO adds 8 bit-times, plus 2 additional TXCLK cycles to the overall delay, while the receive FIFO adds 1 bit-time, plus 4 additional RXCLK cycles to the overall delay. In 10-bit mode, with an initial empty transmit and receive FIFO, the transmit FIFO adds 9 bit-times, plus 2 additional TXCLK cycles to the overall delay, while the receive FIFO adds 1 bit-time, plus 4 additional RXCLK cycles to the overall delay.

17. Is there a VERILOG or VHDL model of the CY7C9689?

Synopsys will offer a full-function logic model of the CY7C9689 Transceiver at a future date (exact date TBD). This model will perform all of the normal chip functions including FIFO enabling/disabling, BIST, 8-bit/10-bit Encoded, and Bypass modes of operation. This model accurately models the "real" part and has been validated by having them run the actual-chip design-simulation vectors and the outgoing-test vectors. Synopsys offers a wide variety of standard product logic models that run on various simulation platforms. Additional information can be found at http://www.synopsys.com/.

18. What is the thermal data for CY7C9689 100-pin TQFP package? What is the max. junction temperature (max. T_j)?

The thermal resistance of the CY7C9689 for different air flow rates is summarized in *Table 4*.

Table 4. Thermal Resistance vs. Air Flow

Air Flow (Lineal feet per minute)	Thermal Resistance θ_{JA} (°C/Watt)
0	45.3
200	37.9
400	34.8

The maximum junction temperature (max. T_j) for the CY7C9689 is 155°C.

19. I need to estimate the reliability of CY7C9689 in my design. How many components does it contain?

Table 5. CY7C9689 Reliability Data

CY7C9689 Parameter	Values
Number of components	199,216
Number of transistors	197,827
Number of gates	25,000
Percent digital by gate count	49%
Percent analog by die area	50%
Die size	163 mils x 162 mils 4.14 mm x 4.11 mm

Built on Cypress Standard 0.42-micron CMOS. Designed for reliable operation at temperatures $-55°C < T_j < 155°C$. All pins characterized to withstand ESD >2001V (per MIL_STD_883, Method 3015). Wafer Fab Capability in San Jose, CA, Round Rock, TX and Bloomington, MN

20. What is the expected power consumption of the CY7C9689 at various serial data rates?

The typical power consumption of the CY7C9689 is summarized in *Table 6* for 4.5V, 5.0V, and 5.5V operation at 25°C at listed serial signaling rates.

Table 6. Power at Various Serial Data Rates

Serial Signaling Rate	Power @ 5.5V	Power @ 5.0V	Power @ 4.5V
50 MBaud	643 mW	531 mW	407 mW
100 MBaud	731 mW	589 mW	453 mW
150 MBaud	900 mW	716 mW	517 mW
200 MBaud	1010 mW	806 mW	583 mW

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