LVDS vs. Low Voltage Differential Signaling

Purpose

While the phrase “Low Voltage Differential Signling for Interface Circuilts” (LVDS) often implies a high-performance, high-speed communication channel that is completely specified by that single phrase, in reality the term “LVDS” does not, in itself, imply either satisfactory high-speed performance or even compatible signaling.

LVDS does not have the same performance as other forms of Low Voltage Differential Signaling like ECL/PECL and CML devices. LVDS is **not** the industry standard for most high-speed serial interfaces.

This paper describes what Standards-Compliant LVDS is and isn’t, and shows that the actual data sheet values describing the input/output parameters must be examined in detail to ensure interoperability, rather than just the ability of the component to state “LVDS Compliant.”

Background

A number of semiconductor companies now support LVDS for serial and parallel communication between semiconductor devices. In addition, a number of recent trade journals espouse the features and advantages of LVDS for high-speed communications. The purpose of this application note is to help clear up the confusion surrounding the generic term “LVDS”, and to explain how it differs from the signaling used for the highest-speed interfaces.

LVDS

LVDS identifies a technology that uses differential signaling to communicate between electrical devices. While documented in both national and international standards, the lack of coordination between these standards (and the poor selection of a common name for this signaling type) places the engineer at a disadvantage.

Signaling Types

There are two common electrical methods to transmit data from a source to a destination. One method uses a “single-ended” signaling concept. Single-ended signaling makes use of two conductors between the transmitter and receiver: a dedicated signal-line to send the signal from transmitter to receiver, and a common ground return shared by all signals.

The other method is a “differential” signaling concept. In differential signaling, true and complement forms of the signal are sent from the transmitter to the receiver. While this also uses two conductors between these devices, they now both carry active signals, and neither is shared with other signals. Note that differential signaling uses twice as many signal lines as single-ended signaling.

Advantages of Differential Signaling

Differential signaling has a number of important advantages over single-ended signaling due to the ability of the differential receiver to reject any signal component that is *common* to both lines (typically noise sources). This ability is commonly referred to as *common-mode* rejection.

This ability to reject noise occurs because the receiver is only sensitive to the difference between the two inputs, and noise that is picked up by the signal lines is generally *common* to both, allowing it to be rejected. With single-ended signaling, the external noise can not be separated from the signal itself.

Because differential signaling rejects common-mode noise, lower voltages and currents can be used for reliable communications versus those used by single-ended methods. An additional benefit from the lower voltages currents of differential signaling is that this often translates to lower power levels in the drivers.

History and Development of Differential Signaling

Emitter Coupled Logic

The advantage of using differential signaling for common-mode rejection and the need to develop high speed data transmission was part of the reason for the development of ECL (emitter-coupled logic). This technology has long been a workhorse in specialized applications like mainframe computers. Because of its speed, good designs required a working knowledge of transmission line theory and termination techniques. Also, the fast edge-rates of the ECL drivers produced some signal radiation and hence coupling to other signal lines. ECL devices supporting differential signaling multiple edge-rates were introduced to help solve some of these problems.

ECL achieves its fast edge rates, and hence high-speed data rate, through the use of current-mode logic or CML. CML is a general name for a logic family that uses transistors as drivers that route current while staying in the linear range of transistor operation. These transistors are never switched fully off or on. Bias currents sent to the driving transistor to switch the device on and off gave rise to the term current mode.

Saturated Logic Families

This method can be contrasted with a saturated switching technique like CMOS or TTL. With saturated-switching logic, the switching speed of the transistor driver is limited to the amount of time needed to sweep out charge in the transistor as it tries to switch from one logic state to the other. The highest data speed with the fastest rise and fall times is obtained using the non-saturated, linear type of logic family, with CML being one such logic family.

Transmission Media

The electrical characteristics of the transmission media are critical to the success of reliable high-speed data transmission. Any change in the impedance of the transmission media will reflect parts of the signal back to the source. These reflections can cause edge rates to degrade, create false signals, and increased radiated emissions. These effects can produce data

errors. Transmission losses in the media also limit the maximum range over which signals can be sent.

In general, the use of low-voltage differential signals, generated by a CML logic family, has been a standard practice for data communications in many high-speed circuit applications. Attention to the electrical transmission path has also been part of the needed work.

LVDS and Standards

What then is the phrase “LVDS” about and what advantages, if any, does it have over the techniques used in the past?

The LVDS concept developed from a need for the previously discussed benefits of differential signaling in order to support a limited range of serial and parallel data transmission. Unfortunately, the use of the letters LVDS to stand for the general concept of low voltage differential signaling created a confusing terminology for the designers of high-speed serial communication links.

The two standards that define the electrical properties of the general LVDS technique are ANSI/TIA/EIA/-644-1995 and IEEE Std. 1596.3-1996. Of the two, the IEEE standard is the lower performance.

The ANSI standard has a recommended upper limit to the signaling rate of 655 Mbits/s, while the IEEE standard has a recommend upper limit of at least 200 Mega-transfers/second. Notice that even the signaling rate terms differ in how the data rates are specified. The ANSI standard states that the device can operate up to 655 Mbits/s, but can operate slower and still meet the specifications (clause 4.2 of the ANSI standard). Along with differing performance levels, the two standards also differ in the input/output voltage levels. In general, if the specifications in the ANSI standard are met, then the IEEE specifications will also be met since the ANSI standard is more rigorous. The ANSI standard seems to be the current desirable specification.

Both IEEE and ANSI standards call for the use of an output driver that consists of a constant current source that switches the direction of current flow in two conductors to produce the two different logic states. This current from the driver passes through a resistor at the differential receiver input that both terminates the transmission line and converts the routed current into a voltage. This voltage is in turn sensed by a receiver that only looks at the voltage across the resistor (and not the voltage between either side of the resistor and ground) to determine the Logic State of the receiver.

The actual construction of the driver is not specified in the standards, however, the reference areas of the standards (Appendices) describe a saturating type of driver, i.e., the driver transistors are either full on or off. This saturating type of driver can be contrasted with the non-saturating, higher-speed CML driver described earlier. Refer to *Figure 1* for a representation of an LVDS Driver Stage. Resistor R1, in series with the on resistance of the FETs, determines the source impedance of the driver. The 3.5 mA current through R1 properly biases the output for differential operation.

The ANSI and IEEE standards both call for differential receivers that operate within a limited common mode voltage range. The receivers also require a terminating resistor across the input. This resistor is used to electrically terminate the transmission media connecting the transmitter to receiver, and provides the differential voltage described earlier. The ANSI standard allows the resistor to be either internal or external to the physical receiver while the IEEE standard requires the terminating resistor to be internal to the receiver. Both standards have a different tolerance for the resistor, with the average value of 100Ω. The electrical impedance of the transmission media should match that of the receiver in order to avoid reflections; however, the electrical properties of the transmission media are not stated in either standard.

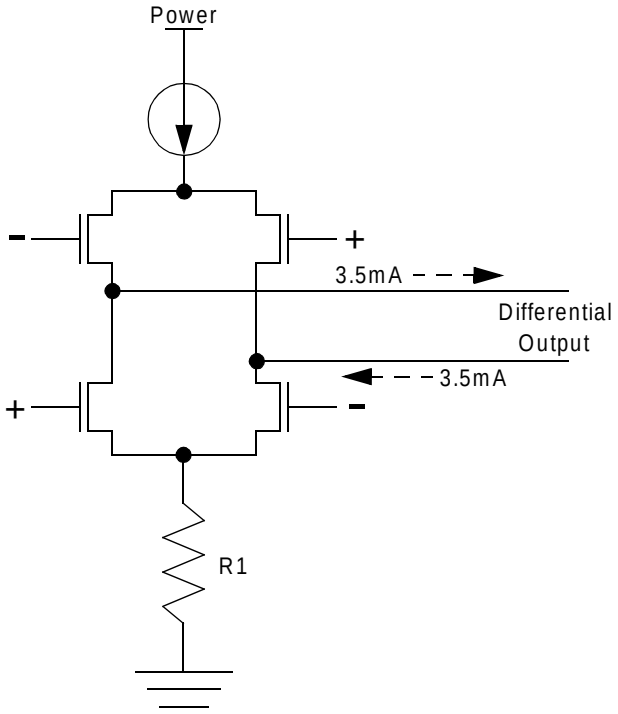

Figure 1. LVDS Output Driver

Table 1 compares some of the electrical parameters between the two LVDS standards. While all specified values are not shown, the table does contain most of the critical parameters. The values in the table highlight that the acronym LVDS does not guarantee a specific set of values. For example, the rise and fall time specifications of the drivers (key parameter for reliable high-speed data transmission) differ from one standard to the other. Note that even the maximum signaling rates are different.

Conclusion

As a design requirement, the term LVDS does not convey the sufficient information by itself. Additional questions regarding actual edge rates, impedance values, saturated versus non-saturated, media impedance, etc., are needed to achieve a product design that will reliably work for a given application.

Differential CML signaling, coupled with attention to the electrical characteristics of the transmission media, is generally used for the highest-speed signaling. While use of standards-compliant LVDS is appropriate for a number of functions, its use of saturating logic limits it to lower speed interfaces.

Table 1. LVDS Signaling Specifications

	IEEE 1596.3-1996		ANSI TIA/EIA-644		
	Min	**Max**	**Min**	**Max**	**Units**
LVDS Driver					
Rise/Fall Time	300	500	260	1500	ps
V-Diff	250	400	250	450	mV
LVDS Receiver					
Input Resistance	90	110	90	132	Ω
Differential Receive Sensitivity	100		100		mV
Signaling Rate		200		650	MBaud

LVDS was created as a way for users to take advantage of the low power and noise rejection that differential signal transmission provides over single-ended circuits, while providing general guidelines for serial transmitters and receivers. Because of the lack of coordination between different forms of LVDS, care must be used when selecting or specifying its use.