Termination and Biasing of HOTLinkII™ High-Speed Serial I/O

Purpose

This application note is one of a series of design considerations for the use of the HOTLinkII™ device. Its purpose is to aid in the design of circuits used to connect the serial high-speed inputs and outputs of the HOTLinkII. It discusses high-speed circuit termination techniques and the required DC-biasing for the serial drivers and receivers used in the HOTLink II device.

Background

The HOTLinkII serial interfaces operate over the 200- to 1500-MBaud signaling rate range. The signaling on these serial interfaces is not simply rapidly changing logic levels, but genuine high-frequency RF signals. The use of high-speed design techniques is necessary to ensure the reliable transmission of information. Failure to understand and correctly implement high-speed techniques may increase the likelihood of signaling errors in the serial data path.

Differential Method Used

There are two common electrical methods to transmit data from a source to a destination. One method uses a “single-ended” signaling concept. Single-ended signaling makes use of two conductors between the transmitter and receiver: a dedicated signal-line to send the signal from transmitter to receiver, and a common ground return shared by many signals.

The other method uses a “differential” signaling concept. In differential signaling, true and complement forms of the signal are sent from the transmitter to the receiver. While this also uses two conductors between the transmitter and receiver, they now both carry active signals, and neither is shared with other signals. Note that differential signaling uses twice as many signal lines as single-ended signaling.

Differential signaling has a number of important advantages over single-ended signaling. One of these is the ability of the differential receiver to reject signal components that are *common* to both lines. This ability is referred to as *common-mode* rejection. Since a differential receiver is only sensitive to the difference between its two inputs, and most of the noise that is picked up by the signal lines is *common* to both, the receiver becomes immune to most noise sources. With single-ended signaling, the external noise picked up by the signal-line can not be completely separated from the true signal.

Because the differential signaling method rejects the common-mode noise signals, lower voltage levels can be used for reliable transmission of serial data versus those levels used by single-ended methods while maintaining the same signal to noise ratio. An additional benefit from the use of lower voltages in differential signaling is that this can reduce the power needs of the output drivers.

The HOTLinkII provides pins for differential signaling on its high-speed serial inputs and outputs. However, the designer can use single-ended connections if the signal environment allows (this is not generally recommended). The use of single-ended or differential signaling depends on the specific noise conditions present in the system.

Impedance Definitions

In order to define the electrical properties of differential lines, various impedance definitions are used. These definitions are consequences of the fact that the signal interconnects used to link the serial outputs to serial inputs behave as transmission lines at these high frequencies; thus the surrounding electrical environment will influence the impedance of these transmission lines. Refer to *Figure 1* for a pictorial representation of the various impedances.

The resistors Za and Zb (*Figure 1*), are a visual aid used in the understanding of the various impedance calculations. In actual practice, impedance is a complex quantity that would use a reactance value along with the resistance to describe the impedance values. The two diagonal lines represent the differential signal lines, with the ground symbol indicating the presence of an RF ground around the signals. The terms Z Differential, Z Common mode, Z Odd mode, and Z Even mode in the following equations are used to describe various properties of the electrical model.

$$Z_{Differential} = Za \parallel (2 \cdot Zb) \quad \text{Eq. 1}$$

$$Z_{Common\ mode} = \frac{Zb}{2} \quad \text{Eq. 2}$$

$$Z_{Odd\ mode} = \left(\frac{Za}{2}\right) \parallel Zb \quad \text{(for differential excitation)} \quad \text{Eq. 3}$$

$$Z_{Even\ mode} = Zb \quad \text{(for common excitation)} \quad \text{Eq. 4}$$

Z Odd mode refers to the impedance of either conductor with respect to ground when the lines are driven from a differential source. *Z Even mode* is the impedance of either conductor to ground when the lines are driven from a common source.

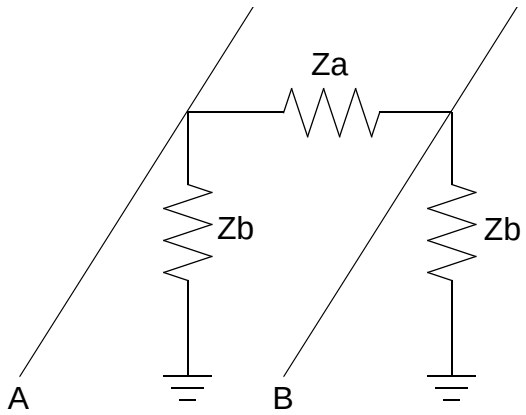

Figure 1. Balanced Transmission Line Model.

Differential sources are defined as those where the changing signal levels on one line occur at the same time but with opposite amplitude values from that of the other line. Common sources are defined as those where the changing signal levels on one line occur at the same time and amplitude as that on the other line.

The use of these “modes” aids in the analysis and measurement of transmission line impedances. Measurements of Odd mode and Common mode impedance are fairly easy to perform with test equipment. When the odd and even mode values are known, then the actual Za and Zb components can be calculated from Equations 3 and 4. This electrical model, based on Za and Zb values, provides a method to calculate the effect on signal levels due to the impedance values used.

The model shown in *Figure 1* is just one possible method to describe the electrical properties of the signal path from the serial driver to the receiver, and is used for the remainder of this application note.

Driver Circuit Description

Figure 2 represents the serial driver output circuit for the HOTLinkII. As shown, the circuit is basically a differential amplifier stage. As implemented in the HOTLinkII, the driver design uses current mode logic (CML). CML operates within the active region of the transistors, therefore they do not operate in cut-off when producing a logic one or saturate when producing a logic zero. This allows the driver switching-speed to be much faster than a driver that has to switch in and out of a saturated state. The input to the driver stage is applied to points A and B. Q1 and Q2 act as power drivers for the output. The output impedance of each driver is 50Ω, which is established by the Rs resistors.

Both driver outputs combine to provide a single differential output with Output A as the “true” output and B as the “complement.” When the impedance definitions from *Figure 1* are used, the following values are tabulated:

Driver Impedance Values

- Zb equals 50Ω.
- Za equals a high value (essentially infinite).
- Z Differential equals 100Ω.
- Z Common mode equals 25Ω.
- Z Odd mode equals 50Ω.
- Z Even mode equals 50Ω.

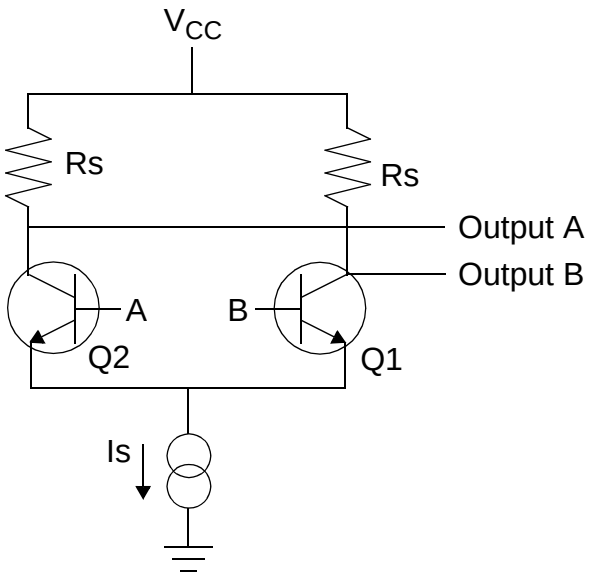

Figure 2. CML Driver Schematic.

The true and complement output signals have a common DC value because of the CML driver construction. DC-blocking capacitors are therefore needed between each output driver and the external circuit to keep this voltage from appearing as a DC-offset on the signaling lines.

Receiver Circuit Description

The serial line receiver for the HOTLinkII is constructed using a high-impedance differential receiver. Using the notation from the impedance definitions, the Rb and Ra values for the receiver are both high or essentially infinite. Since the input impedance of the receiver is high, external components are needed to perform impedance matching to the external transmission line. Because the impedance matching uses external components, optimum matching to most transmission lines can be achieved.

Since the input signals to the receiver are differential, one signal has to be more positive than the other in order to produce a valid output signal. The receiver inputs are internally DC biased to $V_{CC}/2$ in order to maximize the common mode rejection and operating range of the receiver. This biasing is provided internal to the HOTLinkII line receiver. If the source signal has a significant DC-offset (relative to the biased receiver inputs) it can be isolated from the receiver through DC-blocking capacitors.

Signal Transmission Circuit Design

When implementing an interface, the DC-blocking capacitors should be installed as close as possible to the output pins on the driver (or the input lines on the receiver). The reactance of the capacitors should be less than 1Ω at the lowest output frequency (Signaling_rate/10 for 8B/10B coded systems) and have a self-resonance greater than 3 times the highest frequency (Signaling rate * 1.5 for 8B/10B coded systems).

Single-Ended or Differential?

Differential signaling has many advantages over single-ended signaling as previously discussed. However, single-ended signaling can be used if the electrical environment allows for a sufficient signal-to-noise ratio. This would normally require fairly short signal traces and controlled cabling.

Circuit Specifics for Single-Ended

In order to convert the differential drivers to single-ended operation, the true output driver is selected as the source and the complement output should be terminated into a 50Ω load, AC-coupled to ground. The true driver output should be AC-coupled to a transmission line with an impedance equal to 50Ω. Note that for a single transmission line, there is only one impedance value, Zb, and thus there is no need for using the Za and Zb notation.

The serial transmission line should be terminated at the receiver with a 50Ω equivalent impedance. While this could theoretically be done with a pair of 100Ω resistors (as a Thévenin equivalent), this should be avoided. The tolerance on the resistors will generally be such that a small DC-offset is created between the true and complement inputs. This offset will cause duty cycle distortion (DCD) of the received signal. It is

best to terminate with a single 50Ω resistor directly to ground, followed by an AC-coupling capacitor to connect the signal to the line receiver true input. This allows the precision internal networks provide the DC restoration.

The connection must be made to the true input of the line receiver, or a signal inversion will occur. While one (or more) signal inversions are acceptable in NRZI coded data streams, they are not permitted in 8B/10B encoded data. The unused input, which should be left unconnected, will be at a $V_{CC}/2$ potential because of the internal biasing resistors.

For all single-ended connections, DC-blocking capacitors are needed at both the driver and the receiver ends of the link.

Circuit Specifics for Differential Signaling

For the differential connection, both the true and complement outputs of the driver are connected to the transmission line(s). For optimal matching, the transmission line differential impedance should be 100Ω (150Ω is often used for Fibre Channel interfaces). The transmission media impedance values can be constructed using different combinations of Za and Zb values to achieve the same value of Z Differential. For example, two isolated 50Ω coaxial cables and a closely coupled twinaxial line can both achieve the same differential impedance. For the separate coax cables, the Zb value is 50Ω and the Za value is infinite. For a twinaxial line (balanced cable), Zb and Za will have finite values which when combined give a differential value of 100Ω.

The best impedance management method is to maintain the same Zb and Za values for as much of the transmission path as possible, due to the difficult task of switching Za and Zb values while trying to maintaining a constant differential value along the transmission path. Keeping the Za and Zb values constant presents a uniform load impedance to the differential driver.

For the HOTLinkII serial driver, the Zb value is 50Ω and the Za value is very high (or infinite), thus providing a Z differential value of 100Ω. For optimal matching, the transmission media's differential impedance should have a 100Ω value. If the Za and Zb values are different than the serial driver, then the impedance change should occur as close as possible to the driver and the DC-blocking capacitors. The same Za and Zb relationship should then be maintained along the length of the path.

To allow for operation with different impedance cable, the HOTLinkII Serial Receiver uses external termination. This allows the Za and Zb values to be matched to the impedance of the actual transmission media. The terminating resistor (or resistors) along with the DC-blocking capacitors (if used) should be located as close as possible to the receiver input pins.

By matching the differential impedance from the source to the receiver, signal reflections will be minimized, and the transmitted waveform *shape* (not including dispersion effects) is maintained from source to receiver. By maintaining the *shape* of the transmitted signal, the potential for signaling errors in the serial links is minimized.