PRELIMINARY

CYP15G0402DX

Quad HOTLinkII™ SERDES

Features

- **Second generation HOTLink® technology**
- **Fibre Channel and Gigabit Ethernet compliant**
- **10-bit unencoded data transport**
  - **Unencoded aggregate throughput of 12 GB/s**
- **Selectable parity check/generate**
- **Four independent 10-bit channels**
- **Selectable input clocking options**
- **User selectable framing character**
  - **+Comma, ±Comma, or Full K28.5 detect**
  - **Single or Multi-character framer for character alignment**
  - **Low-latency option**
- **Synchronous parallel input interface**
  - **User-configurable threshold level**
  - **Compatible with LVTTL, LVCMOS, LVTTL**
- **Synchronous parallel output interface**
  - **Separate or common V_{DDQ} supply for outputs**
  - **Compatible with LVTTL, LVCMOS, LVTTL**
- **200-to-1500 MBaud serial signaling rate**
- **Internal PLLs with no external PLL components**
  - **Separate clock and data recovery PLL per channel**
  - **Common transmit clock multiplier PLL**
- **Differential PECL-compatible serial inputs**
- **Differential PECL-compatible serial outputs**
  - **Source matched for 50Ω transmission lines**
  - **No external resistors required**
  - **Adjustable amplitude for 100Ω or 150Ω balanced loads**
- **Compatible with fiber-optic modules and copper cables**
- **JTAG boundary scan**
- **Built-In Self-Test (BIST) for at-speed link testing**
- **Per-channel Link Quality Indicator**
  - **Analog signal detect**
  - **Digital signal detect**
- **Low Power (2.4W typical)**
  - **+3.3V V_{CC} supply for serial, analog, and logic sections**
  - **+1.5V to +3.3V V_{DDQ} supply for parallel outputs**
- **256-ball PBGA**
- **0.25µ BiCMOS technology**

Functional Description

The CYP15G0402DX Quad HOTLinkII™ SERDES Transceiver is a point-to-point communications building block allowing the transfer of pre-encoded (or scrambled) data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at speeds ranging from 200 to 1500 MBaud per serial link.

Each transmit channel accepts pre-encoded 10-bit transmission characters in an input register, serializes each character, and drives it out a PECL-compatible differential line driver. Each receive channel accepts a serial data stream at a differential line receiver, deserializes the stream into 10-bit characters, frames these characters to the proper 10-bit character boundaries, and presents these characters to an output register along with a recovered character clock. *Figure 1* illustrates typical connections between independent systems and a CYP15G0402DX.

As a second-generation HOTLink device, the CYP15G0402DX extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial link compatibility (data and BIST) with other HOTLink devices.

The transmit section of the CYP15G0402DX Quad HOTLinkII SERDES consists of four character-wide channels that accept a new pre-encoded 10-bit transmission character on every

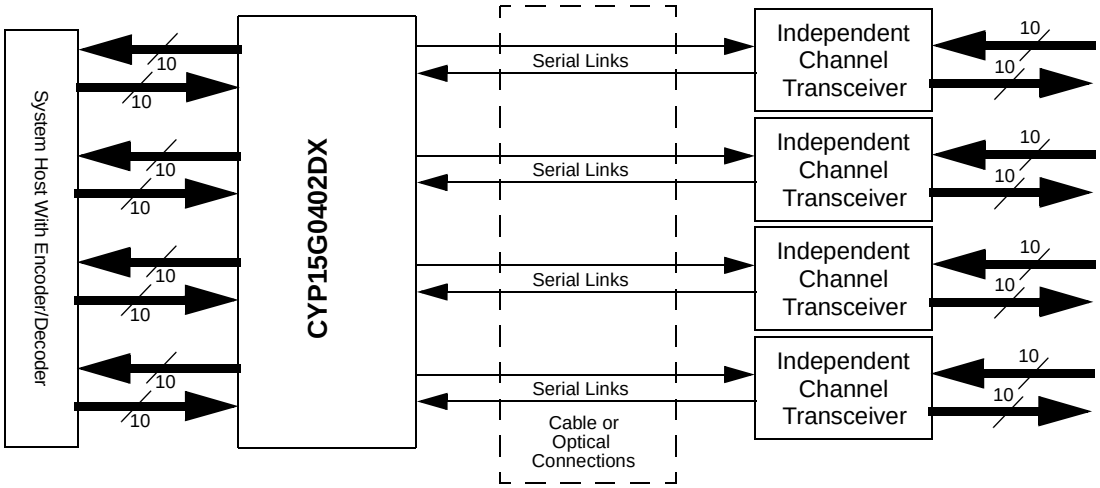


Figure 1. CYP15G0402DX HOTLink II™ System Connections.

clock cycle. Transmission characters are passed from the Transmit Input Register to a Serializer. The serialized characters are output from a Positive ECL (PECL) compatible differential transmission-line driver at a bit-rate of either 10 or 20 times the input reference clock.

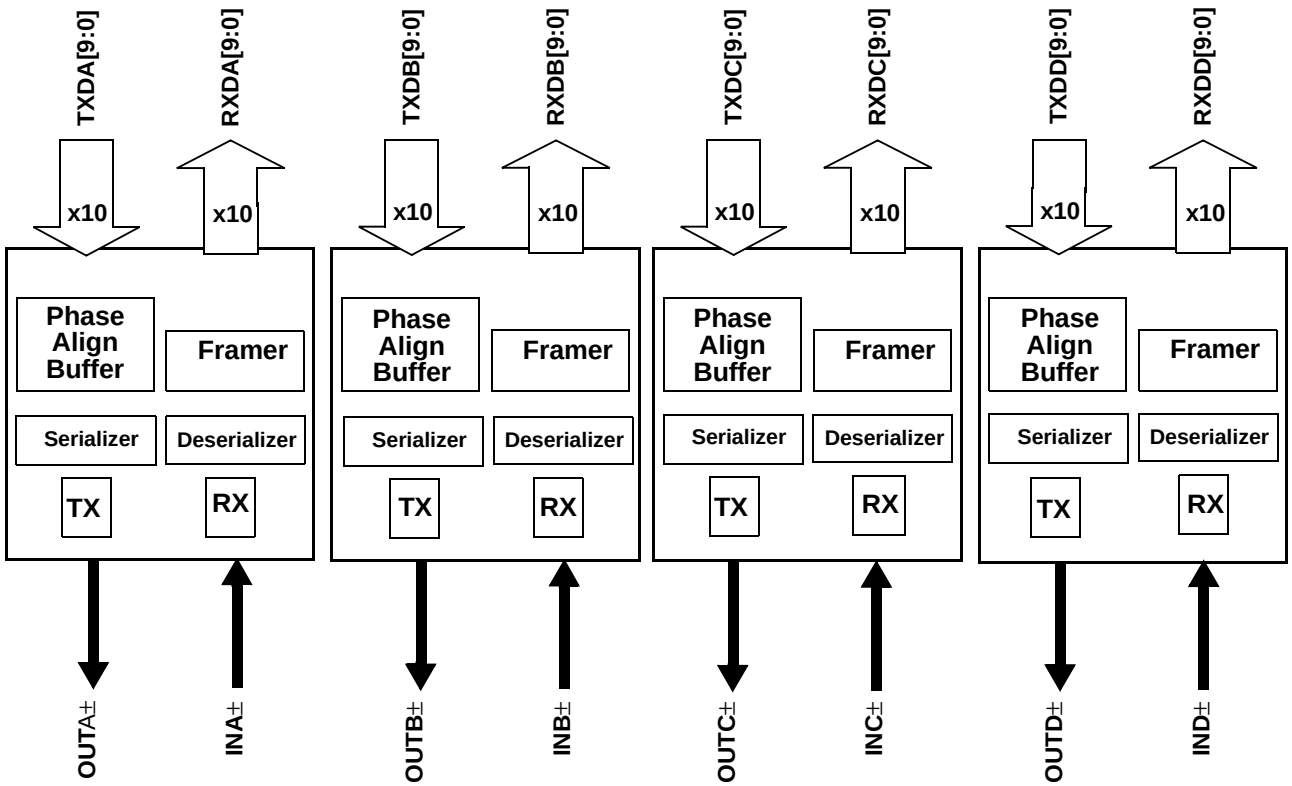
The receive section of the CYP15G0402DX Quad HOTLink II SERDES consists of four character-wide channels. Each channel accepts a serial bit-stream from a PECL-compatible differential line receiver and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. Each recovered bit-stream is deserialized and framed into characters. Recovered characters are then passed to the receiver output register, along with a recovered character clock.

The LVTTL parallel input interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. The receive output interface may be configured to present data relative to a character-rate or half character-rate recovered clock. Both true and complement recovered-clock outputs are available.

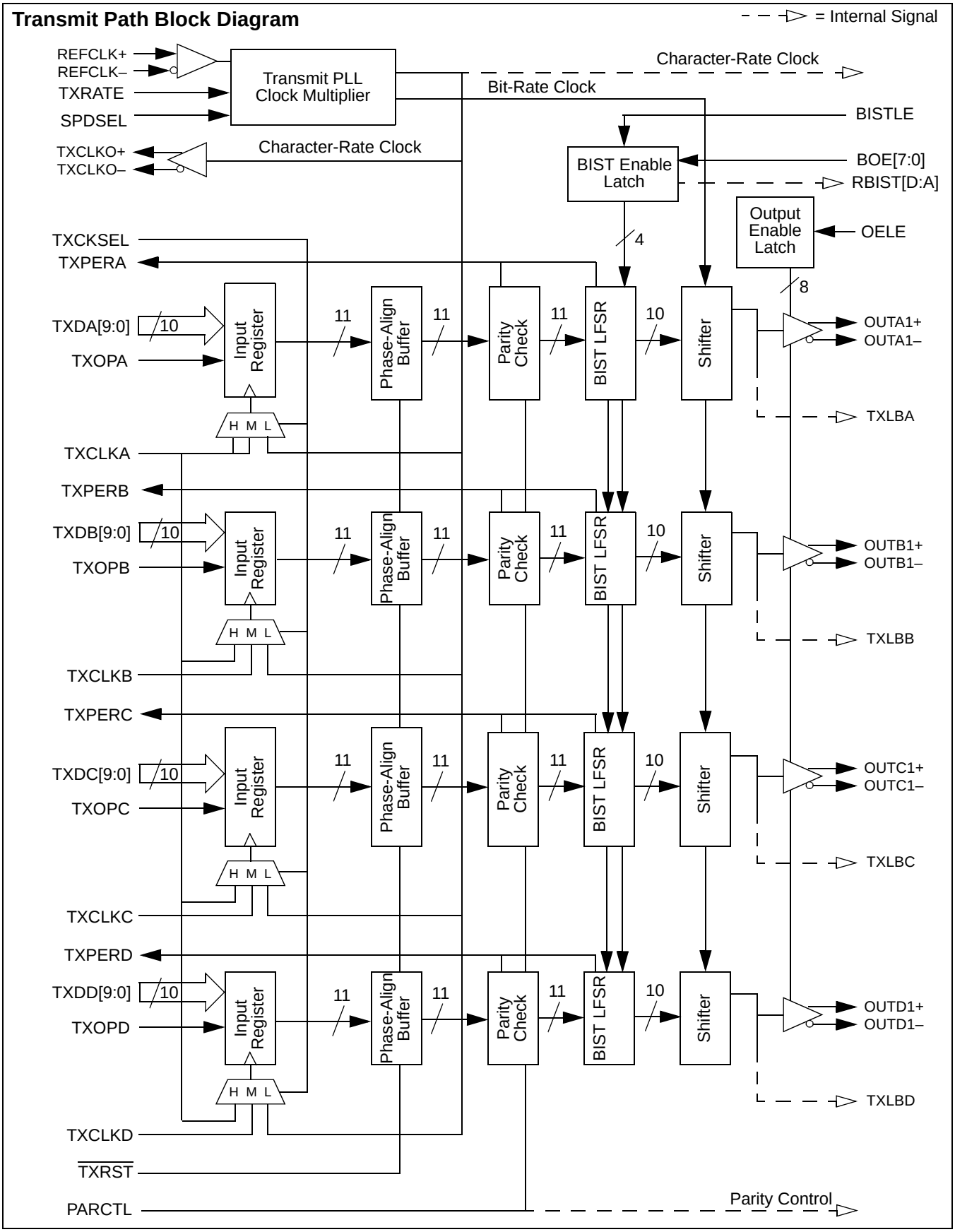
Each transmit and receive channel contains independent Built-In Self-Test (BIST) pattern generators and checkers. This BIST hardware allows at-speed testing of the high-speed serial data paths in each channel, and across the interconnecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting workstations, servers, mass storage, and video transmission equipment.

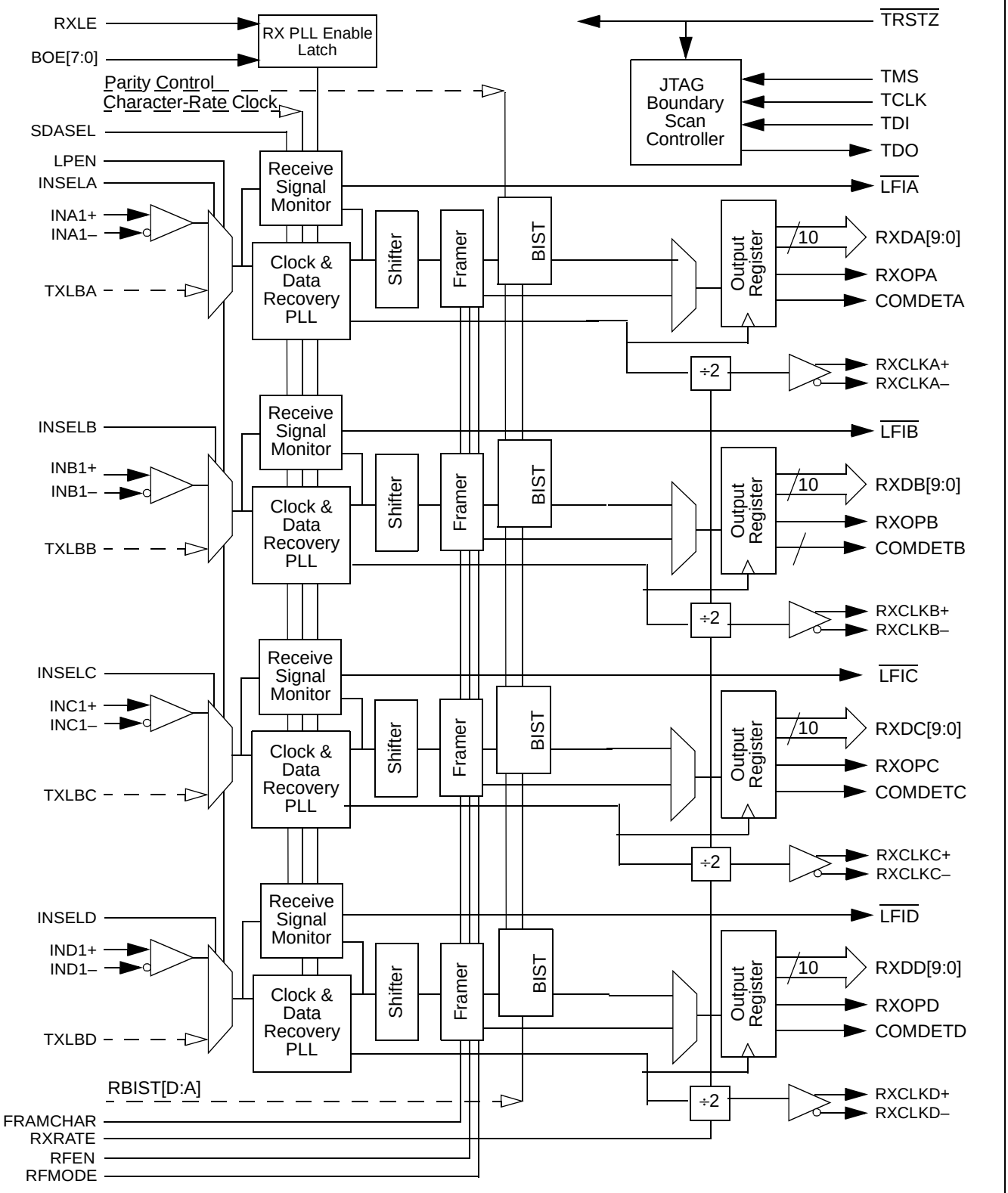
CYP15G0402DX Transceiver Logic Block Diagram



Transmit Path Block Diagram



Receive Path Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	INC-	OUTC -	N/C	N/C	**V_{CC}**	IND-	OUTD -	**GND**	N/C	N/C	INA-	OUTA -	**GND**	N/C	N/C	**V_{CC}**	INB-	OUTB -	N/C	N/C
B	INC+	OUTC +	N/C	N/C	**V_{CC}**	IND+	OUTD +	**GND**	N/C	N/C	INA+	OUTA +	**GND**	N/C	N/C	**V_{CC}**	INB+	OUTB +	N/C	N/C
C	TDI	TMS	LP ENC	LP ENB	**V_{CC}**	PAR CTL	SDA-SEL	**GND**	BOE[7]	BOE[5]	BOE [3]	BOE [1	**GND**	**GND**	**GND**	**V_{CC}**	TX RATE	RX RATE	N/C	TDO
D	TCLK	$\overline{\text{TRSTZ}}$	LP END	LP ENA	**V_{CC}**	RF MODE	SPD SEL	**GND**	BOE[6]	BOE[4]	BOE [2]	BOE [0]	**GND**	**GND**	**GND**	**V_{CC}**	N/C	RXLE	N/C	N/C
E	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
F	TX PERC	TX OPC	TXDC [0]	N/C													BIS-TLE	RXDB [0]	RX-OPB	RXDB [1]
G	TXDC [7]	TXCK SEL	TXDC [4]	TXDC [1]													**GND**	OELE	FRAM CHAR]	RXDB [3]
H	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
J	TXDC [9]	TXDC [5]	TXDC [2}	TXDC [3]													COM-DETB	RXDB [2]	RXDB [7]	RXDB [4]
K	RXDC [4]	RX CLKC -	TXDC [8]	$\overline{\text{LFIC}}$													RXDB [5]	RX DB[6]	RXDB [9]	RX CLK B+
L	RXDC [5]	RX CLKC +	TXCLK C	TXDC [6]													RXDB [8]	$\overline{\text{LFIB}}$	RX-CLK B-	TXDB [6]
M	RXDC [6]	RXDC [7]	RXDC [9]	RXDC [8]													TXDB [9]	TXDB [8]	TX DB[7]	TX CLKB
N	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
P	RXDC [3]	RXDC [2]	RXDC [1]	RXDC [0]													TXDB [5]	TXDB [4]	TX DB[3]	TX DB[2]
R	COM DETC	RX OPC	TX PERD	TX OPD													TXDB [1]	TXDB [0]	TX OPB	TX PERB
T	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
U	TXDD [0]	TXDD [1]	TXDD [2]	TXDD [9]	**V_{CC}**	RXDD [4]	RXDD [3]	**GND**	RX OPD	RF ENC	REF-CLK -	TXDA [1]	**GND**	TXDA [4]	TXDA [8]	**V_{CC}**	RXDA [4]	RX OPA	COM DETA	RX DA[0]
V	TXDD [3]	TXDD [4]	TXDD [8]	RX DD[8]	**V_{CC}**	RXDD [5]	RXDD [1]	**GND**	COM DETD	RF END	REF-CLK +	RFEN B	**GND**	TXDA [3]	TXDA [7]	**V_{CC}**	RXDA [9]	RX DA[5]	RX DA[2]	RX DA[1]
W	TXDD [5]	TXDD [7]	$\overline{\text{LFID}}$	RX CLK D–	**V_{CC}**	RXDD [6]	RXDD [0]	**GND**	TX CLK O–	$\overline{\text{TX}}$ $\overline{\text{RST}}$	TX OPA	RFEN A	**GND**	TXDA [2]	TXDA [6]	**V_{CC}**	$\overline{\text{LFIA}}$	RX CLK A–	RX DA[6]	RX DA[3]
Y	TX DD[6]	TX CLKD	RXDD [9]	RX CLK D+	**V_{CC}**	RXDD [7]	RXDD [2]	**GND**	TX CLK O+	N/C	TX CLKA	TX PERA	**GND**	TXDA [0]	TXDA [5]	**V_{CC}**	TXDA [9]	RX CLK A+	RX DA[8]	RX DA[7]

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +4.2V

DC Voltage Applied to LVTTL Outputs in High-Z State..... –0.5V to V_{DDQ}+0.5V

Output Current into LVTTL Outputs (LOW).....30 mA

DC Input Voltage ..... –0.5V to V_{CC}+0.5V

Static Discharge Voltage.....> 2001 V (per MIL-STD-883, Method 3015)

Latch-Up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 10%	1.5V to V_{CC}
Industrial	–40°C to +85°C	3.3V ± 10%	1.5V to V_{CC}

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPERA TXPERB TXPERC TXPERD	LVTTL Output, changes following TXCLKO↑	Transmit Path Parity Error. Active HIGH. Asserted (HIGH) if parity checking is enabled and a parity error is detected at the Shifter. This output is HIGH for one TXCLKO± clock period to indicate detection of a parity error in the character presented to the shifter. If a parity error is detected, the character in error is replaced with a +C0.7 character to force a corresponding bad character detection at the remote end of the link. This replacement takes place only when parity checking is enabled (PARCTL ≠ LOW). When BIST is enabled for a specific transmit channel, BIST progress is presented on the associated TXPERx output. Once every 511 character times, TXPERx pulses HIGH for one TXCLKO± period to indicate a complete pass through the BIST sequence. When the transmit Phase Align Buffers are enabled (TXCKSEL ≠ LOW), if an underflow or overflow condition is detected, TXPERx for the channel in error is asserted and remains asserted until the Phase Align Buffers are reset ($\overline{\text{TXRST}}$ is sampled LOW).
TXDA[9:0] TXDB[9:0] TXDC[9:0] TXDD[9:0]	LVTTL Input, synchronous, sampled by the respective TXCLKx↑ or TXCLKO↑	Transmit Data Inputs. These inputs are captured on the rising edge of the transmit interface clock (selected by TXCKSEL) and passed to the transmit shifter. TXDx[9:0] specify the specific transmission character to be sent.
TXOPA TXOPB TXOPC TXOPD	LVTTL Input, synchronous, sampled by the respective TXCLKx↑ or TXCLKO↑	Transmit Path Odd Parity. When parity checking is enabled (PARCTL ≠ LOW), the ODD parity captured at these inputs is XORed with the bits on the associated TXDx bus to verify the integrity of the captured character.
Transmit Path Clock and Control		
TXCLKO±	LVTTL Output	Transmit Clock Output. This true and complement clock is synthesized by the transmit PLL and is synchronous to the internal transmit character clock. It operates at either the same frequency as REFCLK, or at twice the frequency of REFCLK (as selected by TXRATE). TXCLKO± is always equal to the VCO bit-clock frequency ÷10. The TXCLKO+ output rising edges and TXCLKO– falling edges are phase aligned to the rising edges of the REFCLK input.
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous	Transmit Clock Phase Reset, active LOW. When LOW, the transmit Phase Align Buffers are allowed to adjust their data transfer timing (relative to the selected input clock) to allow clean transfer of data from the Input Register to the transmit shifter. When $\overline{\text{TXRST}}$ is deasserted (HIGH), the internal phase relationship between the selected TXCLKx and the internal character-rate clock is fixed and the device operates normally. During this reset alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit elasticity buffers are adjusted.

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
TXCKSEL	3-Level Select[1] Static Control Input	Transmit Clock Select. Selects the transmit clock source, used to write data into the transmit Input Register, for the transmit channel(s). When LOW, all four input registers are clocked by the internal TXCLKO↑ derivative of REFCLK. When MID (open), TXCLKx↑ is used as the input register clock for the associated TXDx[9:0] and TXOPx. When HIGH, TXCLKA↑ is used to clock data into the input register for all channels.
TXRATE	LVTTL Input, asynchronous, internal pull-up	Transmit PLL Clock Rate Select. When TXRATE is HIGH, the Transmit PLL multiplies REFCLK by 10 to generate the serial bit-rate clock. When TXRATE is LOW, the transmit PLL multiples REFCLK by 20 to generate the serial bit-rate clock. See *Table 3* for a list of operating REFCLK and serial rates.
TXCLKA TXCLKB TXCLKC TXCLKD	LVTTL Clock Input	Transmit Path Input Clocks. These clocks are frequency coherent to TXCLKO±, but may be offset in phase. Internal operating phase relative to REFLCK is adjusted when $\overline{\text{TXRST}}$ is LOW and locked in when $\overline{\text{TXRST}}$ is HIGH. These inputs are only used when TXCKSEL ≠ LOW.
	LVTTL input, asynchronous, internal pull-up	
Receive Path Data Signals		
RXDA[9:0] RXDB[9:0] RXDC[9:0] RXDD[9:0]	LVTTL Output, synchronous	Receive Data Output. These outputs change following the rising edge of the associated RXCLKx± clock.
COMDETA COMDETB COMDETC COMDETD	LVTTL Output, synchronous	Frame Character Detected. The character in the output register matches that of the selected framing character.
RXOPA RXOPB RXOPC RXOPD	3-State, LVTTL Output	Receive Path Odd Parity. When parity generation is enabled (PARCTL ≠ LOW), the parity output at these pins is valid for the data on the associated RXDx bus bits. When parity generation is disabled (PARCTL = LOW) these output drivers are disabled (High-Z).
RXRATE	LVTTL Input Static Control Input	Receive Clock Rate Select. When LOW, the RXCLKx± clock outputs are complementary clocks operating at half the character rate. Data should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–. When HIGH, the RXCLKx± clock outputs are complementary clocks operating at the recovered character rate. Data should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–.
FRAMCHAR	3-Level Select[1] Static Control Input	Framing Character Select. Used to control the character or portion of a character used for character framing of the received data streams. When LOW, the framer looks for an 8-bit positive COMMA character in the data stream. When MID (open), the framer looks for both positive and negative disparity versions of the 8-bit COMMA character. When HIGH, the framer looks for both positive and negative disparity versions of the K28.5 character.

Note:

1. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
RFMODE	3-Level Select[1] Static Control Input	Reframe Mode Select. Used to control the type of character framing used to adjust the character framing boundaries based on detection of one or more framing characters in the data stream. This signal operates in conjunction with the presently enabled channel bonding mode, and the type of framing character selected. When LOW, the low-latency framer is selected. This will frame on the first occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered clock for one or multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode multi-byte parallel framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phasing regardless of character offset. When HIGH, the alternate mode multi-byte parallel framer is selected. This requires detection of the selected framing character(s) of the allowed disparities in the received data stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phasing regardless of character offset.
VREF	Analog	Logic threshold reference for parallel inputs. Internally biased to $V_{DDQ}/2$. May be adjusted to other reference levels (using external resistors or voltage sources) to accommodate alternate logic types.
Receive Path Clock and Clock Control		
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	3-State, LVTTL Output clock Static control input	Receive Character Clock. These true and complement clocks are the Receive interface clocks which are used to control timing of data output transfers. These clocks are output continuously at either the dual-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATE.
RFENA RFENB RFENC RFEND	LVTTL Input, asynchronous, internal pull-down	Reframe Enable. Active HIGH. When HIGH the framer for the associated channel is enabled to frame per the presently enabled framing mode and selected framing character.
Device Control Signals		
PARCTL	3-Level Select[1], Static Control Input	Parity Check/Generate Control. Used to control the different parity check and generate functions. When LOW, parity checking and generation are disabled, and the RXOPx output drivers are disabled (High-Z). When MID (open), the TXDx[9:0] inputs are checked, along with TXOPx, for valid ODD parity, and valid ODD parity is generated for the RXDx[9:0] outputs and presented on RXOPx. When HIGH, the TXDx[9:0] inputs are checked, along with TXOPx, for valid ODD parity. Valid ODD parity is generated for the RXDx[9:0] and COMDETx outputs and presented on RXOPx.
REFCLK±	Differential LVPECL or single-ended LVCMOS input clock	Reference Clock. This clock input is used as the timing reference for the transmit and receive PLLs. A derivative of this input clock may also be selected to clock the transmit input registers. For an LVCMOS input clock, connect REFCLK+ to the reference clock and leave REFCLK– open. For an LVPECL differential clock, both inputs must be connected. When TXCKSEL is LOW, a character-rate derivative of REFCLK is used as the clock for the parallel transmit data (input) interface.
SPDSEL	3-Level Select[1], Static Control Input	Serial Rate Select. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 200–400 MBaud, MID (open) = 400–800 MBaud, HIGH = 800–1500 MBaud.

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
Analog I/O and Control		
OUTA± OUTB± OUTC± OUTD±	CML Differential Output	Differential Serial Data Outputs. These CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
INA± INB± INC± IND±	LVPECL Differential Input	Differential Serial Data Inputs. These inputs accept the serial data stream for deserialization and decoding. The INx± serial stream is fed to the receiver to extract the data and clock content when LPENx is LOW.
CARADJ	3-Level Select[1], static configuration input	Signal Detect Amplitude Level Select. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in *Table 4*.
LPENA LPENB LPENC LPEND	LVTTL Input, asynchronous, internal pull-down	Loop-Back-Enable. Active HIGH. When asserted (HIGH), the transmit serial data from the associated channel is internally routed to its respective receiver clock and data recovery (CDR) circuit. The serial driver for the channel where LPENx is active is forced to differential logic-1, and serial data inputs for that channel are ignored.
OELE	LVTTL Input, asynchronous, internal pull-up	Serial Driver Output Enable Latch Enable. Active HIGH. When OELE = HIGH, the signals on the BOE[7:0] inputs directly control the OUTx± differential drivers. When the BOE[x] input is HIGH, the associated OUTx± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTx± differential driver is powered down. When OELE returns LOW, the last values present on BOE[7:0] are captured in the internal Output Enable latch. The specific mapping of BOE[7:0] signals to transmit output enables is listed in *Table 2*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to enable all outputs.
BISTLE	LVTTL Input, asynchronous, internal pull-up	Transmit and Receive BIST Latch Enable. Active HIGH. When BISTLE = HIGH, the signals on the BOE[7:0] inputs directly control the transmit and receive BIST enables. When BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data transmission or reception. When BISTLE returns LOW, the last values present on BOE[7:0] are captured in the internal BIST Enable latch. The specific mapping of BOE[7:0] signals to transmit and receive BIST enables is listed in *Table 2*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on all transmit and receive channels.
RXLE	LVTTL Input, asynchronous, internal pull-up	Receive Channel Power-Control Latch Enable. Active HIGH. When RXLE = HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the receive PLLs and analog logic. When the BOE[7:0] input is HIGH, the associated receive channel A through receive channel D PLL and analog logic are active. When the BOE[7:0] input is LOW, the associated receive channel A through receive channel D PLL and analog logic are placed in a non-functional power saving mode. When RXLE returns LOW, the last values present on BOE[7:0] are captured in the internal RX PLL Enable latch. The specific mapping of BOE[7:0] signals to the associated receive channel enables is listed in *Table 2*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to enable all receive channels.

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
BOE[7:0]	LVTTL Input, asynchronous, internal pull-up	BIST, Serial Output, and Receive Channel Enables. These inputs are passed to and through the output enable latch when OELE is HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST enable latch when BISTLE is HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel enable latch when RXLE is HIGH, and captured in this latch when RXLE returns LOW.
$\overline{\text{LFIA}}$ $\overline{\text{LFIB}}$ $\overline{\text{LFIC}}$ $\overline{\text{LFID}}$	LVTTL Output, changes following RXCLKx↑	Link Fault Indication Output. Active LOW. LFI* is the logical OR of three internal conditions on the associated channel: 1. Received serial data frequency outside expected range 2. Analog amplitude below expected levels 3. Transition density lower than expected
JTAG Interface		
TMS	LVCMOS Input, internal pull-up	Test Mode Select. Enables JTAG Test Mode.
TCLK	LVCMOS Input, internal pull-down	JTAG Test Clock
TDO	3-State LVCMOS Output	Test Data Out. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVCMOS Input, internal pull-up	Test Data In. JTAG data input port.
$\overline{\text{TRSTZ}}$	LVCMOS Input, internal pull-up	Test Reset. JTAG and full chip reset. Active LOW. Initializes the JTAG controller and all other state machines.
Power		
V_{CC}		+3.3V Power for Serial Outputs, Analog, Logic circuits, and all IO's.
GND		Signal and Power Ground for all internal circuits.

CYP15G0402DX HOTLink II SERDES Operation

The CYP15G0402DX is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links, from one or multiple sources to multiple destinations. This device contains four character-wide channels.

CYP15G0402DX Transmit Data Path

Data Path

The transmit path of the CYP15G0402DX supports four character-wide data paths. These data paths are unencoded and require pre-encoded or scrambled data for reliable transport of information.

Input Register

The bits in the Input Register for each channel have fixed bit assignments, as listed in *Table 1*

Table 1. Input Register Bit Mapping

Signal Name	Bus Weight	10B Name
TXDx[0] (LSB)	2^0	a[2]
TXDx[1]	2^1	b
TXDx[2]	2^2	c
TXDx[3]	2^3	d
TXDx[4]	2^4	e
TXDx[5]	2^5	i
TXDx[6]	2^6	f
TXDx[7]	2^7	g
TXDx[8]	2^8	h
TXDx[9] (MSB)	2^9	j
TXOPx[3]		

Each input register captures a minimum of 10 bits on each input clock cycle. When parity checking is enabled, the TXOPx parity input is also captured in the associated input register.

Input Register Clocking

The transmit Input Registers can be configured to accept data relative to a number of different clock sources. The selection of the clock source is controlled by TXCKSEL.

When TXCKSEL is LOW, the transmit Input Registers capture data synchronous to the TXCLKO± derivative of REFCLK. When TXCKSEL is MID (open), the rising edge of TXCLKx is used to capture the data at the associated TXDx[9:0] and TXOPx inputs. When TXCKSEL is HIGH, the rising edge of TXCLKA is used to capture the data at the associated TXDx[9:0] and TXOPx inputs on all four channels.

Phase-Align Buffer

Data from the Input Registers are passed to the associated Phase-Align Buffer. When the transmit Input Registers are configured to capture data synchronous to REFCLK (TXCKSEL = LOW), the Phase-Align Buffers are bypassed and data is passed directly to the parity check and serializer blocks (to reduce latency).

When the Input Registers are clocked with an uncontrolled phase relationship to REFCLK (TXCKSEL ≠ LOW), the Phase-Align Buffers are enabled. These buffers are used to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of these Phase-Align Buffers takes place when the $\overline{\text{TXRST}}$ input is asserted LOW. When $\overline{\text{TXRST}}$ is returned HIGH, the present input clock phase relative to REFCLK is set.

Once set, the input clocks are allowed to skew in time up to half a character period in either direction relative to REFCLK; i.e., ±180°. This time-shift allows the delay paths of the character clocks (relative to REFLCK) to change due to operating voltage and temperature, while not affecting the design operation. $\overline{\text{TXRST}}$ is an asynchronous input.

Parity Support

In addition to the ten data and control bits that are captured at each channel, a TXOPx input is also available on each channel. This allows the CYP15G0402DX to support ODD parity checking for each channel. When PARCTL is LOW, parity checking is disabled. When PARCTL is MID (open) or HIGH, parity is checked on the TXDx[9:0] and TXOPx bits.

If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character in error is replaced with the 1001111000 pattern (an invalid character) regardless of the running disparity of the previous character.

Transmit BIST

The transmitter interfaces contain internal pattern generators that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in *Table 2* (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Receiver(s).

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator in the associated transmit channel (or the BIST checker in the associated receive channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned high to open the latch again. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a a device reset ($\overline{\text{TRSTZ}}$ is sampled LOW).

All data and data-control information present at the associated TXDx[7:0] and TXCTx[1:0] inputs are ignored when BIST is active on that channel. If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and management of clock-frequency variations.

Serial Output Drivers

The serial interface Output Drivers make use of high-performance differential CML (Current Mode Logic) to provide a source-matched driver for the transmission lines. These drivers accept data from the Transmit Shifters. These outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or AC-coupled transmission lines.

When configured for local loopback (LPEN = HIGH), the output drivers for all enabled ports are configured to drive a static differential logic-1.

Each output can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the OELE latch-enable signal. When OELE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Serial Output Enable latch to control the serial output drivers. The BOE[7:0] input associated with a specific OUTx± driver is listed in *Table 2*.

Notes:
2. LSB is shifted out first.
3. The TXOPx inputs are also captured in the associated input register, but their interpretation is under the separate control of PARCTL.

Table 2. Output Enable, BIST, and Receive Channel Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[7]	X	Transmit D	X
BOE[6]	OUTD±	Receive D	Receive D
BOE[5]	X	Transmit C	X
BOE[4]	OUTC±	Receive C	Receive C
BOE[3]	X	Transmit B	X
BOE[2]	OUTB±	Receive B	Receive B
BOE[1]	X	Transmit A	X
BOE[0]	OUTA±	Receive A	Receive A

When OELE is HIGH and BOE[x] is HIGH, the associated serial driver is enabled to drive any attached transmission line When OELE is HIGH and BOE[x] is LOW, the associated driver is disabled and internally configured for minimum power dissipation. If both outputs for a channel are in this disabled state, the associated internal logic for that channel is also configured for lowest power operation. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to opened the latch again.

Note: When a disabled transmit channel (i.e., both outputs disabled) is re-enabled, the data on the serial outputs may not meet all timing specifications for up to 10 ms.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiplies that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the transmit Shifter.

The clock multiplier PLL can accept a REFCLK input between 10 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP15G0402DX clock multiplier (controlled by the TXRATE input) and by the signal level on the SPDSEL input.

SPDSEL is a 3-level select[1] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signalling rate and allowable range of REFCLK frequencies is listed in *Table 3*.

Table 3. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	0	10–20	200–400
	1	20–40	
MID (Open)	0	20–40	400–800
	1	40–80	
HIGH	0	40–75	800–1500
	1	80–150	

The REFCLK± input is a non-standard input. Internally it is a differential input with each input internally biased to 1.5V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a LVPECL clock that is DC- or AC-coupled, or a differential LVTTL or LVCMOS clock.

CYP15G0402DX Receive Data Path

Serial Line Receivers

A high-sensitivity differential line receiver, INx±, is available on each channel for accepting a serial bit stream. The serial line receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB ($V_{DIF} \geq$ 100 mV, or 200 mV peak-to-peak differential) or can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL logic family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages.

The local loopback input (LPENx) for each channel allows the serial transmit data for the associated channel to be routed internally back to the clock and data recovery circuit associated with that channel. When a channel is configured for local loopback, the associated transmit serial driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers or optical drivers.

Receive Channel Enabled

The CYP15G0402DX contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the RXLE latch-enable signal. When RXLE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Receive Channel Enable latch to control the PLLs and logic of the associated receive channel. The BOE[7:0] input associated with a specific receive channel is listed in *Table 2*.

When RXLE is HIGH and BOE[x] is HIGH, the associated receive channel enabled to receive and decode a serial stream from the selected line receiver. When RXLE is HIGH and BOE[x] is LOW, the associated receive channel is disabled and internally configured for minimum power dissipation.

Signal Detect

Each Line Receiver is simultaneously monitored for:

- analog amplitude
- transition density
- received data stream outside normal frequency range (±200 ppm)

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFIx (Link Fault Indicator) output associated with each receive channel. These LFIx outputs change synchronous to the receive interface recovered clock (RXCLKx±).

While the majority of these signal monitors are based on fixed constants, the analog amplitude level detection is adjustable

to allow operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the CARADJ signal, a 3-level select[1] (ternary) input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 4*. This input effects the analog monitors for all receive channels.

Table 4. Analog Amplitude Detect Valid Signal Levels

CARADJ	Typical Signal with Peak Amplitudes Above
LOW	140 mV p-p differential
MID (Open)	280 mV p-p differential
HIGH	420 mV p-p differential

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate Clock/Data Recovery (CDR) block within each channel. The clock extraction function is performed by high-performance embedded phase-locked loops (PLL) that track the frequency of the incoming bit streams and align the phase of their internal bit-rate clocks to the transitions in the selected serial data streams.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) reference clock on the REFCLK± input. This REFCLK± input is used to ensure that the VCO (within each CDR) is operating at the correct frequency (rather than some harmonic of the bit-rate), to improve PLL acquisition time, and to limit unlocked frequency excursions of the CDR VCO when no data is present at the serial inputs.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits set by the integrated range controls, the CDR PLL will track REFCLK instead of the data stream. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK is required to be within ±200 ppm of the frequency of the clock that drives the REFCLK signal of the *remote* transmitter to ensure a lock to the incoming data stream.

Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for one or more COMMA or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

Framing Character

The CYP15G0402DX allows selection of one of three combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

FRAMCHAR is a 3-level select [1] input that allows selection of one of three different characters or character combinations. These combinations are listed in *Table 5*.

Framer

The framer on each channel operates in one of three different modes, as selected by the RFMODE input. When RFMODE is

Table 5. Framing Character Selector

FRAMCHAR	Bits Detected in Framer	
	Character Name	Bits Detected
LOW	+COMMA	00111110XX
MID (Open)	+COMMA –COMMA	00111110XX or 11000001XX
HIGH	+K28.5 –K28.5	0011111010 or 1100000101

LOW, the low-latency framer is selected. This framer operates by stretching the recovered character clock until it aligns with the character boundaries. In this mode the framer aligns on the first detection of the selected framing character.

When RFMODE is MID (open) the Cypress-mode multi-character framer is selected. The detection of multiple framing characters makes the associated link much more robust to incorrect framing due to aliased SYNC characters in the data stream. In this mode the framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock will not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODE is HIGH, the alternate-mode multi-character framer is enabled. Like Cypress-mode multi-character framing, multiple framing characters must be detected to adjust the character boundaries. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, before character framing is adjusted.

> **NOTE:** The 8B/10B running disparity rules prohibit the presence of multiple +COMMA characters as consecutive characters, except for the K28.7 comma character. Because of this, the combination of FRAMCHAR LOW and RFMODE HIGH is not recommended. While framing can still take place while following all 8B/10B coding rules, this configuration prevents framing to the normal K28.5 character.

Framing is enabled for a channel when the associated RFENx input is HIGH. When RFENx is LOW, the framer for the associated channel is disabled. When a framer is disabled, no changes are made to the recovered character boundaries on that channel, regardless of the presence of framing characters in the data stream.

BIST LFSR

The output register of each Framer is normally used to pass received characters to the associated output register. When configured for BIST mode, this register becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). When enabled, this LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received

Table 6. BIST Status Bits

Status			Priority	Description
COMDETx	RXDx[0]	RXDx[1]		BIST Mode (RXBISTEN is LOW)
0	0	0	7	**BIST Data Compare.** Data Character compared correctly.
0	0	1	7	**BIST Command Compare.** Command Character compared correctly.
0	1	0	2	**BIST Last Good.** Last Character of BIST sequence detected and valid.
0	1	1	5	Reserved
1	0	0	4	**BIST Last Bad.** Last Character of BIST sequence was detected invalid.
1	0	1	1	**BIST Start.** RXBISTEN recognized on this channel, but character compares have not yet commenced. Also presented when the receive PLL is tracking REFCLK instead of the selected data stream.
1	1	0	6	**BIST Error.** While comparing characters, a mismatch was found in one or more of the decoded character bits.
1	1	1	3	**BIST Wait.** The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

data stream, the associated receiver checks each character received with each character generated by the LFSR and indicates compare errors and BIST status at the RXDx[2:0] bits of the output register.

These generators are enabled by the associated BOE[x] signals listed in *Table 2* (when the BISTLE latch enable input is HIGH).When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator/checker in the associated receive channel (or the BIST generator in the associated transmit channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch.These values remain in the BIST Enable Latch until BISTLE is returned high to open the latch again. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a device reset ($\overline{\text{TRSTZ}}$ is sampled LOW).

The LFSR is initialized by the BIST hardware once the external enable (RXBISTENx) is recognized. This sets the BIST LFSR to the BIST-loop start-code of D0.0 (D0.0 is sent only once per BIST loop). The status of the BIST progress and any character mismatches is presented on the RXDx[2:0] outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXDx[2:0] indicates 01X for one RXCLK cycle per BIST loop to indicate loop completion. This can be used to check test pattern progress.

The specific patterns checked by each receiver are described in detail in the Cypress application note “HOTLink Built-In Self-Test.” The sequence compared by the CYP15G0402DX is identical to that in the CY7B933 and CY7C924, allowing interoperable systems to be built when used at compatible serial signalling rates.

If a large number of errors are detected, the receive BIST state machine aborts the compare operations and resets the LFSR to look for the start of the BIST sequence again.

Output Bus

Each receive channel presents a 12-signal output bus consisting of:

- a 10-bit data bus
- a COMMA detect indicator
- a parity bit

The signals present on this output bus are shown in *Table 7*.

Table 7. Output Register Bit Assignments

Signal Name	Bus Weight	10B Name
RXOPx[4]		
COMDET[4]		
RXDx[0] (LSB)	2^0	a[5]
RXDx[1]	2^1	b
RXDx[2]	2^2	c
RXDx[3]	2^3	d
RXDx[4]	2^4	e
RXDx[5]	2^5	i
RXDx[6]	2^6	f
RXDx[7]	2^7	g
RXDx[8]	2^8	h
RXDx[9] (MSB)	2^9	j

The framed 10-bit value is presented to the associated Output Register, along with a status output indicating if the character in the output register matches the selected framing characters.

The COMDETx status outputs operate the same regardless of the bit combination selected for character framing by the FRAMCHAR input. COMDETx is HIGH when the character in the output register of the associated channel contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the low-latency framer and half-rate receive port clocking are also enabled (RFMODE and RXRATE are both LOW), the framer will stretch the recovered clock to the next 20-bit boundary such that the rising edge of RXCLKx+ occurs when COMDET is present on the associated output bus.

When the standard framer is enabled and half-rate receive port clocking is also enabled (RFMODE is MID or HIGH and RXRATE is LOW), the output clock is not modified, but a single pipeline stage may be added or subtracted from the data stream by the framer logic such that the rising edge of RXCLKx+ occurs when COMDET is present on the associated output bus.

Notes:

4. The RXOPx and COMDETx outputs are also driven from the associated output register, but their generation and interpretation are separate from the data bus.
5. LSB is shifted in first

This adjustment only occurs when the framer for that channel is enabled (RFENx is HIGH). When the framer is disabled, the clock boundaries are not adjusted, and COMDETx may be active during the rising edge of RXCLKx– (if an odd number of characters were received following the initial framing).

Parity Generation

In addition to the 10 data and COMDETx status bit that are output on each channel, an RXOPx output is also available on that channel. This allows the CYP15G0402DX to support ODD parity generation for each channel. To handle a wide range of system environments, the CYP15G0402DX supports two different forms of parity generation (in addition to no parity):

- parity on the RXDx[9:0] character
- parity on the RXDx[9:0] character and COMDETx status

These modes differ in the number bits which are included in the parity calculation. For all cases, only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in *Table 8*.

Parity generation is enabled through the 3-level select PARCTL input. When PARCTL is LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z).

When PARCTL is MID (open), ODD parity is generated for the RXDx[9:0] bits.

When PARCTL is HIGH, ODD parity is generated for both the RXDx[9:0] bits and the associated COMDETx signal.

Table 8. Output Register Parity Generation

Signal Name	Receive Parity Generate Mode (PARCTL)		
	LOW[6]	MID	HIGH
COMDETx			X[7]
RXDx[0]		X	X
RXDx[1]		X	X
RXDx[2]		X	X
RXDx[3]		X	X
RXDx[4]		X	X
RXDx[5]		X	X
RXDx[6]		X	X
RXDx[7]		X	X
RXDx[8]		X	X
RXDx[9]		X	X

JTAG Support

The CYP15G0402DX contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs and outputs and REFCLK. The high-speed serial inputs are not part of the JTAG test chain.

JTAG ID

The JTAG device ID for the CYP15G0402DX is ‘0C801069’x.

3-Level Select Inputs

Each 3-Level select input reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11 respectively.

Notes:

6. Receive path parity output drivers (RXOPx) are disabled (High-Z) when PARCTL is LOW.
7. When BIST is not enabled (RXBISTEN is HIGH), COMDETx is usually driven to a logic-0, but will be driven HIGH when the character in the output buffer is the selected framing character.

CYP15G0402DX DC Electrical Characteristics Over the Operating Range

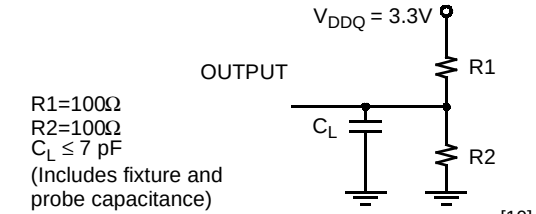
Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL Compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –4 mA, V_{DDQ} = Min.	V_{DDQ}–0.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{DDQ} = Min.		0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[8]	–30	–100	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
LVTTL Compatible Inputs					
V_{IHT}	Input HIGH Voltage		VREF+0.1	V_{DDQ}+0.3	V
V_{ILT}	Input LOW Voltage		–0.5	VREF–0.1	V
I_{IHT}	Input HIGH Current	REFCLK Input, V_{IN} = V_{CC}		+500	µA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	REFCLK Input, V_{IN} = 0.0V		–500	µA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLK±					
V_{DIFF}	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.0	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		GND	V_{CC}–0.4V	V
V_{COM}	Common Mode Range		0.8	V_{CC}	V
3-Level Inputs					
V_{IHH}	Three-Level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-Level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID Current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW Current	V_{IN} = GND		–200	µA
Differential CML Serial Outputs: OUTA±, OUTB±, OUTC±, OUTD±					
V_{OHC}	Output HIGH Voltage (V_{CC} referenced)	100Ω differential load, CURSET = 1	V_{CC} – 0.5	V_{CC} – 0.2	V
		100Ω differential load, CURSET = 0			V
		150Ω differential load, CURSET = 1			V
		150Ω differential load, CURSET = 0	V_{CC} – 0.5	V_{CC} – 0.2	V
V_{OLC}	Output LOW Voltage (V_{CC} referenced)	100Ω differential load, CURSET = 1	V_{CC} – 1.1	V_{CC} – 0.7	V
		100Ω differential load, CURSET = 0			V
		150Ω differential load, CURSET = 1			V
		150Ω differential load, CURSET = 0	V_{CC} – 1.1	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load, CURSET = 1	560	1200	mV
		100Ω differential load, CURSET = 0			mV
		150Ω differential load, CURSET = 1			mV
		150Ω differential load, CURSET = 0	560	1200	mV

Note:
8. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.

CYP15G0402DX DC Electrical Characteristics Over the Operating Range (continued)

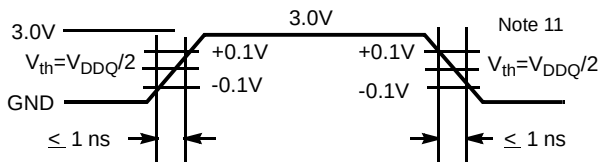
Parameter	Description	Test Conditions		Min.	Max.	Unit
Differential Serial Line Receiver Inputs: INA±, INB±, INC±, IND±						
V_{DIFF}	Input Differential Voltage |(IN+) – (IN–)|			100	1200	mV
V_{IHH}	Highest Input HIGH Voltage			V_{CC} – 1.2	V_{CC}	V
V_{ILL}	Lowest Input LOW Voltage			V_{CC} – 2.0	V_{CC} – 1.45	V
I_{IHH}	Input HIGH Current	$V_{IN} = V_{IHH}$ Max.			750	µA
I_{ILL}	Input LOW Current	$V_{IN} = V_{ILL}$ Min.		–200		µA
Miscellaneous				**Typ.**	**Max.**	
I_{CC}[9]	Power Supply Current	Freq. = Max.	Commercial	730	870	mA
			Industrial			mA

AC Test Loads and Waveforms

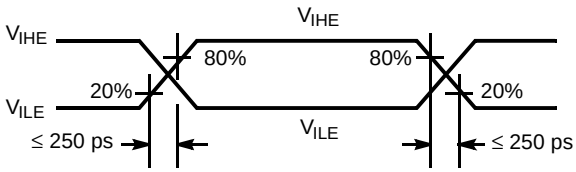


(a) LVTTL AC Test Load [10]

(b) CML AC Test Load [10]



(c) LVTTL Input Test Waveform



(d) PECL Input Test Waveform

Note:

9. Maximum I_{CC} is measured with V_{DDQ} = MAX, V_{CC} = MAX, RFEN = LOW, and outputs unloaded. Typical I_{CC} is measured with V_{CC} = 3.3V, T_A = 25°C, RFEN = LOW, and outputs unloaded.
10. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
11. The TTL switching threshold is VREF, which has a default level of V_{DDQ}/2. All timing references are made relative to the point where the respective rising or falling signal edge crosses this threshold voltage.

CYP15G0402DX Transmitter LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{TS}	TXCLKx Clock Cycle Frequency	20	150	MHz
t_{TXCLK}	TXCLKx Period	6.66	50	ns
t_{TXCLKH}	TXCLKx HIGH Time	2.2		ns
t_{TXCLKL}	TXCLKx LOW Time	2.2		ns
t_{TXCLKR} [12]	TXCLKx Rise Time	0.7	5	ns
t_{TXCLKF} [12]	TXCLKx Fall Time	0.7	5	ns
t_{TXDS}	Transmit Data Set-Up Time to TXCLKx↑ (TXCKSEL ≠ LOW)	1.5		ns
t_{TXDH}	Transmit Data Hold Time from TXCLKx↑ (TXCKSEL ≠ LOW)	1		ns
f_{TOS}	TXCLKO Clock Cycle Frequency (= 1x or 2x REFCLK Frequency)	20	150	MHz
t_{TXCLKO}	TXCLKO Period	6.66	50	ns
$t_{TXCLKOD}$	TXCLKO Duty Cycle	47	53	%
t_{TXOH}	TXCLKO HIGH Time	2.5		ns
t_{TXOL}	TXCLKO LOW Time	2.5		ns
t_{TXODS}	Transmit Data Set-Up Time to TXCLKO↑ (TXCKSEL = LOW)	1.5		ns
t_{TXODH}	Transmit Data Hold Time from TXCLKO↑ (TXCKSEL = LOW)	1		ns
t_{TXRSS}	$\overline{\text{TXRST}}$ Set-Up Time to TXCLKO↑	3		ns
t_{TXRSH}	$\overline{\text{TXRST}}$ Hold Time from TXCLKO↑	1		ns

CYP15G0402DX Receiver LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{RS}	RXCLKx Clock Output Frequency	10	150	MHz
t_{RXCLKP}	RXCLKx Period	6.66	100	ns
t_{RXCLKH}	RXCLKx HIGH Time (RXRATE = HIGH)	2.5	51	ns
	RXCLKx HIGH Time (RXRATE = LOW)	5	25	ns
t_{RXCLKL}	RXCLKx LOW Time (RXRATE = HIGH)	2.5	51	ns
	RXCLKx HIGH Time (RXRATE = LOW)	5	25	
t_{RXCLKR} [12]	RXCLKx Rise Time	0.5	1.2	ns
t_{RXCLKF} [12]	RXCLKx Fall Time	0.5	1.2	ns
t_{RXDS} [13]	Status and Data Set-Up Time To RXCLKx↑	2.5		ns
t_{RXDH} [13]	Status and Data Hold Time From RXCLKx↑	1.5		ns

Notes:

12. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
13. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.

CYP15G0402DX REFCLK Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{REF}	REFCLK Clock Frequency	10	150	MHz
t_{REFCLK}	REFCLK Period	6.6	100	ns
t_{REFH}	REFCLK HIGH Time (TXRATE = LOW)	4.0	70	ns
	REFCLK HIGH Time (TXRATE = HIGH)	2.4	35	ns
t_{REFL}	REFCLK LOW Time (TXRATE = LOW)	4.0	70	ns
	REFCLK LOW Time (TXRATE = HIGH)	2.4	35	ns
t_{REFD}	REFCLK Duty Cycle	30	70	%
t_{REFR}[12]	REFCLK Rise Time	0.3	5	ns
t_{REFF}[12]	REFCLK Fall Time	0.3	5	ns
t_{TREFDS}	Transmit Data Set-Up Time to REFCLK↑ (TXCKSEL = LOW)	1.5		ns
t_{TREFDH}	Transmit Data Hold Time from REFCLK↑ (TXCKSEL = LOW)	1		ns
t_{REFRX}	REFCLK Frequency Referenced to Received Clock Period[14]	–0.02	+0.02	%

CYP15G0402DX Transmit Serial Outputs and TX PLL Characteristics Over the Operating Range

Parameter	Description	Condition	Min.	Max.	Unit
t_B	Bit Time		5000	660	ps
t_{RISE}	CML Output Rise Time 20–80% (CML Test Load)[12]	SPDSEL = HIGH	100	250	ps
		SPDSEL = MID	200	500	ps
		SPDSEL = LOW	400	1000	ps
t_{FALL}	CML Output Fall Time 80–20% (CML Test Load [12]	SPDSEL = HIGH	100	250	ps
		SPDSEL = MID	200	500	ps
		SPDSEL = LOW	400	1000	ps
t_{DJ}	Deterministic Jitter (peak-peak)[12, 15]			35	ps
t_{RJ}	Random Jitter (σ)[12, 16]			8	ps
t_{TXLOCK}	Transmit PLL lock to REFCLK	TBD	TBD	ns	

Notes:

14. REFCLK has no phase or frequency relationship with RXCLK and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±200- ppm (±0.02%) of the transmitter PLL reference (REFCLK) frequency, necessitating a ±100-ppm crystal.
15. While sending continuous K28.5s, outputs loaded to a balanced 100Ω load, over the operating range.
16. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.

Receive Serial Inputs and CDR PLL Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
t_{RXLOCK}	Receive PLL Lock to Input Data Stream (cold start)		10	ms
	Receive PLL Lock to Input Data Stream		2500	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate	TBD	TBD	ns
t_{SA}	Static Alignment[12, 17]			ps
t_{EFW}	Error Free Window [12, 18, 19]	0.75		UI

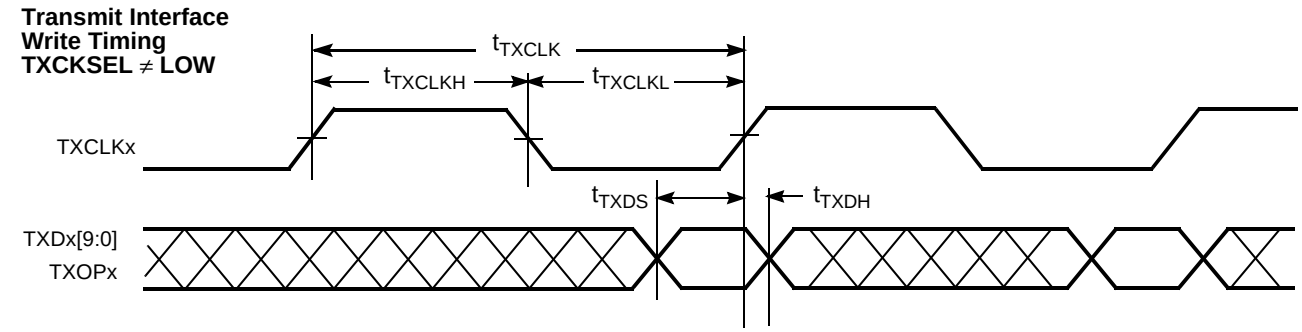
Capacitance[12]

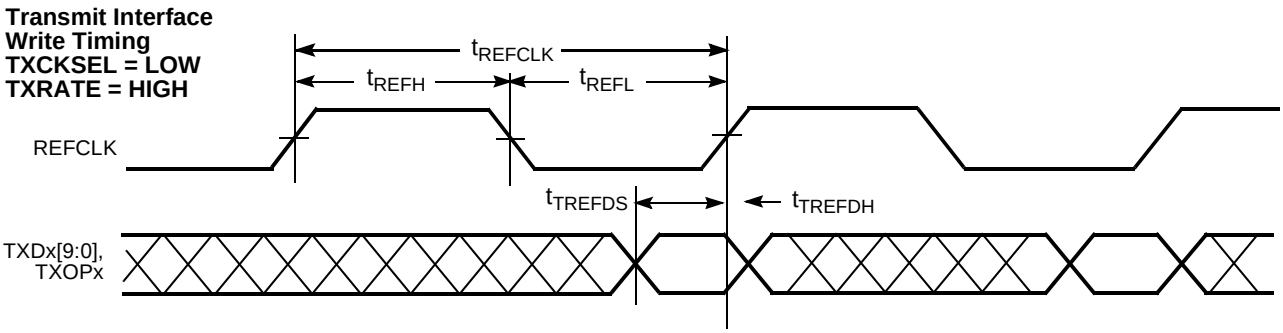
Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 3.3V$	7	pF
C_{INPECL}	PECL input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 3.3V$	4	pF

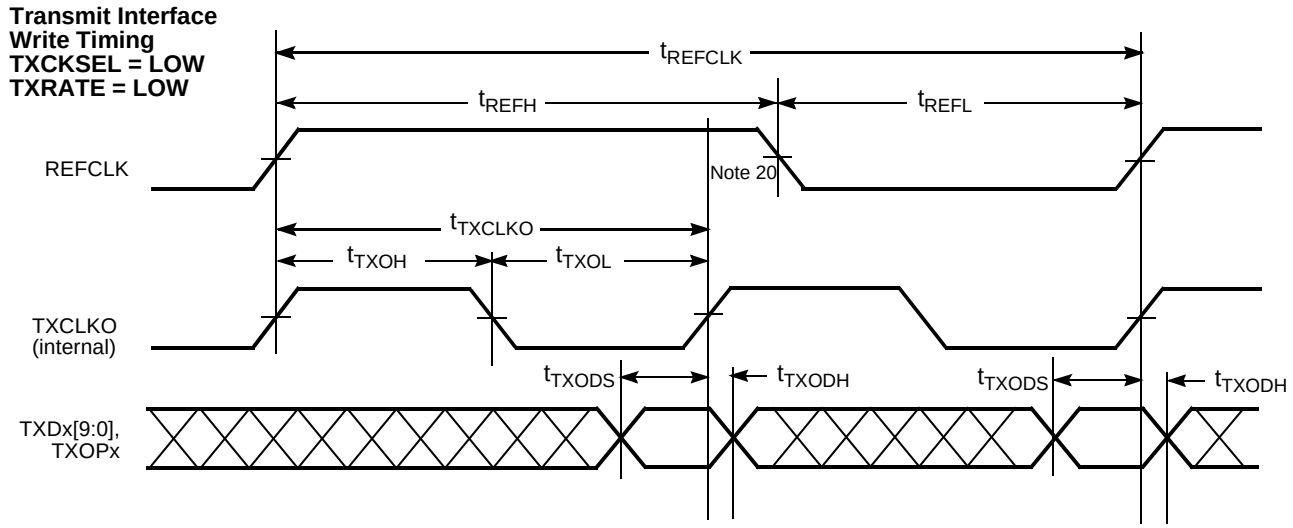
Notes:

17. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a character error occurs.
18. Receiver UI (Unit Interval) is calculated as $1/(f_{REF} * 20)$ (when RXRATE is HIGH) or $1/(f_{REF} * 10)$ (when RXRATE is LOW) if no data is being received, or $1/(f_{REF} * 20)$ (when RXRATE is HIGH) or $1/(f_{REF} * 10)$ (when RXRATE is LOW) of the remote transmitter if data is being received. In an operating link this is equivalent to t_B.
19. Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.

HOTLinkII Transmitter Switching Waveforms







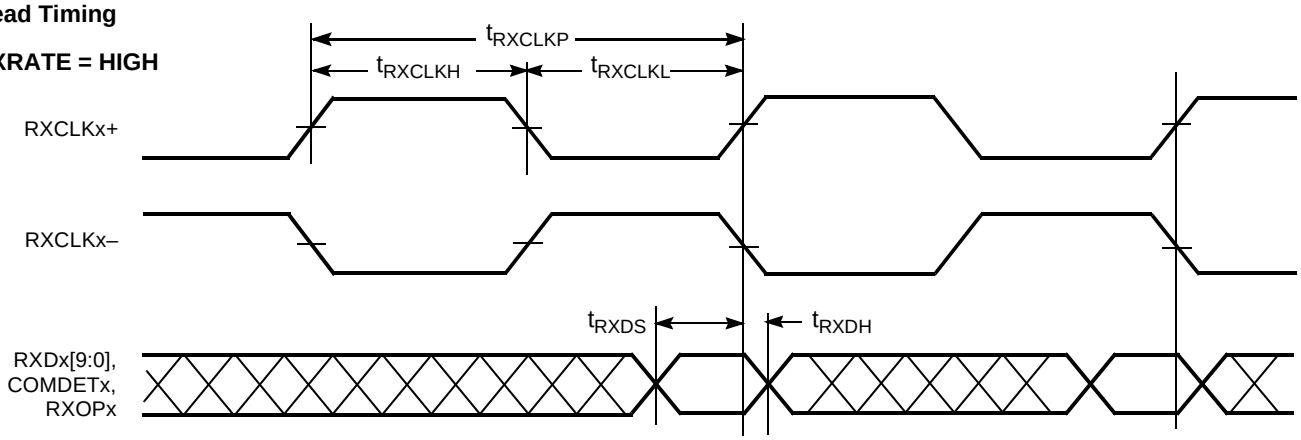
Note:

20. When REFCLK is configured for half-rate operation (TXRATE = LOW) and data is captured using REFCLK instead of a TXCLKx clock (TXCKSEL = LOW), data is captured using the rising edges of the internally synthesized character rate clock. While the rising edge of this clock (TXCLKO) is aligned to the rising edge of REFLCK, it is not aligned to the falling edge of REFCLK.

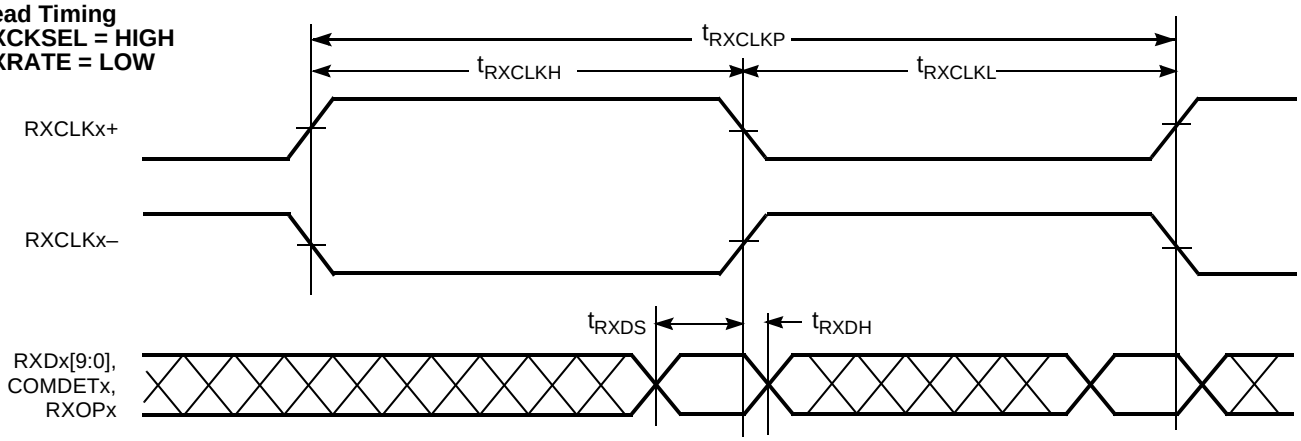
HOTLink II Receiver Switching Waveforms

Receive Interface Read Timing

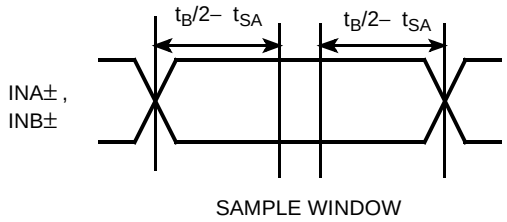
RXRATE = HIGH



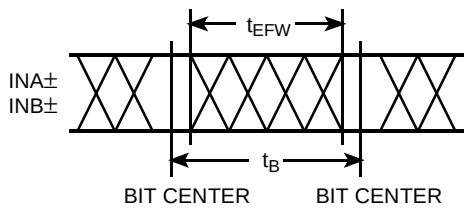
Receive Interface Read Timing
RXCKSEL = HIGH
RXRATE = LOW



Static Alignment



Error-Free Window

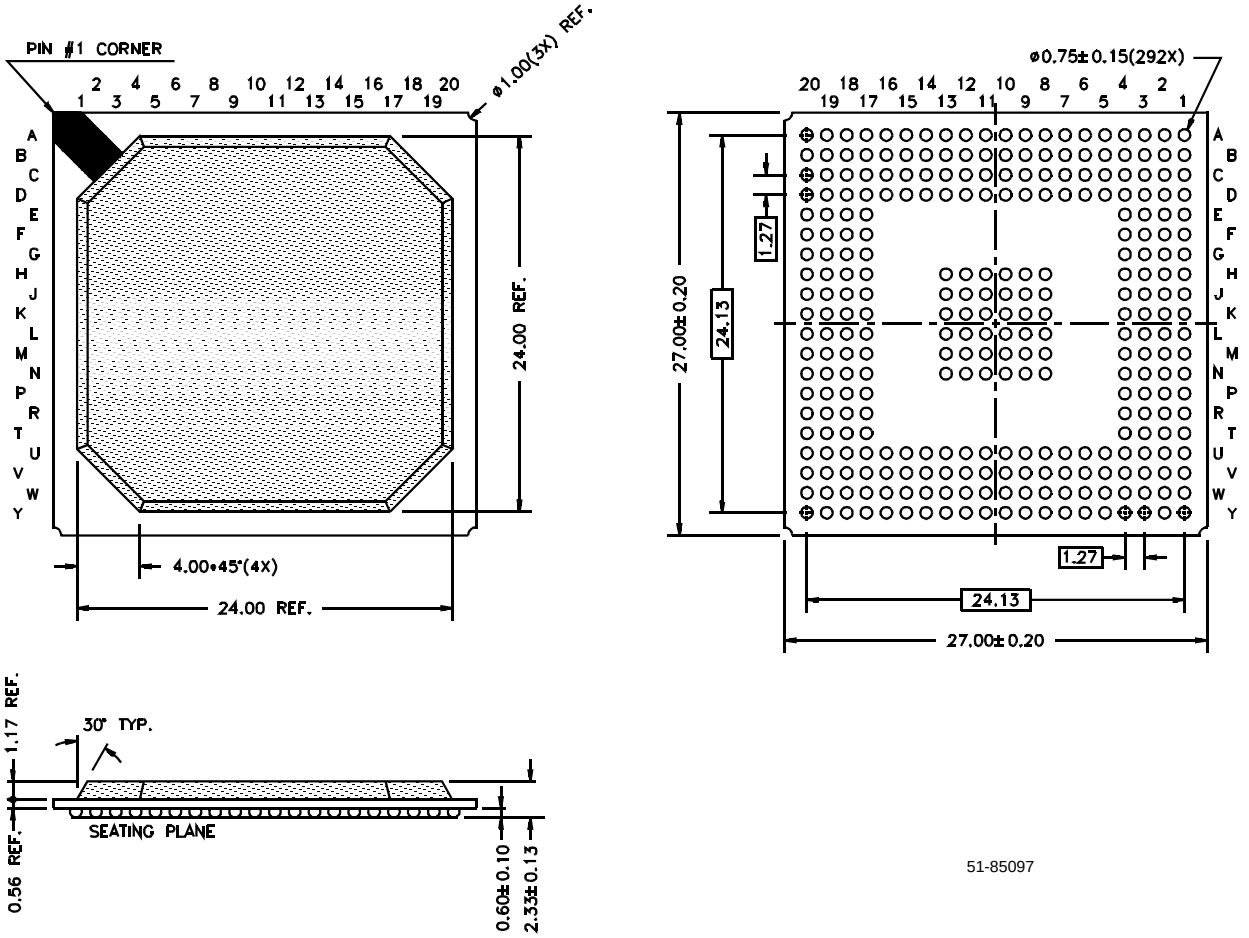


Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYP15G0402DX -BGC	BG256	256-Ball Plastic Ball Grid Array	Commercial
Standard	CYP15G0402DX -BGI	BG256	256-Ball Plastic Ball Grid Array	Industrial

Package Diagram

256-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG256



Document Title: CYP15G0402DX Quad HOTLinkII™ SERDES Document Number: 38-02023				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	108363	07/11/01	TME	New Data Sheet
*A	108915	07/31/01	AMV	Changed name of Part from PHY to SERDES