Multi-Gigabit Multi-Mode Quad Transceiver

Features

- **2.488 Gbps up to 3.125 Gbps per channel**
- **XAUI/10G Ethernet compatible mode**
- **InfiniBand™ compatible**
- **SSTL_2 parallel interface**
- **Programmable 8-bit or 10-bit SERDES**
- **Selectable 8B/10B encoding/decoding**
- **Ethernet PCS functions using the IEEE802.3z ordered set state machine**
- **Programmable framing**
  - **— SONET/SDH A1/A2**
  - **— 1G Ethernet/Fibre Channel, InfiniBand, XAUI 8B/10B COMMA**
- **Diagnostic loop back and line loop back**
- **Signal detect input**
- **Single 2.5 V supply**
- **Low power — 2.5 W typical (625 mW per channel)**
- **Industrial temperature range –40°C to +85°C**

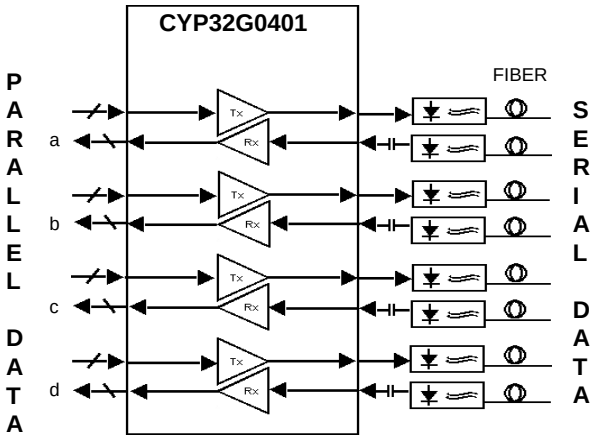


Figure 1. Typical CYP32G0401DX Application Block Diagram

Table 1. CYP32G0401DX Operating Modes

MODE	SER 8_10	EN-CODE	FRAME	APPLICATION
1	0	1	1	10 bit SERDES, 8B/10B encoding/decoding, COMMA framing, and PCS functions
2	0	0	0	10 bit SERDES, no encoding/decoding and no framing
3	0	1	0	10 bit SERDES, 8B/10B encoding/decoding and COMMA framing
4	1	0	0	8 bit SERDES, no encoding/decoding and A1/A2 framing

Choose from four defined operating modes by setting variables SER8_10, ENCODE, and FRAME. Selected mode applies to all four channels.

General Description

The CYP32G0401DX is a fully integrated quad transceiver device capable of operating at serial rates up to 3.125 Gbps per channel. It performs the 8B/10B encode and decode functions compatible with the 10G Ethernet and InfiniBand physical layer, parallel-to-serial, serial-to-parallel, and clock recovery functions for use in LAN and WAN applications. The Multi-Gigabit Multi-Mode versatility of the CYP32G0401DX was designed for backplane applications for WAN, LAN, WIN, and storage networks' switches and routers as well as for InfiniBand™ and XAUI 10G Ethernet port applications.

Functional Description

Overview

Figure 1 shows a block diagram of a typical four-channel application. The transceiver has four defined modes of operation as shown in *Table 1*.

MODE 1 – 10-bit SERDES (Ethernet PCS functions; 8B/10B encoding/decoding; COMMA framing)

The transmit side accepts data in the form of 8-bit words at up to 312.5 Mbps, performs Ethernet PCS functions using the IEEE802.3z ordered set state machine, 8B/10B encoding and serialization of the encoded words into a serial bit stream transmitting at up to 3.125 Gbps. The receive side deserializes the data and performs COMMA framing, 8B/10B decoding, and Ethernet PCS functions. (SER8_10=0, ENCODE=1, FRAME=1).

MODE 2 – 10-bit SERDES (no encoding/decoding; no framing)

The transmit side accepts data in the form of 10-bit words at up to 312.5 Mbps, and serializes them into a bit stream transmitting at up to 3.125 Gbps. The receive side de-serializes the

data. No framing function is performed. (SER8_10=0, ENCODE=0, FRAME=0).

MODE 3 – 10-bit SERDES (8B/10B encoding/decoding; COMMA framing)

The transmit side accepts data in the form of 8-bit words at up to 312.5 Mbps, performs 8B/10B encoding, and serializes the encoded words into a bit stream transmitting at up to 3.125 Gbps. The receive side deserializes the data, and performs COMMA framing and 8B/10B decoding. (SER8_10=0, ENCODE=1, FRAME=0).

MODE 4 – 8-bit SERDES (no encoding/decoding; A1/A2 framing)

The transmit side accepts data in the form of 8-bit words at up to 350 Mbps, and serializes them into a bit stream transmitting at up to 2.8 Gbps. The receive side deserializes the data and performs SONET/SDH A1/A2 framing. (SER8_10=1, ENCODE=0, FRAME=0).

Architecture Overview

Figure 2 is a block diagram showing one of the four multi-gigabit transceiver channels contained within the CYP32G0401DX. Also shown are the internal Management Interface and Frequency Synthesizer blocks, which are common to all channels. Pin names are written in uppercase letters, with lowercase suffixes (a, b, c, d) applied later, as needed, to distinguish among the four channels.

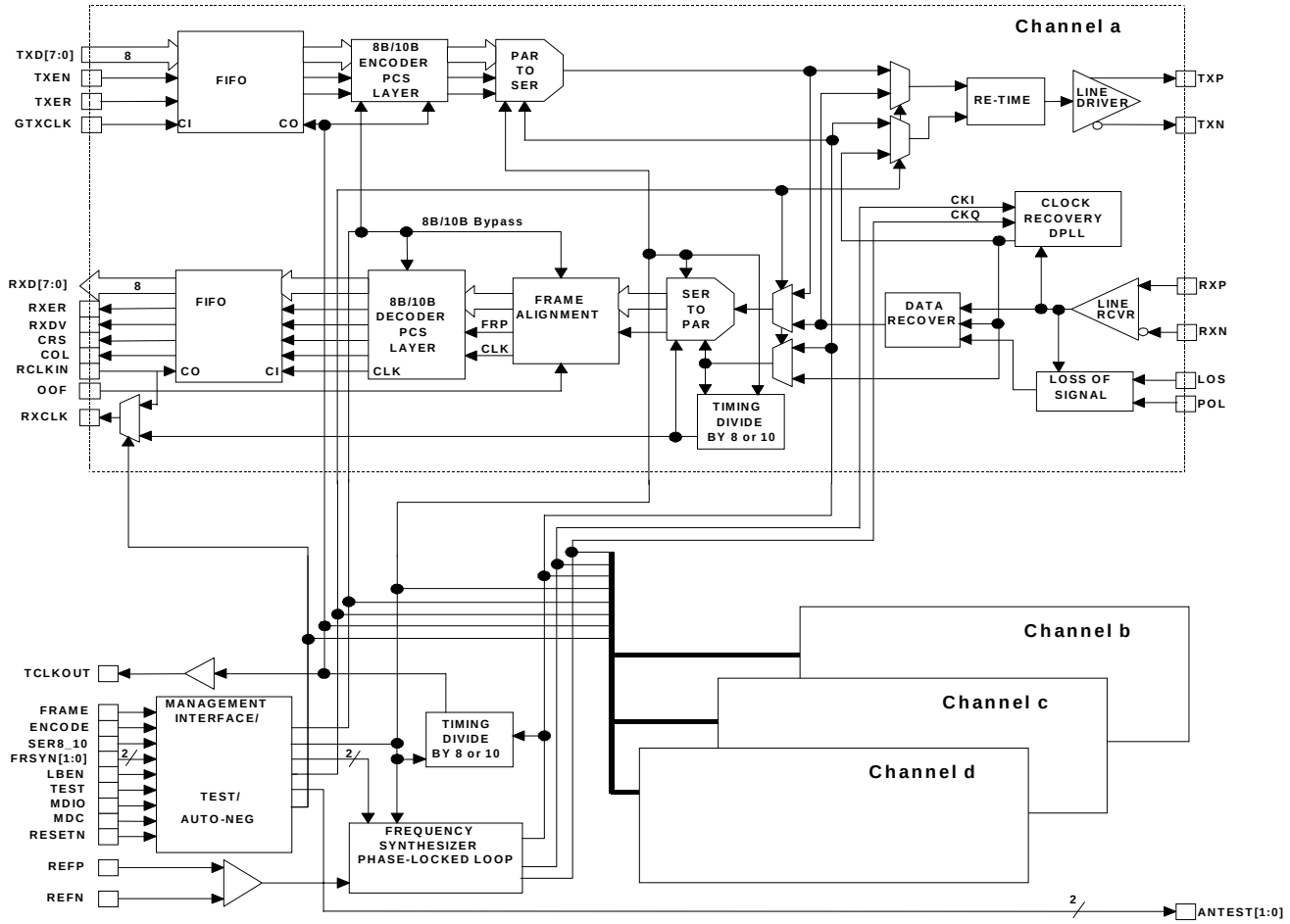


Figure 2. CYP32G0401DX Multi-Gigabit Multi-Mode Transceiver Block Diagram

256-Lead Ball Grid Array (BGA)

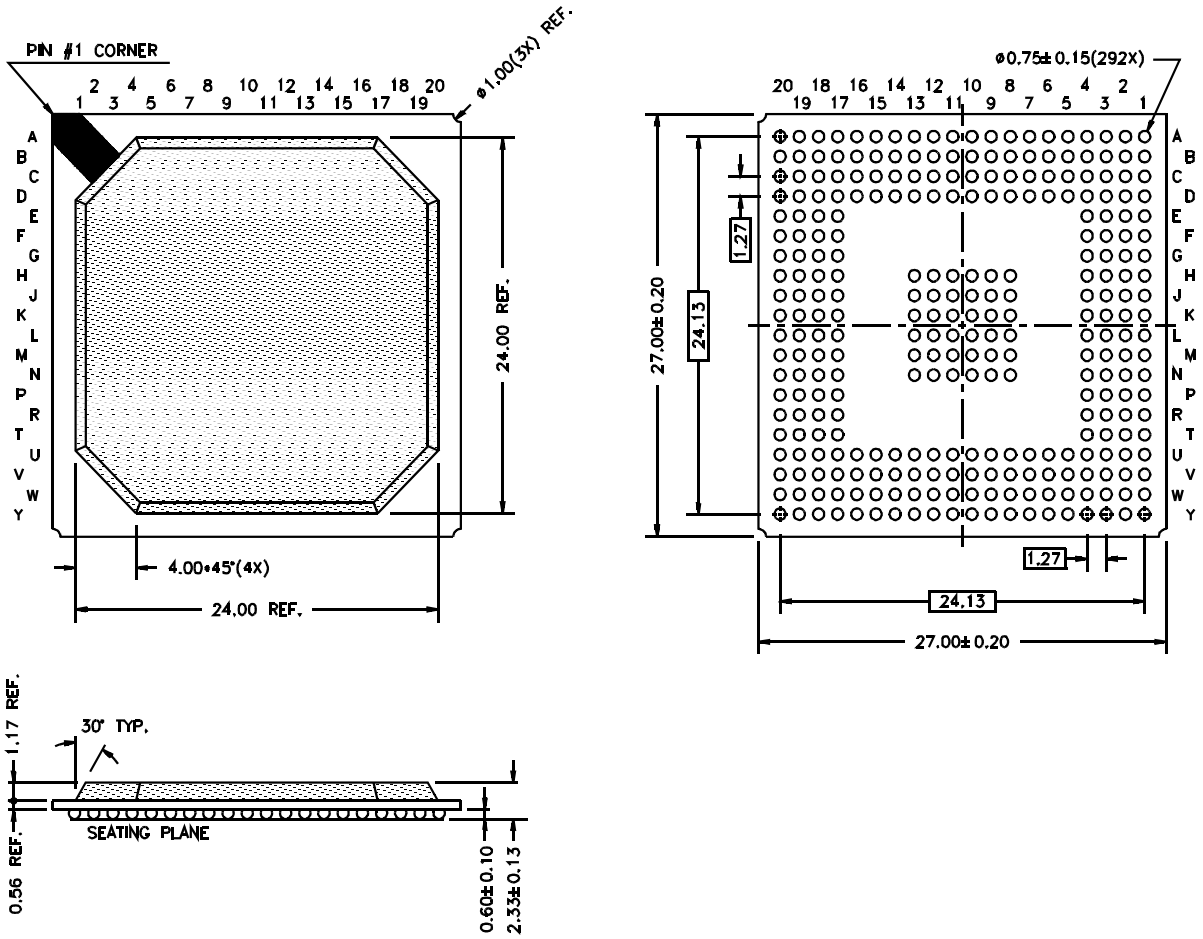
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	DGND	DGND	DGND	RCLKINc	RXD2c	RXCLKc	GTXCLKc	TXD5c	DGND	DGND	TCLKOUT	GTXCLKb	DGND	TXD4b	RCLKINb	RXD7b	RXCLKb	DGND	DGND	DGND
B	DGND	DVDD	DVDD	RXD5c	RXD3c	RXD0c	TXD1c	TXD3c	TXD7c	TXENc	VDIGCc	TXD0b	TXD2b	TXD5b	RXDVb	RXD6b	RXD4b	DVDD	DVDD	DGND
C	DGND	DVDD	DVDD	RXD7c	RXD4c	RXD1c	COLc	TXD2c	TXD6c	TXERc	TSYNC	TXD1b	TXD3b	TXD7b	TXENb	RXD5b	RXD3b	DVDD	DVDD	DGND
D	OOFd	RXDVc	RXERc	DVDD	RXD6c	CRSc	DVDD	TXD0c	TXD4c	DVDD	GDIGCc	GDIGCb	TXD6b	DVDD	TXERb	RXERb	DVDD	RXD2b	RXD1b	RXD0b
E	RXCLKd	RXD7d	RXDVd	OOFc													COLb	CRSb	OOFa	RXCLKa
F	RXD4d	RXD5d	RXD6d	RXERd													OOFb	RXDVa	RXERa	RXD7a
G	RCLKINd	RXD2d	RXD3d	GDIGCd													GDIGCa	RXD6a	RXD4a	RXD3a
H	DGND	RXD0d	RXD1d	COLd													RXD5a	RXD2a	CRSa	RCLKINa
J	GTXCLKd	TXD1d	TXD0d	CRSd													RXD1a	RXD0a	COLa	DGND
K	TXD5d	TXD4d	TXD3d	TXD2d													DVDD	TXD0a	GTXCLKa	DGND
L	DGND	TXD7d	TXD6d	VDIGCd													TXD4a	TXD3a	TXD2a	TXD1a
M	DGND	TXENd	DVDD	TXERd													TXENa	TXD7a	TXD6a	TXD5a
N	RESETN	TEST	FRSYN1	FRSYN0													MDIO	TXERa	VDIGCa	DGND
P	ANTEST0	ANTEST1	GTXMc	AVDD													AVDD	VRXMb	MDC	VDIGCb
R	REFP	VTXMc	VRXMc	GTXMd													VTXMb	TRS	TCK	TMS
T	REFN	GRXMc	VTXMd	VRXMd													GRXMa	GTXMb	TDI	TDO
U	GRXMd	ENCODE	FRAME	AVDD	LOSd	GRXDd	AVDD	TXNd	TXPd	GTXDc	VTXDb	TXNa	TXPa	AVDD	GRXDa	GTXMa	AVDD	VRXMa	LBEN	GRXMb
V	AGND	AVDD	AVDD	SER8_10	LOSc	POLd	GRXDc	GTXDd	TXNc	TXPc	TXPb	TXNb	GTXDa	GRXDb	VRXDa	LOSb	POLa	AVDD	AVDD	AGND
W	AGND	AVDD	AVDD	VRXDd	RXNd	RXPd	VTXDd	GFS3	VTXDc	GFS1	VFS2	GTXDb	VTXDa	VRXDb	RXNa	RXPa	VTXMa	AVDD	AVDD	AGND
Y	AGND	AGND	AGND	POLc	VRXDc	RXNc	RXPc	AGND	VFS3	VFS1	AGND	AGND	GFS2	RXNb	RXPb	POLb	LOSa	AGND	AGND	AGND

Figure 3. Pin Configuration

Package Diagram

256-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG256



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