Interfacing with the SST™

This application note describes how to interface the CY7B951 SONET/SDH Serial Transceiver (SST™) with other physical-layer devices. The SST performs clock and data recovery from a SONET/SDH (Synchronous Optical NETwork/Synchronous Digital Hierarchy) 51.84 Mb/s or 155.52 Mb/s interface and can be used in a variety of SONET and ATM applications. The application note will begin with a brief introduction to the SST. Next, interface examples will be given that illustrate how to connect the SST to three different ATM controller devices; the first from PMC-Sierra called the PM5345 SUNI, the second, also from PMC-Sierra, called the S/UNI-LITE, and the third from Integrated Telecom Technologies (IgT) called the WAC-013.

Introduction

The CY7B951 SST is used in SONET/SDH applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit Clock, from a byte-rate source through the use of a frequency multiplier Phase-Locked Loop (PLL), and differential data buffering for the Transmit side of the system (see *Figure 1*). The pinout is shown in *Figure 2.*

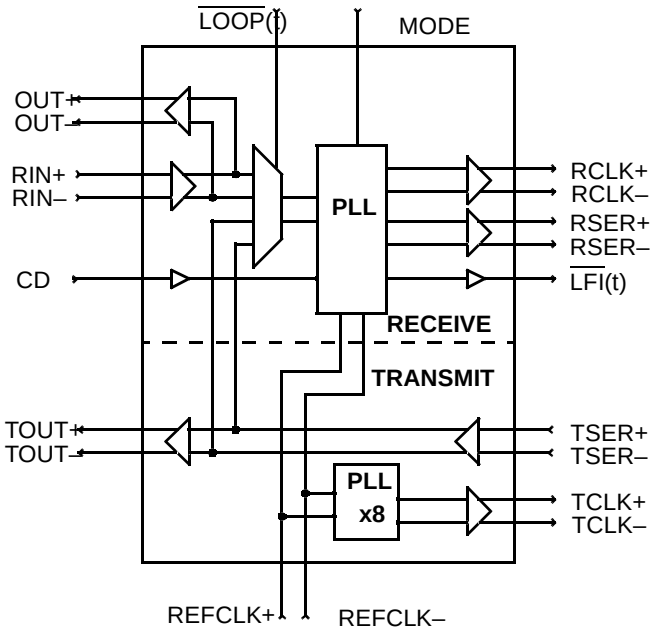

Figure 1. SST Block Diagram

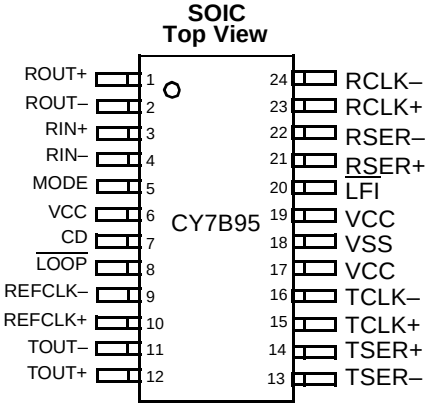

Figure 2. SST Pinout

Operating Frequency

The SST operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. When MODE is connected to V_{CC}, the highest operating range of the device is selected. A 19.44-MHz ±1% source must drive the REFCLK input and the transmit PLL will multiply this rate by 8 to provide an output clock that operates at 155.52 MHz ±1%. When the MODE input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48-MHz ±1% source must drive the REFCLK inputs and the transmit PLL will multiply this rate by 8 to provide an output clock that operates at 51.84 MHz ±1%. In addition, when the MODE input is left unconnected or forced to approximately $V_{CC}/2$, the device enters Test Mode.

Transmit Functions

The Transmit section of the SST contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLK*8) to produce a PECL (Pseudo ECL or Positive ECL) differential output clock (TCLK±). The Transmitter has two operating ranges that are selectable with the three-level MODE pin, as explained above. The SST Transmit frequency multiplier PLL allows low-cost byte-rate clock sources to be used to time the upstream serial data transmitter.

The REFCLK± inputs can be configured in three different ways. When both REFCLK+ and REFCLK– are connected to a differential 100K compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK– or the REFCLK+ input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the SST yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical fiber drivers, twisted pair, or coaxial cable.

Receive Functions

The primary function of the Receiver is to generate recovered clock (RCLK±) and data (RSER±) signals from the incoming differential PECL data stream (RIN±). These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (2–5V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media (such as coaxial cable or twisted pair).

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK*8) and is used as a bit-rate reference in comparison to the recovered clock to improve PLL lock time, and to provide a center frequency for operation in the absence of input data stream transitions. The Receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE pin, as explained earlier. To ensure accurate data and clock recovery, REFCLK*8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLK*8 frequency accuracy be within 20–100 ppm.

The differential input serial data (RIN±) is not only used by the PLL to recover the clock and data, but it is also buffered and presented as the PECL differential output pair ROUT±. This output pair can be used as part of the transmission line interface circuit for base-line wander compensation, improving system performance by providing reduced input jitter and increased data eye opening.

Carrier Detect (CD) and Link Fault Indicator ($\overline{\text{LFI}}$) Functions

The Link Fault Indicator ($\overline{\text{LFI}}$) output is a TTL-level output that indicates the status of the Receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. $\overline{\text{LFI}}$ is controlled by the Carrier Detect (CD) input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper-based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL-compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a PECL LOW, the $\overline{\text{LFI}}$ output will transition LOW, the Receiver PLL will align itself with the REFCLK*8 frequency, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data stream inputs (RIN).

In addition, the SST has a built-in transitions detector that also checks the quality of the incoming data stream. The absence of data transitions can be caused by a break in the transmission media, a problem at the transmitter end of the media, or a problem with the transmit or receive media coupling hardware. The SST will detect a quiet link by counting the number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 512 bit times have passed without a data transition on RIN±, $\overline{\text{LFI}}$ will transition LOW. The Receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK*8 frequency. This will insure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. $\overline{\text{LFI}}$ will be driven HIGH again and the Receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 512 bit times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW (≤0.8V). When CD is pulled to a TTL LOW, the $\overline{\text{LFI}}$ will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLK*8 frequency. $\overline{\text{LFI}}$ LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When $\overline{\text{LFI}}$ is left unconnected, an internal pull-down resistor will pull this input to ground.

Loop Back Testing

The TTL level $\overline{\text{LOOP}}$ pin is used to perform loop-back testing. When $\overline{\text{LOOP}}$ is asserted (held LOW) the Transmitter serial inputs (TSER±) are used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT±) and the differential Receiver inputs (RIN±). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the $\overline{\text{LOOP}}$ input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The $\overline{\text{LOOP}}$ feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the $\overline{\text{LOOP}}$ pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

Power-Down Modes

There are several power-down features on the SST. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output current. If the TOUT± or ROUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected the entire Transmit PLL will be powered down.

By leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC} the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the ($\overline{\text{LFI}}$ will still reflect the state of the CD input. This feature can be used for aggressive power management.

Interfacing with the PM5345 (SUNI)

The PM5345 is used in ATM applications for SONET frame processing, ATM cell processing, and error monitoring. The PMC-Sierra SUNI device requires Receive serial data aligned with a bit-rate clock. These signals need to be supplied through the RXD± and RXC± inputs respectively. A

155.52-MHz PECL Transmit clock (TXC±) is required to provide PM5345 transmit side clocking. For copper-based systems, the TXD± outputs must be buffered in order to drive transmission lines with low impedances. Lastly, a LOS detection is required from the clock and data recovery engine to aid in the determination of the LOS, LOF, and OOF error conditions reported by the SUNI device. This signal is brought in through the SUNI GPIN (General Purpose Input). Before the introduction of the SST, clock and data recovery devices were interfaced to the PMC-SUNI as shown in *Figure 3.*

Figure 4 shows the SST signal connections with the PMC-Sierra PM5345 SUNI. The SST, together with the PM5345, provides a complete Physical layer interface. The Receive section of the SST provides serial SONET/SDH data at 155.52 Mb/s to the receive section of the PM5345 (RXC± and RXD±). The Transmit section of the SST provides the transmit side 155.52-MHz clock that is used by the PM5345 TXCI± input by multiplying a 19.44-MHz oscillator by eight. This function eliminates the need for an expensive 155.52-MHz oscillator to be used in the system. The SST buffers the TXD± output signals from the SUNI device for driving copper-based systems or for improved operation in fiber-based systems.

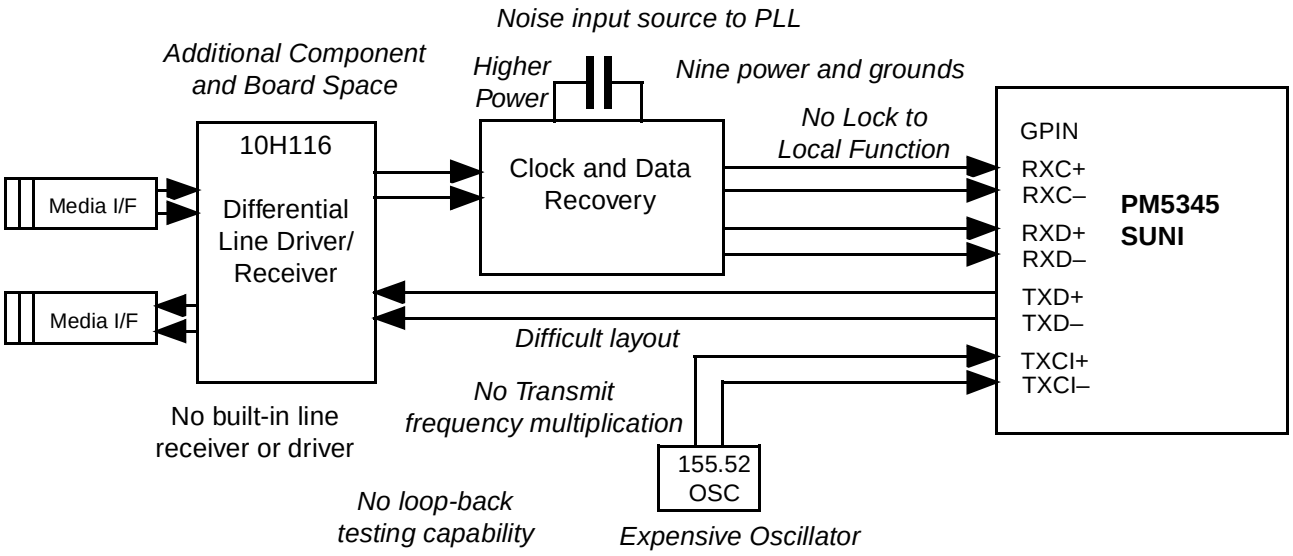

Figure 3. Typical SUNI interface without the Use of the SST

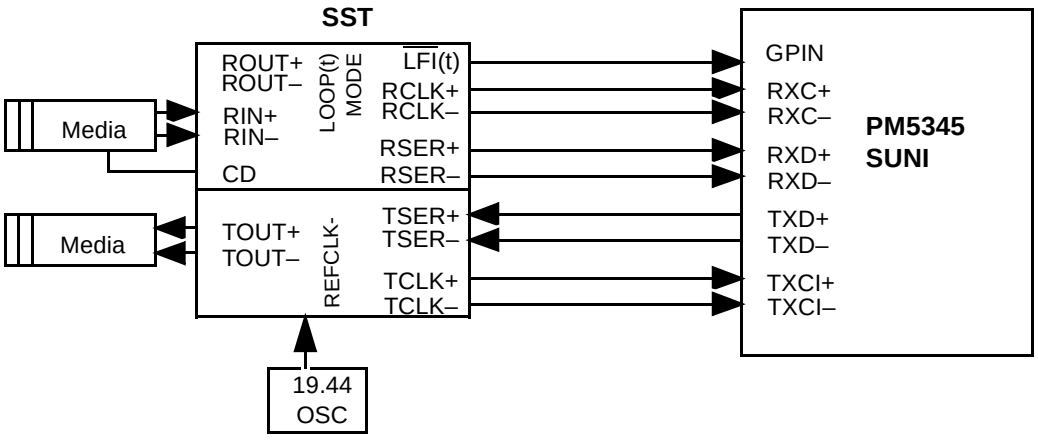

Figure 4. SST to PMC-Sierra PM5345 SUNI Connection Diagram

The $\overline{LFI}$ output is used to drive the GPIN input. This $\overline{LFI}$ output will transition LOW when any of the following occur: the CD (Carrier Detect) input transitions LOW, the frequency of the incoming data is outside of the lock range of the Receive PLL, or there have been no transitions in the incoming data stream for the last 512 bit times. Additionally, when the CD input is forced LOW by an output from a source such as the signal detect of an optical module or an external transition detection circuitry for copper-based systems, the SST will force the RSER± outputs LOW. This will aid the SUNI device in the determination of the LOS state and minimize the length of time needed to determine an error condition.

Figure 5 shows an electrical interface of the SST to the PMC-SUNI device. Each SST PECL output is AC coupled into the SUNI inputs with a .01-µF capacitor, and is loaded with an 80Ω pull-up resistor and a 130Ω pull-down resistor. This scheme allows the SUNI device to self-bias (since the SUNI has a bias circuit built into each PECL input) its inputs and also provides the SST outputs with 50Ω terminations to approximately V_{CC} – 2V. The termination resistors are bypassed with .01-µF capacitors to provide high-speed switching current. For PCB trace impedances higher than 50Ω, the terminating resistors should be scaled accordingly. For example, a 100Ω transmission line would require a pull-up resistor of 160Ω and a pull-down resistor of 260Ω. Terminations for the SST outputs (TCLK, RCLK, RSER) should be placed as close to the SUNI as possible.

The TXD± outputs require different termination resistors values. The ideal biasing voltage for TXD± is 4.2V. This bias is achieved by connecting a 62Ω pull up to TAVD and a 330Ω pull down to GND at the end of the termination line connecting TXD± and TSER±. These resistor values are calculated based on Z_0 = 50Ω. For PCB trace impedances higher than 50Ω, the terminating resistors should be scaled accordingly. For example, a 100Ω transmission line would require a pull-up resistor of 120Ω and a pull-down resistor of 636Ω. In addition, the VT2 resistor should also be scaled from 628Ω to 1260Ω when using 100Ω trace impedances. In general, R_{VT2} = 12.564 * Z_0.

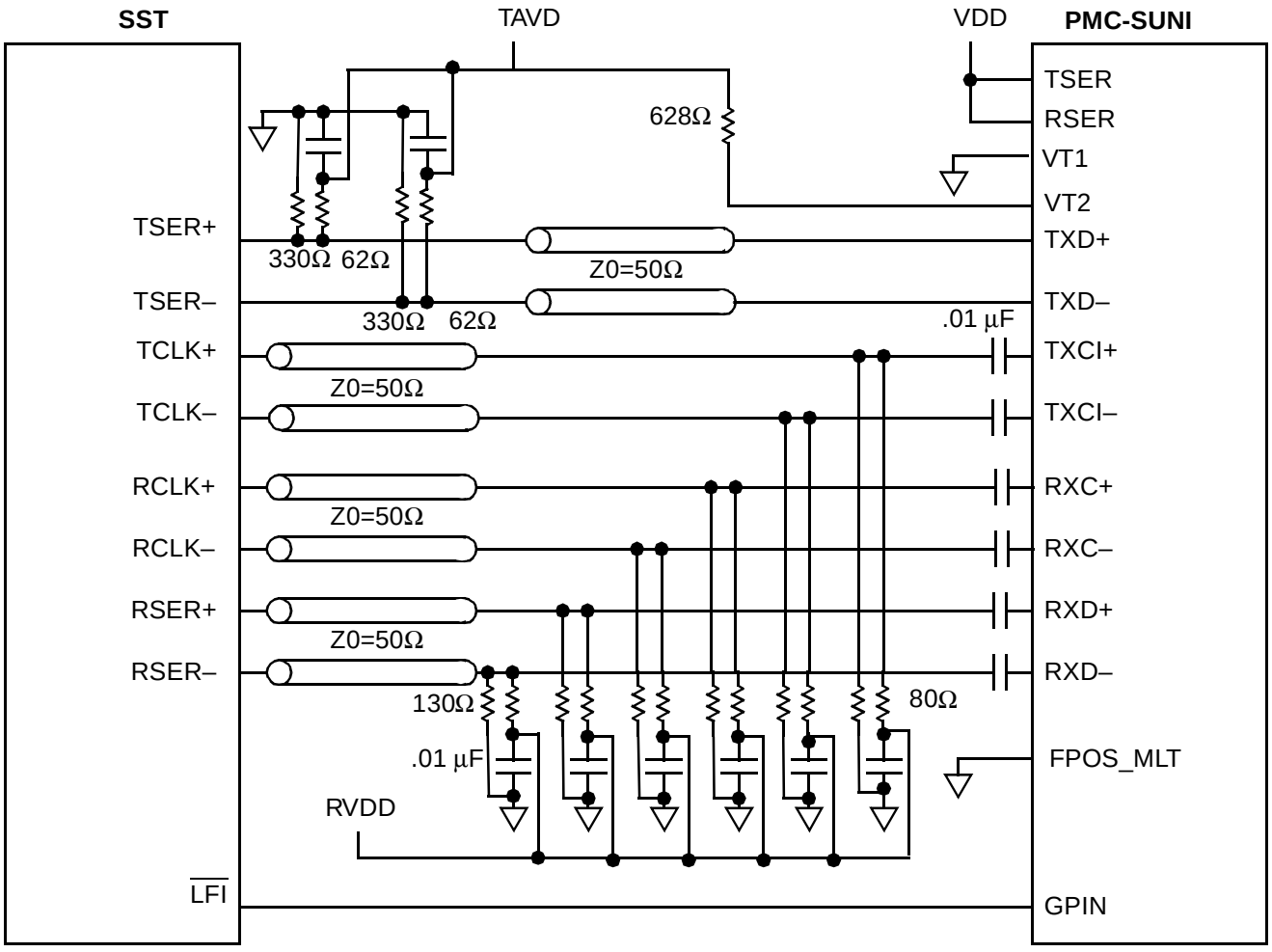

Figure 5. High Performance SST to PMC SUNI Interface

Interfacing with the PM5346 (S/UNI-LITE)

The PM5346 is another PMC-Sierra product used in ATM systems for clock and data recovery, SONET frame processing, ATM cell processing, and error monitoring. Its small package size makes it more desirable than the PM5345 in cases where not all of the SONET frame processing functions of the PM5345 are needed. For performance reasons, the PLL of S/UNI-LITE can be bypassed and the SST can be used to perform clock and data recovery functions for the S/UNI-LITE.

Figure 6 shows how to interface the SST to the S/UNI-LITE. When RBYP is tied HIGH, the internal PLL of the S/UNI-LITE is disabled and RRCLK± is used to sample RXD±. In this configuration, the SST is used to supply the bit-aligned RRCLK. This is achieved by connecting RCLK± to RRCLK± and RSER± to RXD± using four equal-length traces. Each of these traces has an 80Ω pull-up to RVDD and a 130Ω pull-down to GND. These termination resistors are bypassed with .01-µF capacitors to satisfy the high-speed switching current requirements. A .01-µF DC-blocking capacitor is used in series with the transmission line to allow the S/UNI-LITE to self-bias its inputs (since the S/UNI-LITE, like the SUNI, also has bias circuits built into each PECL input). All these passive components are placed close to the S/UNI-LITE.

In the same way, the transmit side PLL of the S/UNI-LITE can also be disabled. When TBYP is tied HIGH, the clock multiplication function of the S/UNI-LITE is disabled and the 155.52-MHz or 51.84-MHz clock received from either RRCLK± or TRCLK± is used for clocking the transmit portion of the S/UNI-LITE. If the LOOPT bit of the Master Control register of the S/UNI-LITE is 1, RRCLK will be used and when the LOOPT bit is 0, TRCLK± will be used. TRCLK± is supplied by TCLK± of the SST. The termination/biasing circuit used for this TRCLK connection is the same as that used in the RXD± and RRCLK± connections described previously. These termination/biasing circuits should also be placed as close to the S/UNI-LITE as possible.

For the TXD± to TSER± connections, a 237Ω source resistor in series with a .01-µF capacitor placed closed to the S/UNI-LITE side is used with a 67Ω pull-up to TAVD and a 192Ω pull-down to GND placed close to the SST side to provide the necessary termination and biasing.

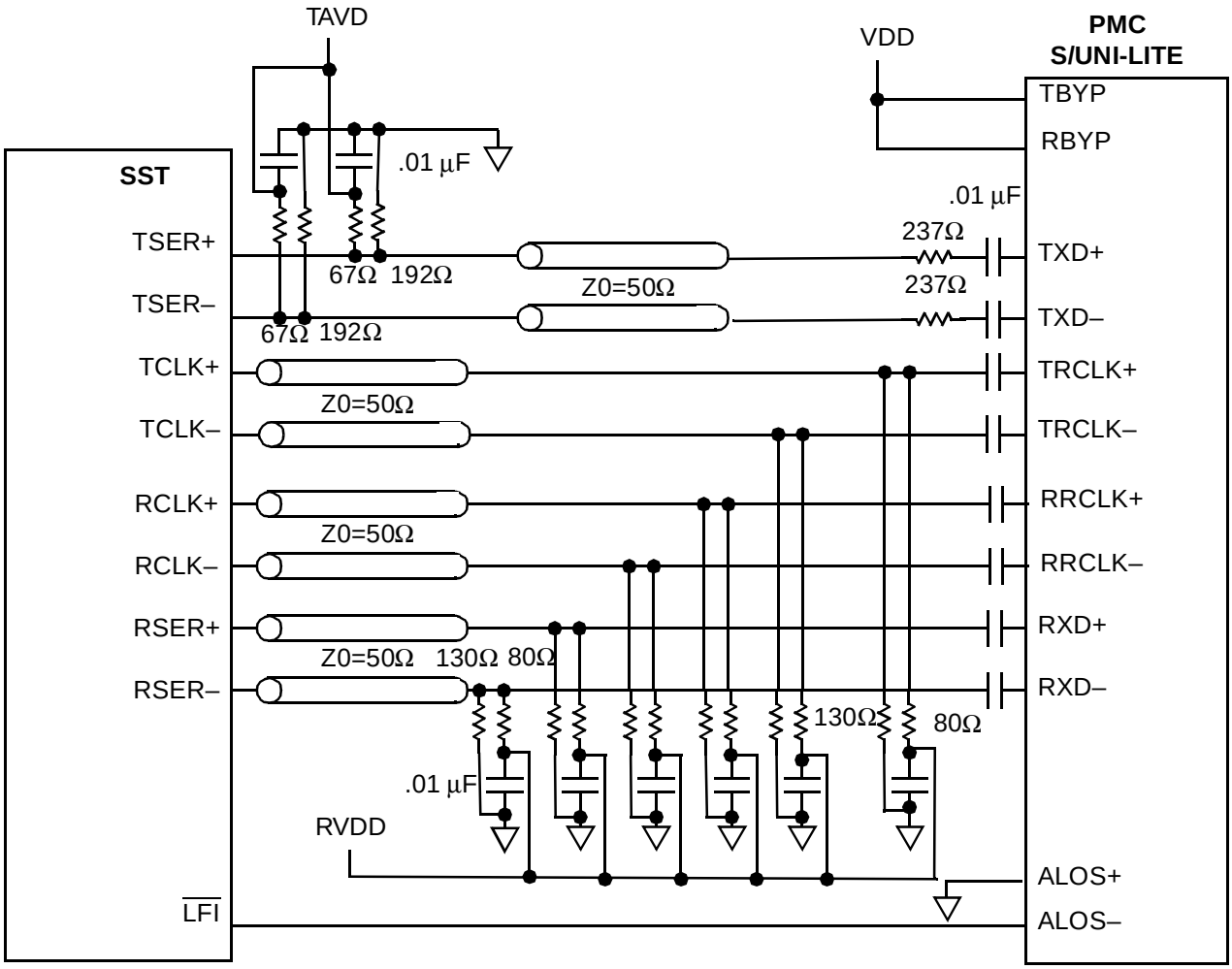

Figure 6. High Performance SST to PMC S/UNI-LITE Interface

Interfacing with the IgT WAC-013.

The Integrated Telecom Technology (IgT) WAC-013 provides SONET frame processing, ATM cell processing, and error monitoring. The IgT device requires differential PECL Receive data (RS_SER_DATA) aligned with a differential PECL bit-rate clock (RS_SER_CLK). These signals represent the recovered clock and data from a SONET/SDH STS-3/STM-1 data stream of 155.52 Mb/s or a SONET STS-1 data stream of 51.84 Mb/s. The WAC-013 also requires a bit-rate transmit-clock (TS_SER_CLK) for Transmit Side clocking. The transmit data (TS_SER_DATA) should also be buffered for driving low-impedance transmission lines or copper transmission media. Prior to the introduction of the SST, clock and data recovery devices were connected to the WAC-013 as shown in *Figure 7*.

Figure 8 shows the SST signal connections with the IgT WAC-013. The SST, together with the WAC-013, provides a complete physical-layer interface. The Receive section of the SST provides serial SONET/SDH data at 155.52 Mb/s or 51.84 Mb/s (depending on the state of the SST MODE pin) to the Receive section of the IgT RS_SER_DATA and RS_SER_CLK inputs. The Transmit section of the SST provides the bit-rate clock (TS_SER_CLK) and Transmit buffering of the TS_SER_DATA outputs. The SST multiples a 19.44-MHz reference clock (6.48-MHz for STS-1 applications) by eight to produce the 155.52-MHz (51.84-MHz) transmit clock. This frequency multiplication function eliminates the need for an expensive 155.52-MHz crystal oscillator.

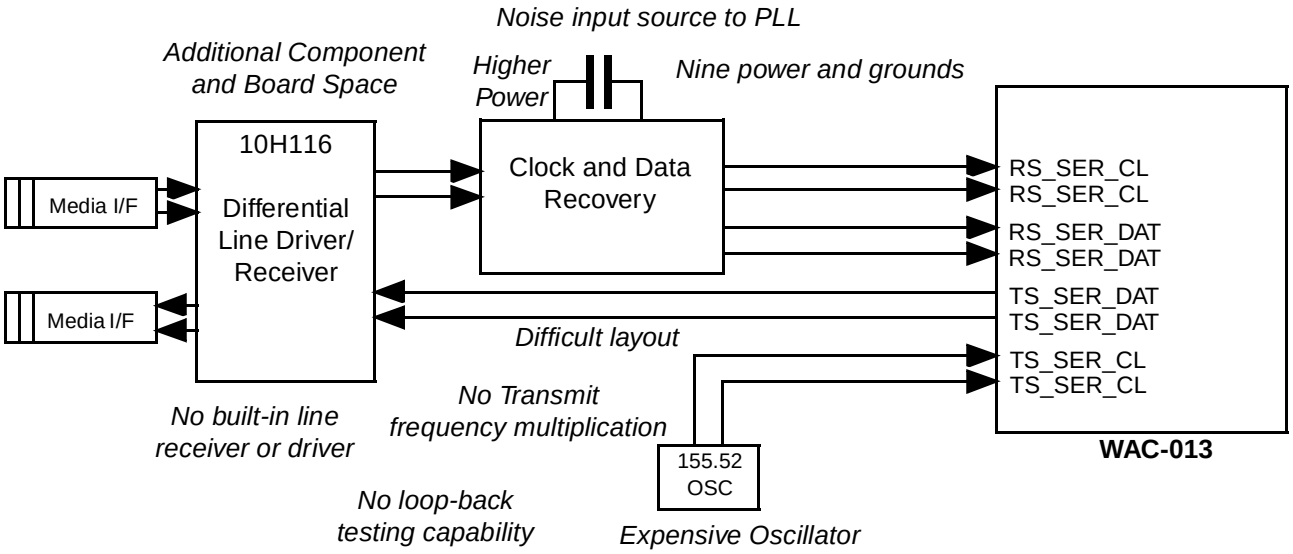

Figure 7. Typical WAC-013 interface without the Use of the SST

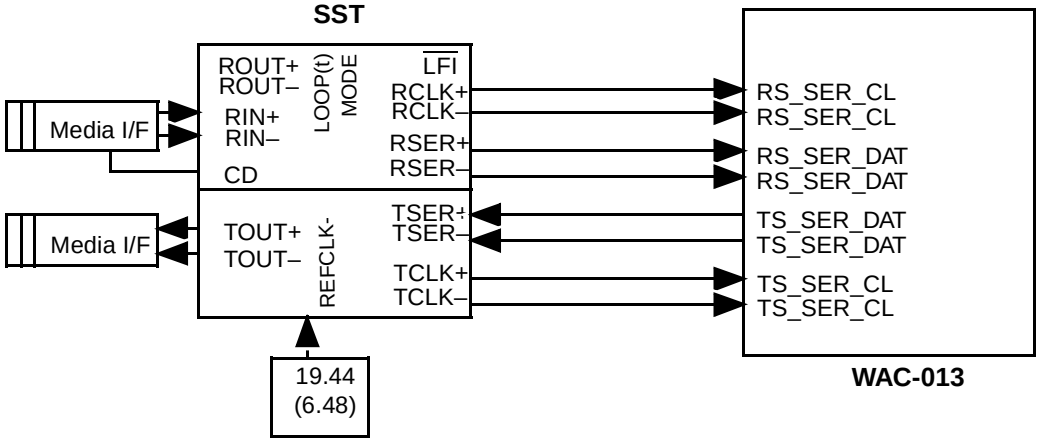

Figure 8. SST to IgT WAC-013 Connection Diagram

Figure 9 shows the electrical interface of the SST to the WAC-013. The outputs are loaded and terminated with 80Ω pull-up resistors and 130Ω pull-down resistors at the load. This provides a 50Ω termination to V_{CC} – 2V. These resistors are also bypassed with a .01-µF capacitor to provide high-speed switching current. For PCB trace impedances higher than 50Ω, the terminating resistors should be scaled accordingly. For example, a 100Ω transmission line would require a pull-up resistor of 160Ω and a pull-down resistor of 260Ω.

Conclusion

The interface examples shown in this note demonstrate how to connect the SST to the PMC-Sierra PM5345 SUNI, the PMC-Sierra PM5346 S/UNI-LITE, and the IgT WAC-013. Together these devices provide a complete physical-layer solution for ATM applications over SONET/SDH at 155.52 Mb/s and 51.84 Mb/s. The SST greatly simplifies the physical-layer implementation with its ability to generate a Loss of Signal indication, its capability to lock to the local reference clock during error conditions, and its capacity to buffer the transmit data stream for driving low-impedance transmission lines. The SST also reduces the cost of physical-layer implementations by eliminating the need for a 155.52-MHz crystal oscillator with its ability to multiply a byte-rate clock to provide the bit-rate transmit source. Cypress's expertise in PLL-based clock and data recovery as well as the added features of the SST provide designers with the capacity to create simple, low cost, and robust ATM physical-layer designs.

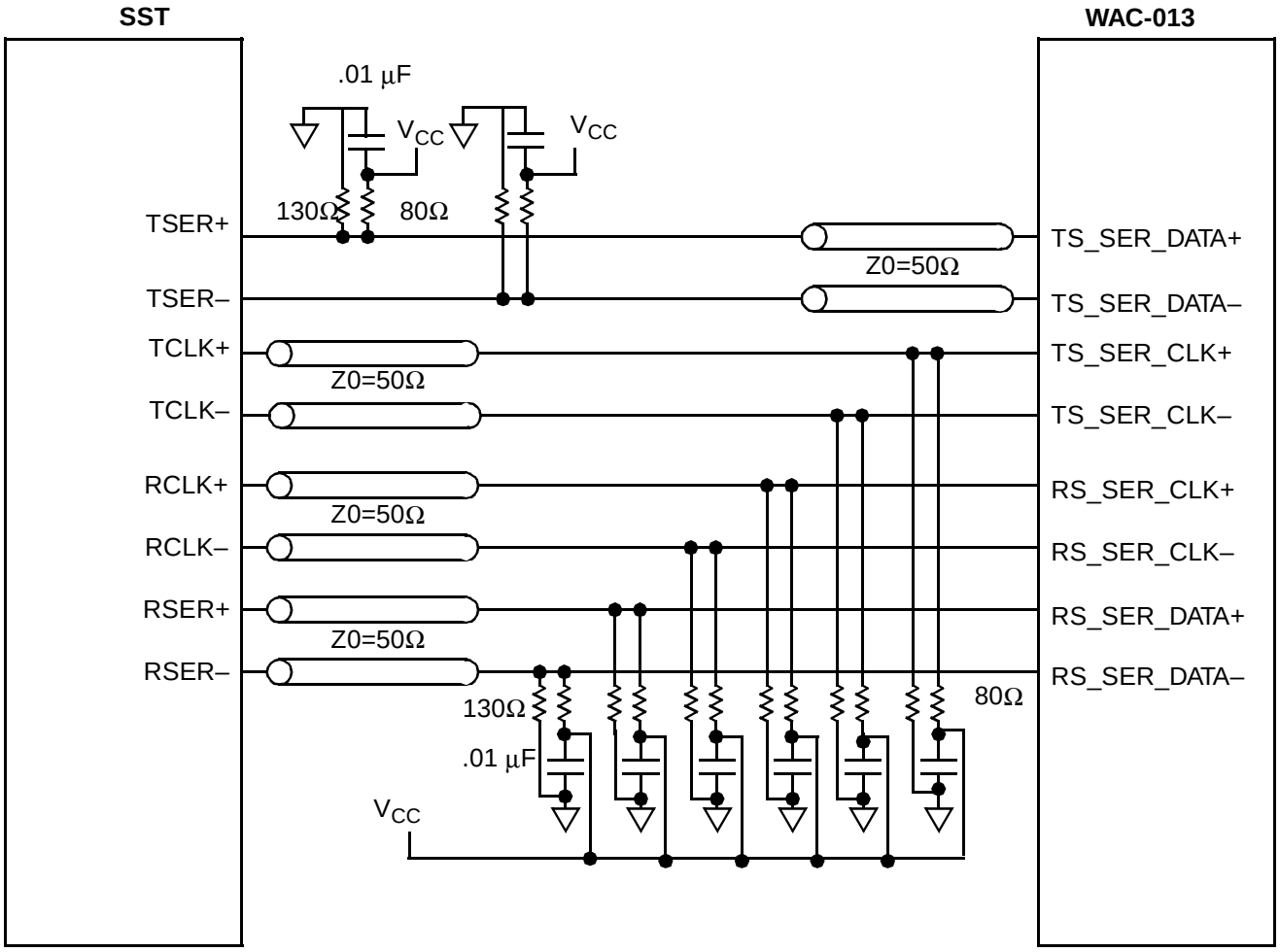

Figure 9. High Performance SST to WAC-013 Interface

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