CY9267 SMPTE 259M Evaluation Board User's Guide

Overview

This document describes the construction, interfaces, and operation of the CY9267 SMPTE 259M evaluation board. Complete artwork and schematics are also included.

The CY9267 evaluation board implements a complete bidirectional ANSI/SMPTE 259M Serial Digital Interface (SDI) using the Cypress SMPTE Chip Set. The SMPTE Chip Set is comprised of 4 components:

- CY7C9235 SMPTE 259M/DVB-ASI Scrambler-Controller
- CY7B9234 SMPTE HOTLink™ Transmitter
- CY7C9335 SMPTE 259M/DVB-ASI Descrambler/Framer-Controller
- CY7B9334 SMPTE HOTLink Receiver

The transmit portion of the chip set consists of the CY7C9235 and CY7B9234. Together they provide the proper scrambling, encoding, and parallel-to-serial conversion of digital component (SMPTE125M) or composite (SMPTE 244M) video. The receive portion of this chip set consists of the CY7B9334 and CY7C9335. Together they provide the proper serial-to-parallel conversion, decoding, descrambling, and framing of these same video formats. Additional information on the Cypress SMPTE chip set can be found in the following documents:

- "Implement a SMPTE 259M Serial Digital Interface Using SMPTE HOTLink and CY7C9235/9335" application note
- CY7B9234/9334 SMPTE HOTLink Transmitter/Receiver datasheet
- CY7C9235 SMPTE 259M/DVB-ASI Scrambler-Controller datasheet
- CY7C9335 SMPTE 259M/DVB-ASI Descrambler/Framer-Controller datasheet

The CY9267 SMPTE evaluation board provides a simple evaluation vehicle for the Cypress SMPTE Chip Set. It accepts a parallel digital video stream via a 25-pin D-subminiature (D-sub) connector. This input is both mechanically and electrically compliant with SMPTE bit-parallel digital interfaces. The parallel video is then encoded and serialized. The serialized encoded video is output through two 75Ω BNC outputs.

The receiver portion of the CY9267 evaluation board accepts a SMPTE 259M-BCD serial video stream via a 75Ω BNC input, and deserializes and frames the data. The framed video stream is then output as a SMPTE compliant bit-parallel data stream through another 25-pin D-sub connector. Additional header pins and connectors are provided for monitoring various signals, including a separate BNC output for "eye diagram" monitoring of the received equalized serial stream.

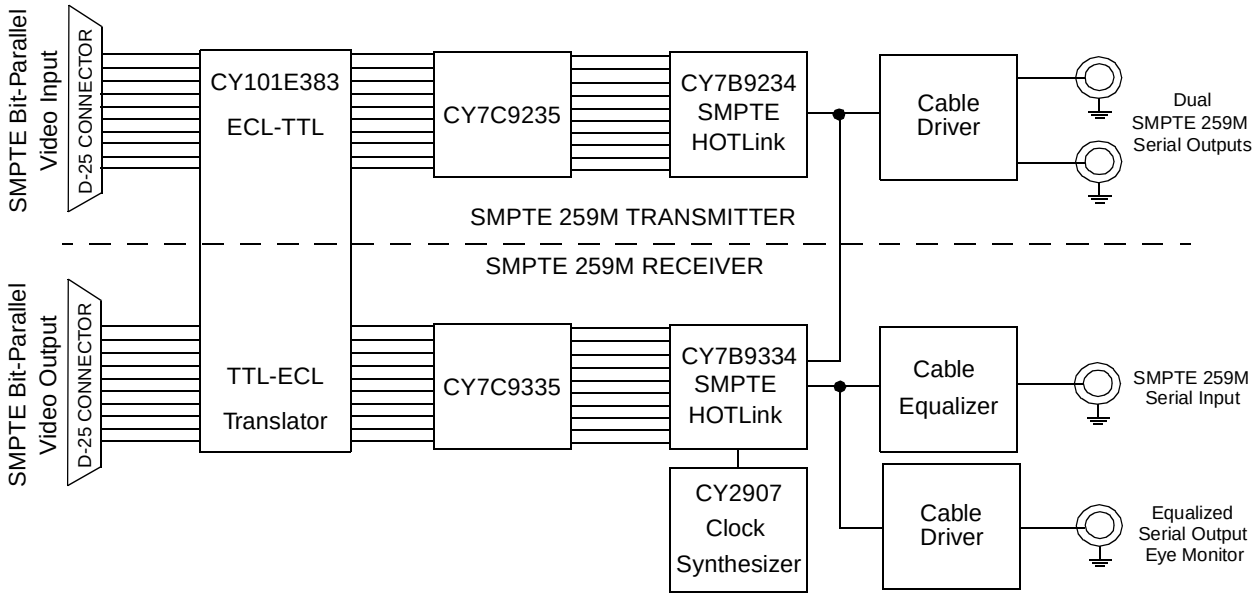

Figure 1. Block Diagram of CY9267 SMPTE 259M Evaluation Board

The evaluation board can also be used as a stand-alone transport vehicle for 10-bit 4:2:2 component or $4f_{SC}$ composite digital video streams across 75Ω coaxial cables. It is fully compliant to ANSI bit-parallel and ANSI/SMPTE 259M-BCD serial interface standards.

Functional Description

The block diagram in *Figure 1* illustrates the major functional components of the CY9267 SMPTE evaluation board. A detailed and complete schematic, parts list, and layout are provided later in this document.

The CY9267 evaluation board has numerous features:

- Serialization of SMPTE 125M, 267M, or 244M bit-parallel digital video in compliance to SMPTE 259M-BCD
- Deserialization of SMPTE 259M-BCD digital video
- Selectable local loopback operation
- Selectable scrambler/descrambler bypass mode for sending user defined data
- Buffered equalized eye monitor
- Header pins for easy access to input and output signals
- 3-pin screw terminal or 6-pin PC power supply inputs
- LED indicators for power and signal detection

The transmit path accepts a bit-parallel digital video stream through a female 25-pin D-sub connector. This parallel data is expected to conform to SMPTE 125M (Component Video Signal 4:2:2- Bit Parallel Digital Interface), SMPTE 244M (System M/NTSC Composite Video Signals-Bit-Parallel Digital Interface), or SMPTE 267M (Component Video Signal 4:2:2, 19x9 Aspect Ratio). These standards specify the signalling to be ECL levels.

For operation with the Cypress SMPTE chip set, these ECL signals must be converted to the TTL domain. A CY101E383 is used to translate the ten differential data lines to TTL levels. The parallel interface, however, contains eleven differential ECL signals (ten data and one clock), requiring an additional ECL-TTL translator. A Motorola MC100ELT24 (not shown in *Figure 1*) is used for the translation of the clock.

The parallel TTL-level data is then captured by a CY74FCT825T (not shown in *Figure 1*). This register is necessary to allow the parallel interface to operate with the minimum setup and hold times specified by the SMPTE standards for bit-parallel interfaces. The output of this register is then fed to the CY7C9235 SMPTE/DVB Scrambler Controller.

The CY7C9235 scrambles and encodes the data, then passes the parallel data to the CY7B9234 SMPTE HOTLink Transmitter for serialization. The differential PECL outputs of the CY7B9234 are connected to both a cable driver and the inputs of the CY7B9334 SMPTE HOTLink Receiver (for loopback operation). The cable driver outputs connect to two female 75Ω BNC connectors.

The receive path accepts a serial video input through a female 75Ω BNC connector. The serial input is first processed by an adaptive cable equalizer. This equalizer removes the effects of frequency selective attenuation and dispersion caused by cables. The equalized output is a PECL-level signal that connects to a second line driver, and to the CY7B9334 SMPTE HOTLink Receiver.

This second line driver allows access to the equalized signal. It can be used for either an "eye monitor" output, or for a loop-through path to additional SMPTE receivers. While this monitor output meets all the amplitude and drive requirements of SMPTE-259M, the delivered signal may not be usable at the full 300m distance of the transmit path serial outputs. This is because the signal at this point is only equalized and redriven, but it has not been reclocked to remove all the jitter.

The CY7B9334 SMPTE HOTLink Receiver accepts the equalized and buffered serial-video signal for deserialization. It uses a high performance PLL to extract a bit-rate clock from the transitions in the data stream. This bit-rate clock is then used to sample the data stream and capture the bits in the data stream. The CY7B9334 converts the individual bits into 10-bit characters. These characters are output with a synchronous character rate clock.

A character-rate reference clock must be furnished to the CY7B9334. This clock is used only as a reference and has no phase relationship to either the received serial video stream or the output character clock. This clock is generated using a CY2907 General Purpose Clock Synthesizer. This device has two control inputs (S0 and S1) which determine which of the four SMPTE 259M clock rates are generated.

The 10-bit parallel characters output from the CY7B9334 are connected to the CY7C9335 SMPTE/DVB Descrambler/Framer. It reverses the encoding and scrambling operations added to the serial stream, and frames the data to the proper character boundaries. The TTL parallel output of the CY7C9335 is converted back to ECL levels using the other half of the CY101E383 that provided the ECL-TTL translation. A Motorola MC100ELT25 is used to translate the clock. The parallel ECL output drives another female 25-pin D-sub connector.

Input/Output Description

25-Pin D-Subminiature Connector

The CY9267 evaluation board has two female 25-pin D-sub connectors labelled J1 and J2. J1 presents parallel video that has been decoded and framed from a serial SMPTE 259M-BCD input. J2 accepts parallel video input to be serialized. The pinout for both 25-pin D-sub connectors is defined by the SMPTE 125M, 244M, and 267M standards and is shown in *Table 1*. The pin numbering of the 25-pin D-sub connector is shown in *Figure 2*.

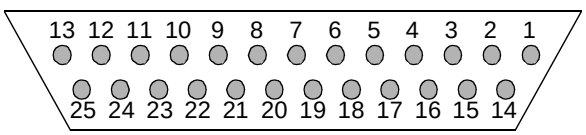

Figure 2. Pin Numbering for Female 25-Pin D-Sub Connector

Bayonet Neil-Councilman (BNC) Connectors

The CY9267 evaluation board has four female 75Ω BNC connectors labelled J7–J10. J9 and J10 present the serialized outputs from the cable driver. These BNC outputs are identical in functionality but opposite in phase. They can be used

Table 1. SMPTE 25 Pin D-Sub Connector Definition

PIN	SIGNAL LINE	PIN	SIGNAL LINE
1	CLOCK	14	CLOCK RETURN
2	SYSTEM GND	15	SYSTEM GND
3	DATA9 (MSB)	16	DATA9 RETURN
4	DATA8	17	DATA8 RETURN
5	DATA7	18	DATA7 RETURN
6	DATA6	19	DATA6 RETURN
7	DATA5	20	DATA5 RETURN
8	DATA4	21	DATA4 RETURN
9	DATA3	22	DATA3 RETURN
10	DATA2	23	DATA2 RETURN
11	DATA1	24	DATA1 RETURN
12	DATA0 (LSB)	25	DATA0 RETURN
13	CABLE SHIELD		

to monitor the serial scrambled-data, to connect to a separate piece of SMPTE 259M compliant equipment, or to connect to the local receiver to complete a serial link.

The remaining BNC connectors are associated with the receive path. J7 is the serial input to the receiver which can be fed from the local J9 or J10 outputs of the transmit path, or from a separate piece of equipment. J8 is the redriven equalized serial output from the cable equalizer which can be used for "eye diagram" monitoring or as a feed through path to other SMPTE equipment.

Power Supply

The CY9267 SMPTE evaluation board requires two supply voltages, +5V ±10% and –5V ±10%, with a common ground reference. The positive supply is used for all components necessary for SMPTE 259M operation, while the negative supply is used only for the ECL/TTL interface conversion required by the SMPTE parallel interfaces. Two connectors, J3 and J6, are provided for powering the board.

J3 is designed to mate with the PS9 power connector from a PC power supply. The PS9 connector is one of two designed to mate with the PC's motherboard. This connector has pin assignments as shown in *Figure 3*.

NOTE: Improper use of a PC power supply can result in damage to the CY9267 evaluation board. These supplies contain a second power connector (PS8) that also mates with J3. This second connector presents voltages (+12V) and a pinout that are incompatible with J3. Older versions of these supplies may also not regulate correctly, or may generate excessive switching noise, with the small load of the CY9267.

The J6 connector is a 3-pole terminal block. This connector allows attachment of standard bench power supplies via screw terminal attachment of wire leads from the supply.

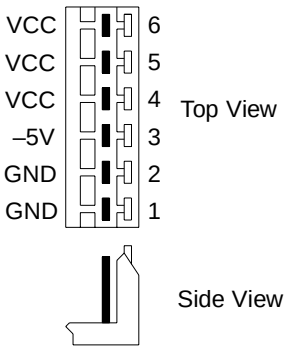

Figure 3. J3 Pin Assignment

LEDs

There CY9267 contains three status LEDs. The LEDs indicate

- LED1= +5V supply present
- LED2= –5V supply present
- LED3= SIG DET (valid signal present at J7)

Header Pins

Two arrays of header pins, J4 and J5, allow access to the parallel data streams. J4 provides access to the receive path DATA9–DATA0 outputs, and J5 provides access to the transmit path DATA9–DATA0 input signals between the input register and the CY7C9235 scrambler. GND and CLK signals are also present to allow simple tracing of these signals with a logic analyzer. The pin assignments on J4 and J5 are the same, and are shown in *Figure 4*.

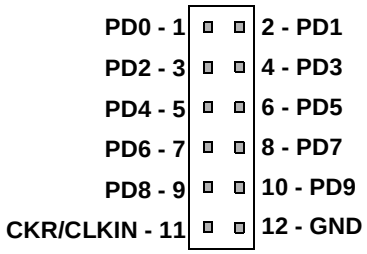

Figure 4. Pin Assignments For J4 and J5

Jumper Pins and Test Points

The CY9267 is configurable, through a number of jumpers, for multiple data rates and multiple modes of operation. The jumpers and a number of test points are collectively located near the center of the CY9267 evaluation board, and are shown in *Figure 5*.

Six jumpers (JP1–JP6) allow the board to be configured to perform various functions and modes of operation. Incorrect configuration of the jumpers may prevent the board from operating correctly.

The different modes of operation are described in the Configuration Settings section of this document. Additional information on many of the signals can be found in the CY7C9235

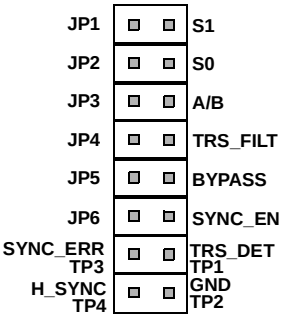

Figure 5. Jumper and Test Point Pin Assignment

and CY7C9335 datasheets. The jumper functions are as described in *Table 2*.

Three test or monitor points are also provided. These are used to access outputs of the SMPTE chip set. The various test points can be monitored with either a logic analyzer or oscilloscope. The signals present on these test points are listed in *Table 3*.

Table 2. Jumper Pin Descriptions

Schematic Label	Signal Name	Description			
JP1/JP2	S1/S0	JP1	JP2	Frequency	These jumpers control the CY2907 clock synthesizer. The CY2907 provides the reference clock for the SMPTE receiver. They should be set to match the expected character-rate clock of the video stream. All four SMPTE standard rates are available. * The CY7B9234 and CY7B9334 are not certified for operation at the 14.3 MHz character rate.
		OFF	OFF	36.0 MHz	
		OFF	ON	27.0 MHz	
		ON	OFF	17.7 MHz	
		ON*	ON*	14.3 MHz*	
JP3	A/$\overline{B}$	This jumper controls the A/$\overline{B}$ input of the CY7B9334. When no jumper is present, the CY7B9334 accepts a serial stream input from the J7 BNC connector. When a jumper is present, the CY7B9334 accepts its serial stream directly from the CY7B9234 for local loopback mode.			
JP4	BYPASS	This jumper controls the BYPASS inputs of the CY7C9235/9335. When no jumper is present, the BYPASS inputs are pulled HIGH (active). Data is routed around both the SMPTE scrambler and the NRZI encoder on the CY7C9235. On the CY7C9335, data is routed around both the SMPTE descrambler and NRZ decoder. When a jumper is present, data is passed through the SMPTE scrambler/descrambler and encoder/decoder.			
JP5	$\overline{\text{TRS\_FILT}}$	This jumper controls the TRS_FILT input of the CY7C9235. When no jumper is present, data is passed to the scrambler without modification. When a jumper is present, all characters from 000–003 are converted to 000, and all characters from 3FC–3FF are converted to 3FF. This allows generation of a proper 30-bit TRS when 8-bit video or non-standard video streams are sent.			
JP6	SYNC_EN	This jumper controls the filtering of TRS sequences in the CY7C9335. When no jumper is present, the SYNC_EN input of the CY7C9335 is pulled HIGH (active). When active, and a TRS sequence is detected, if the 10-bit character boundary is different from that of the previously received TRS, the H_SYNC output is toggled, but the character offset is not updated. If the immediately following TRS also has a different offset, the H_SYNC output is again toggled and the character offset is updated to match that of the detected TRS sequence. When a jumper is in place, the SYNC_EN input of the CY7C9335 is LOW and the framer will update the character offset and toggle H_SYNC on all detected TRS sequences.			

Table 3. Output Test Point Definition

Schematic Label	Signal Name	Description
TP1	$\overline{\text{TRS\_DET}}$	This test point provides access to the $\overline{\text{TRS\_DET}}$ output of the CY7C9235. This output indicates when a character used in the TRS sequence is detected in the input register. If the data contains any of the reserved TRS characters (000–003 or 3FC–3FF in 10-bit hex), this output goes LOW for one clock period. If the character in the input register is any other character, this output remains HIGH.
TP3	SYNC_ERR	This test point provides access to the SYNC_ERR output of the CY7C9335. This output pulses HIGH for one CKR clock period to indicate the detection of a TRS that is offset from its previous 10-bit character offset. This only occurs when SYNC_EN is active (JP1) and the character offset is not updated.
TP4	H_SYNC	This test point provides access to the H_SYNC (horizontal sync) output of the CY7C9335. This output toggles every time a TRS is recognized.

CY9267 SMPTE Evaluation Board Set-Up

A +5V, GND, and –5V supplies must be provided through either the J3 (6-pin PC power supply) or J6 (3-pole terminal block) connectors. The respective LEDs should indicate (light on) when proper power is provided to the board.

NOTE: These LEDs only indicate that a supply is present with the correct polarity. No check is performed on the specific voltage levels presented by the power supply.

The parallel inputs of the SMPTE transmitter and parallel output of SMPTE receiver can be monitored by means of a logic analyzer or oscilloscope on the J4 and J5 header pins.

The output serial stream can be monitored through either J9 or J10. To view a stable output eye diagram, this output should be driven into a 75Ω load, with the scope trigger being based on the CLKIN transmit-path clock. This clock reference is available on J5-11.

The serial receive signal can be monitored (following equalization) at J8. To view a stable output eye diagram, this output should be driven into a 75Ω load, with the scope trigger being based on the CKR receive-path recovered clock. This clock reference is available on J4-11.

Due to the wide bandwidths of these high-speed serial signals, an oscilloscope with at least 1 GHz bandwidth should be used for measurements on the serial video signals.

Configuration

The CY9267 SMPTE evaluation board can be used in four different modes: serialization, deserialization, local loopback and bypass. These modes operate at all supported data rates. The appropriate jumper settings for each mode are discussed in *Table 2* and the following paragraphs.

The CY9267 SMPTE evaluation board is compliant to SMPTE 259M-BCD. This means that it supports (at a minimum) the following video formats and data rates:

- Level B - 177 Mbps PAL composite
- Level C - 270 Mbps 525/625 Component Video
- Level D - 360 Mbps 525/625 Component Video

NOTE: Level A (143 Mbps NTSC composite) is not presently supported by the CY7B9234 and CY7B9334.

Serialization

The conversion of parallel SMPTE 125M, 244M, or 267M digital video into a SMPTE 259M-BCD compliant serial stream is the normal operating mode of the transmit path of the CY9267 evaluation board. In this mode, SMPTE compliant bit-parallel data is accepted at the J2 connector, scrambled, encoded, serialized, and output through J9 and J10. For proper operation, parallel digital data with a character clock is required as a signal source and must be connected to J2.

This parallel input can be sourced from the J1 output on the CY9267 SMPTE evaluation board, or from a separate piece of equipment. The SMPTE 259M serial output from J9 or J10 can then be connected to either a separate piece of equipment or to the serial input of the receiver (J7). To avoid signal losses and reflections due to impedance mismatches, 75Ω coaxial cable should be used for these connections.

To operate in this mode, the JP4 and JP5 jumpers must be present.

Deserialization

The conversion of SMPTE 259M-BCD compliant serial video into parallel SMPTE 125M, 244M, or 267M digital video is the normal operating function of the SMPTE receiver path of the CY9267 evaluation board. In this mode SMPTE compliant serial data is accepted at J7, equalized, deserialized, decoded, descrambled, framed and output through J1. For proper operation, a serial video stream must be connected to J7.

This serial video input can be sourced from either the J9 or J10 outputs of the local SMPTE transmitter, or from a separate piece of equipment.

To operate in this mode, the JP4 and JP6 jumpers must be present. The JP1 and JP2 (S0 and S1) jumpers must be set per *Table 2* to match the expected character-rate clock of the data stream.

Local Loopback

Local loopback is a diagnostic mode of the CY9267 that allows the user to establish a link between the SMPTE serial transmitter and the SMPTE serial receiver, without going through a coaxial cable or having the serial signal leave the board. In this mode, the OUTC± differential PECL outputs of the CY7B9234 SMPTE HOTLink Transmitter are directly connected to the INB± inputs of the CY7B9334 SMPTE HOTLink

Receiver. The cable driver and cable equalizer are not utilized and no coaxial cable is needed.

To operate in this mode JP3, JP4, JP5, and JP6 must be present. The JP1 and JP2 jumpers must be set per *Table 2* to match the expected character-rate clock of the received serial-video stream.

Bypass

Bypass is a diagnostic mode that can operate in conjunction with any of the previously described modes. In Bypass mode, the parallel data is routed around the SMPTE scrambler/descrambler and the encoder/decoder. The 10-bit parallel data is passed unchanged from its original state. This allows the devices to pass user defined data that is not SMPTE 259M compliant. It also permits the SMPTE HOTLink devices to be tested for run lengths in excess of those found in normal SMPTE serial streams.

Bypass mode is enabled by removing the JP4 (bypass) jumper. The settings of other jumpers remain as described in the alternate modes.

Schematics and Parts List

The complete schematic for the CY9267 SMPTE evaluation board is shown in *Figures 6* through *13*. Artwork for all board layers and silkscreens are shown in *Figures 14* through *19*. A complete parts list for the assembled board is shown in *Table 4*.

References

1. *Television—10-Bit 4:2:2 Component and 4f_{SC} Composite Digital Signals- Serial Digital Interface*, ANSI/SMPTE 259M-1997, Society of Motion Picture and Television Engineers, 1997
2. *Television—Component Video Signal 4:2:2-Bit-Parallel Digital Interface*, ANSI/SMPTE 125M-1995, Society of Motion Picture and Television Engineers, 1995
3. *Television—System M/NTSC Composite Video Signals-Bit-Parallel Digital Interface*, ANSI/SMPTE 244M-1995, Society of Motion Picture and Television Engineers, 1995
4. *Cypress HOTLink User's Guide*, Cypress Semiconductor Corporation, 1995
5. *Cypress CY7B9234/9334 SMPTE HOTLink Data Sheet*, Cypress Semiconductor Corporation, 1997
6. *Cypress CY7C9235 SMPTE 259M/DVB-ASI Scrambler-Controller Data Sheet*, Cypress Semiconductor Corporation, 1997
7. *Cypress CY7C9335 SMPTE 259M/DVB-ASI Descrambler/Framer-Controller Data Sheet*, Cypress Semiconductor Corporation, 1997

Table 4. CY9267 SMPTE Evaluation Board - Part List

Instance	Part Number	Description
U1	Motorola MC100ELT25	Differential ECL - TTL Translator
U2	Motorola MC100ELT24	TTL-Differential ECL Translator
U3	Cypress CY101E383	ECL/TTL/ECL Translator
U4	Cypress 74FCT825CT	10-Bit Bus Interface Register
U5	Cypress CY7C9335	SMPTE Decoder/Framer
U6	IC74F04	Hex Inverter
U7	Cypress CY7C9235	SMPTE Encoder
U8	Cypress CY7B9334-400	SMPTE HOTLink Receiver
U9	Cypress CY2907	General Purpose Clock Generator
U10	Epson MA-506 12.000 MHz	12.000 MHz Surface Mount Quartz Crystal
U11	N/A	N/A
U12	Cypress CY7B9234-400	SMPTE HOTLink Transmitter
U13	Comlinear CLC014	Adaptive Cable Equalizer
U14, U15	Comlinear CLC007	Serial Cable Driver
D1	DL4148-ND Switching Diode	Diode
RN1, RN2	CTS9350	270 Ohm Resistor Network-SOIC
RN3, RN4	CTS9213	100 Ohm Resistor Network-SOIC
J1, J2		Female 25-pin D-sub Connector
J3		6-pin PC Power Connector
J4, J5		12 pin Header Array
J6		3-Pole Terminal Block
J7, J8, J9, J10		75 Ohm BNC Female BNC Connector
R1, R2, R15, R16, R21, R23, R24, R28	75Ω 1/8W, 1%	1206 Chip Resistor
R3, R4, R9	330Ω 1/8W, 5%	1206 Chip Resistor
R5, R6, R7, R8, R10, R11	1KΩ 1/8W, 5%	1206 Chip Resistor
R12, R25	107Ω 1/8W, 1%	1206 Chip Resistor
R13, R14, R26, R27	51.1Ω 1/8W, 1%	1206 Chip Resistor
R17, R18	270Ω 1/8W, 5%	1206 Chip Resistor
R19, R20	100Ω 1/8W, 5%	1206 Chip Resistor
R22	37.4Ω 1/8W, 1%	1206 Chip Resistor

Table 4. CY9267 SMPTE Evaluation Board - Part List (continued)

Instance	Part Number	Description
C1, C2, C3, C5, C6, C7, C8, C9, C11, C12, C13, C14, C15, C16, C17, C18, C20, C21,C24, C25, C31	0.01 µF	1206 X7R Chip Capacitor
C10,C19, C4, C32	22 µF	1206 Tantalum Capacitor
C22, C33, C23, C26, C27,C29, C30, C34	0.1 µF	1206 X7R Chip Capacitor
C28	100 pF	1206 C0G Chip Capacitor
C35	2 pF	0805 Chip Capacitor

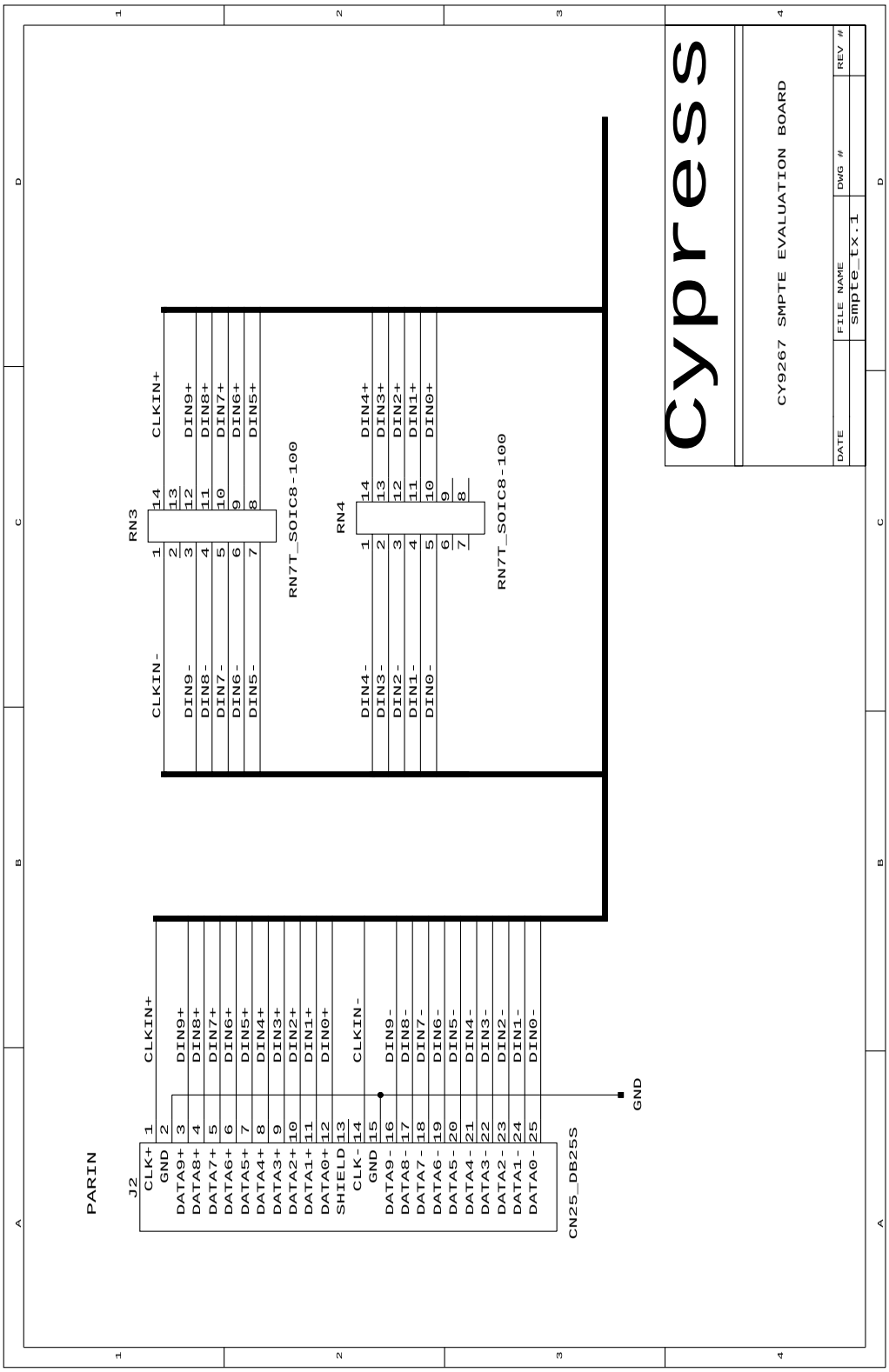

Figure 6. Schematic of CY9267 (sheet 1 of 8)

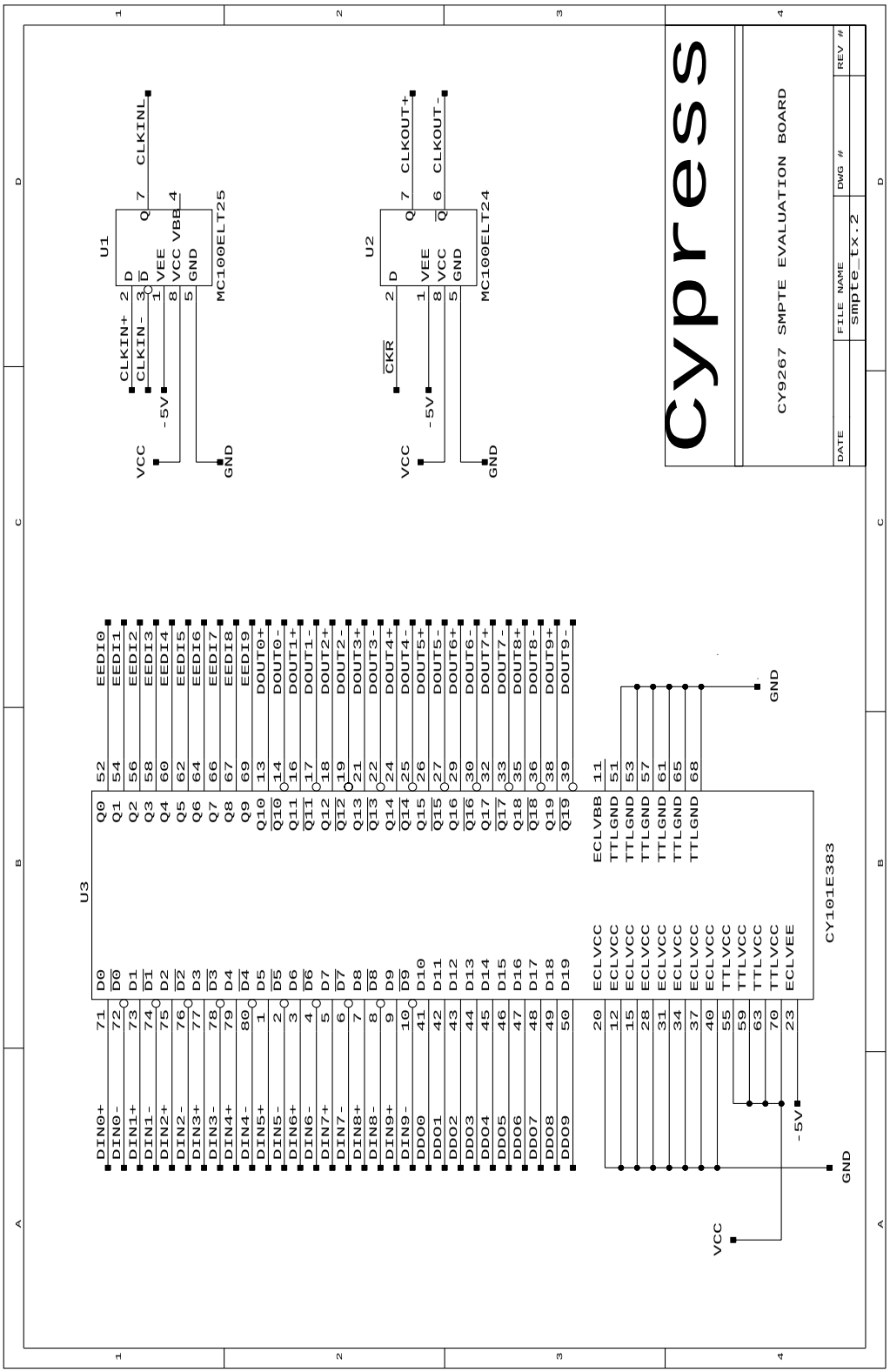

Figure 7. Schematic of CY9267 (sheet 2 of 8)

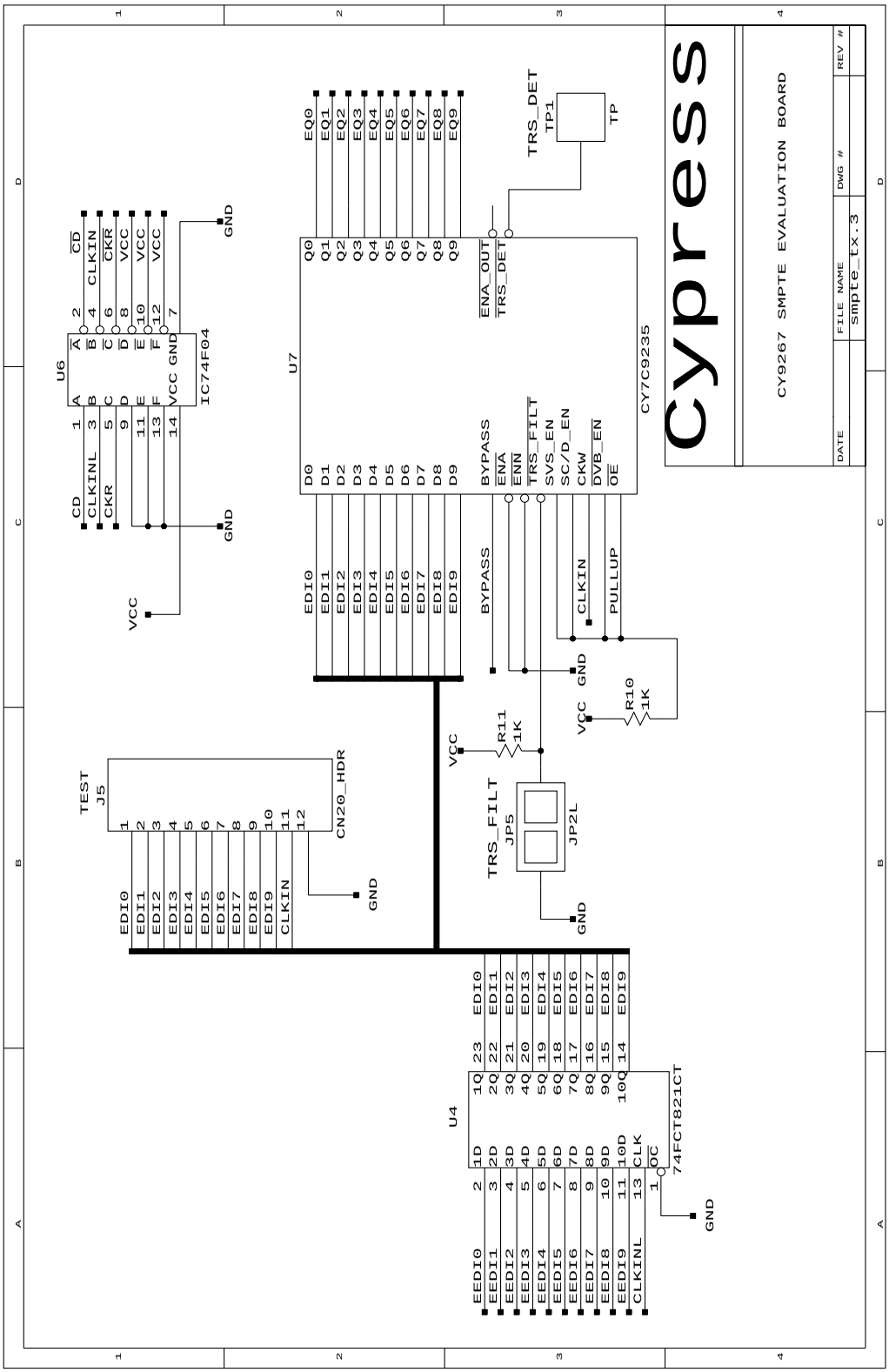

Figure 8. Schematic of CY9267 (sheet 3 of 8)

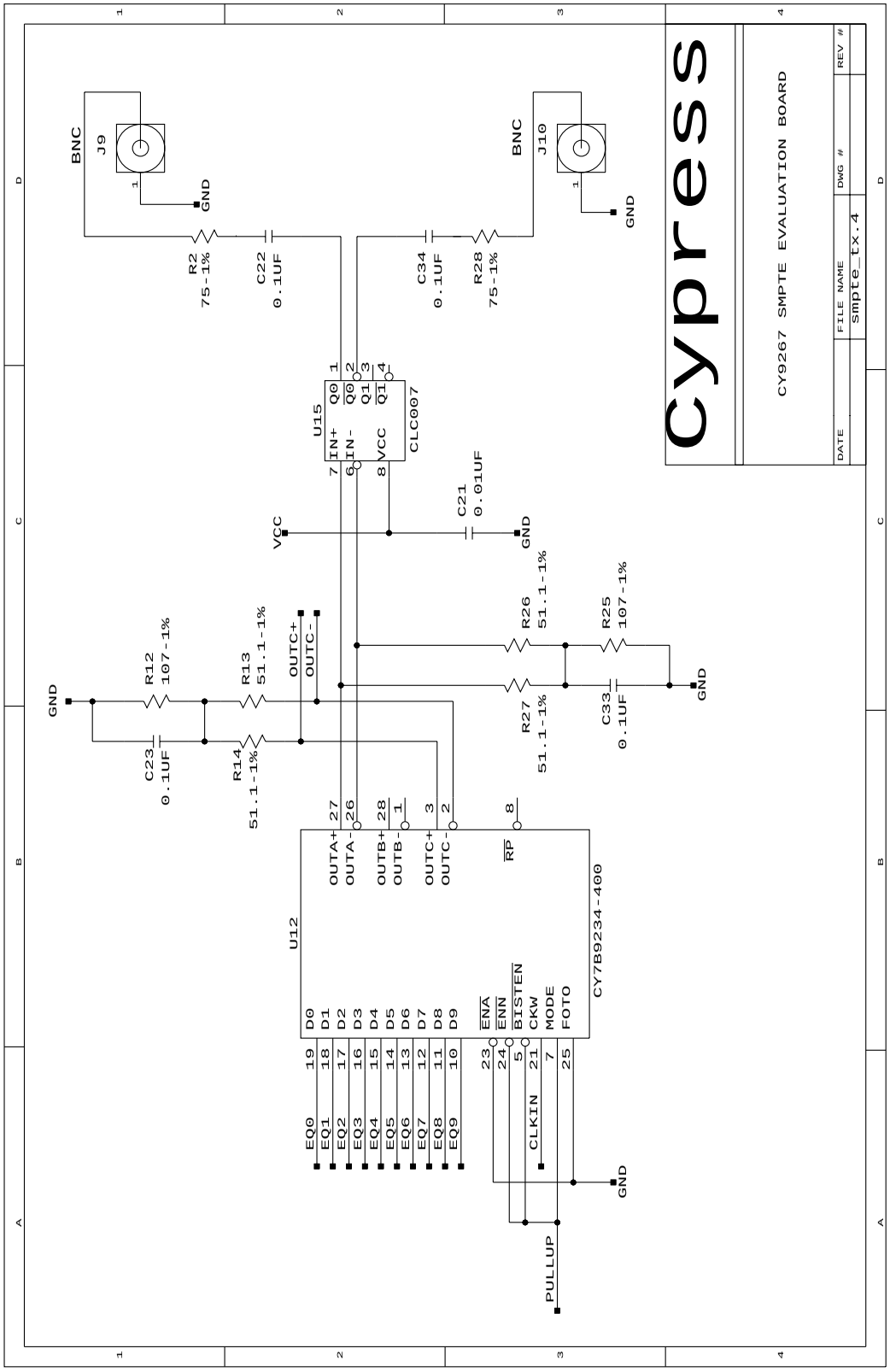

Figure 9. Schematic of CY9267 (sheet 4 of 8)

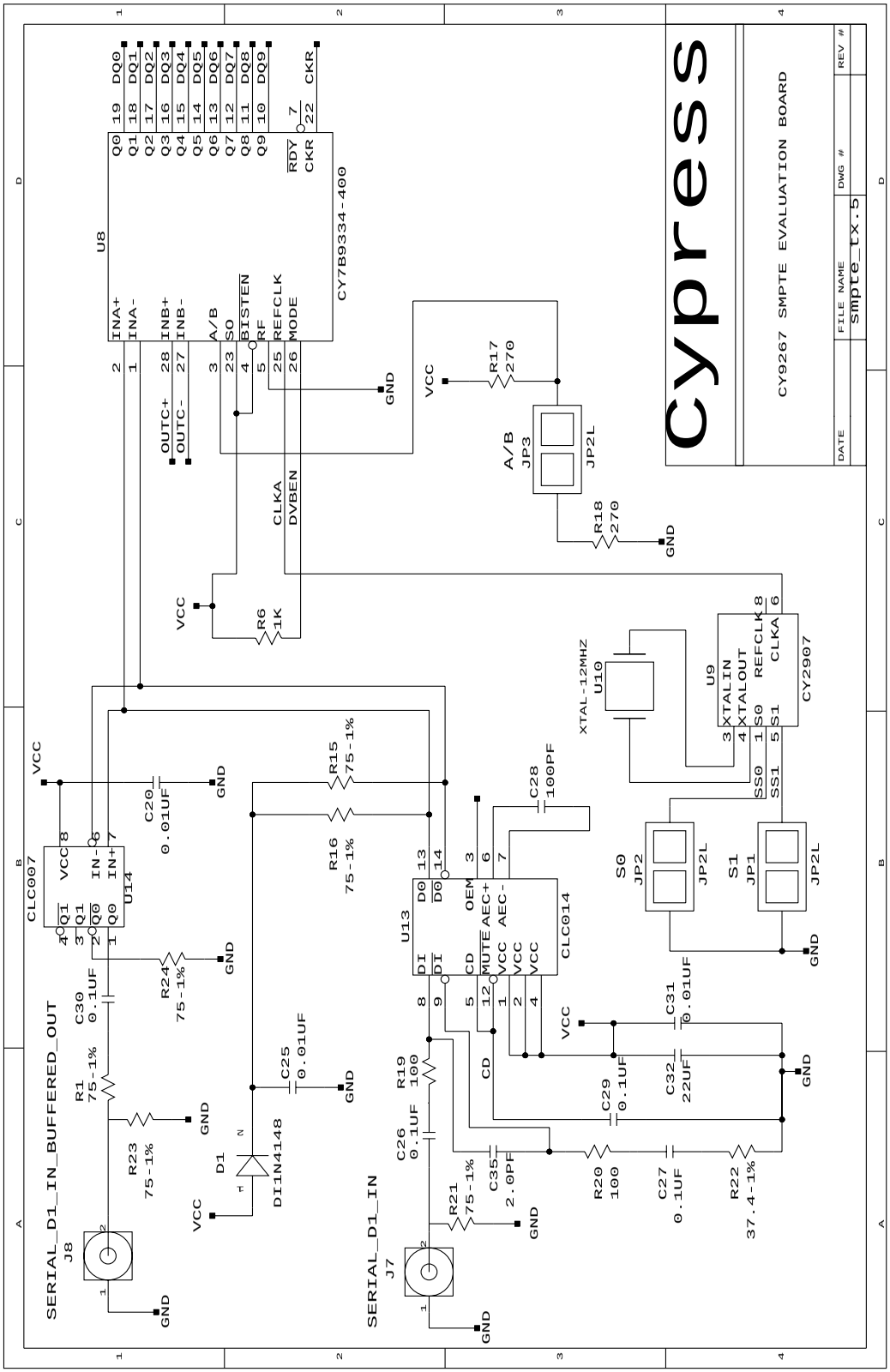

Figure 10. Schematic of CY9267 (sheet 5 of 8)

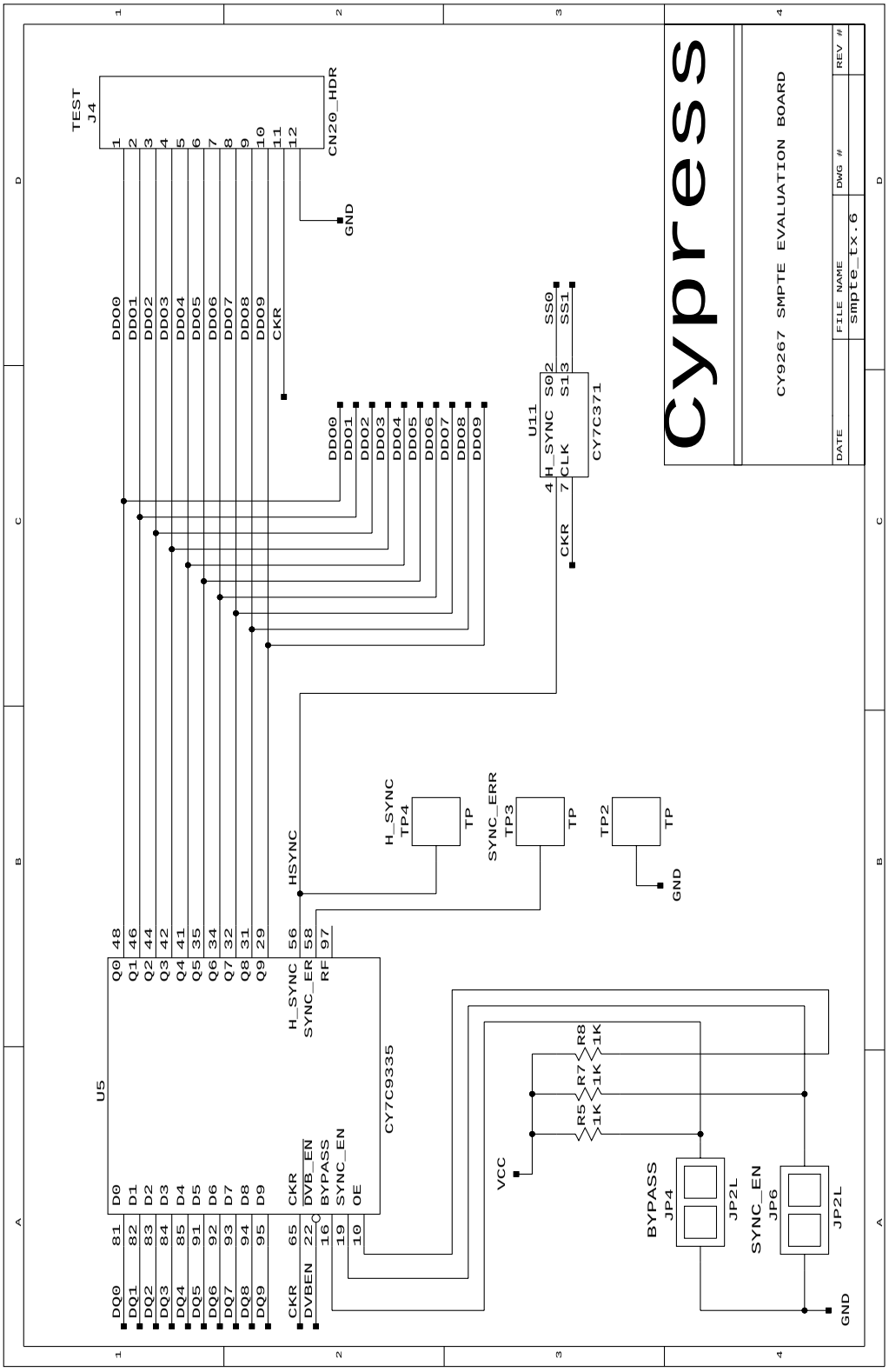

Figure 11. Schematic of CY9267 (sheet 6 of 8)

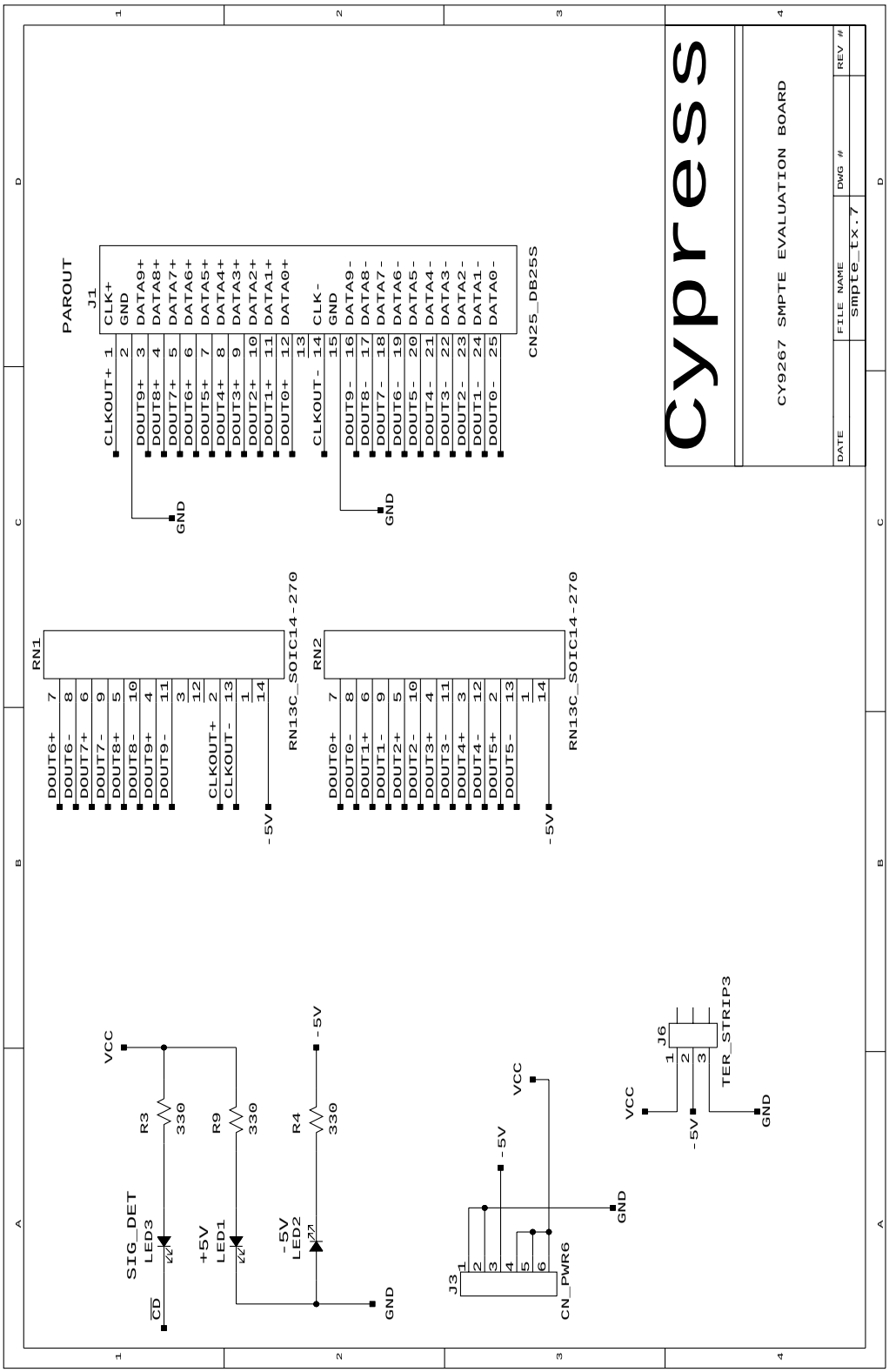

Figure 12. Schematic of CY9267 (sheet 7 of 8)

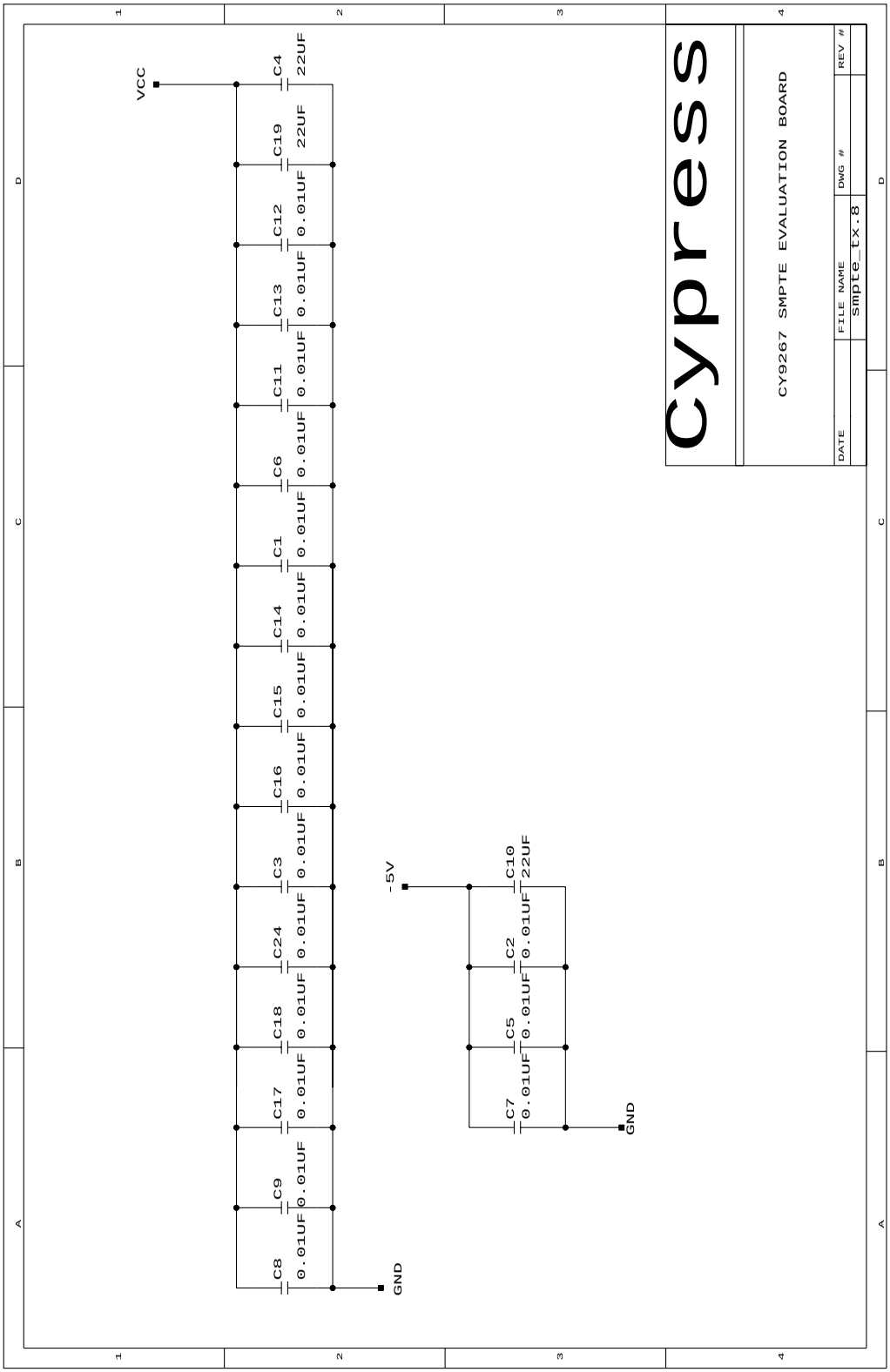

Figure 13. Schematic of CY9267 (sheet 8 of 8)

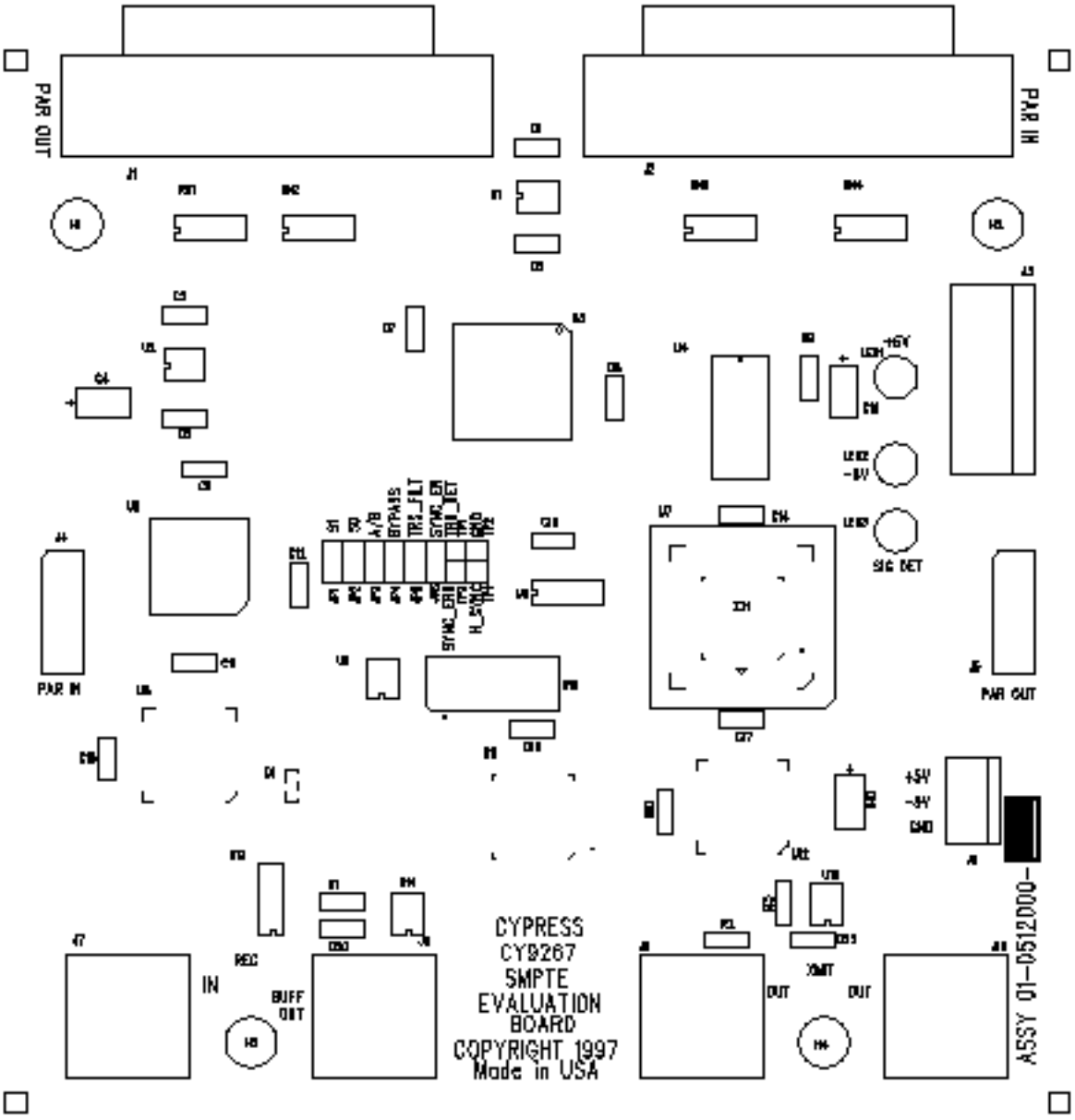

Figure 14. Top Layer Silkscreen (sheet 1 of 6)

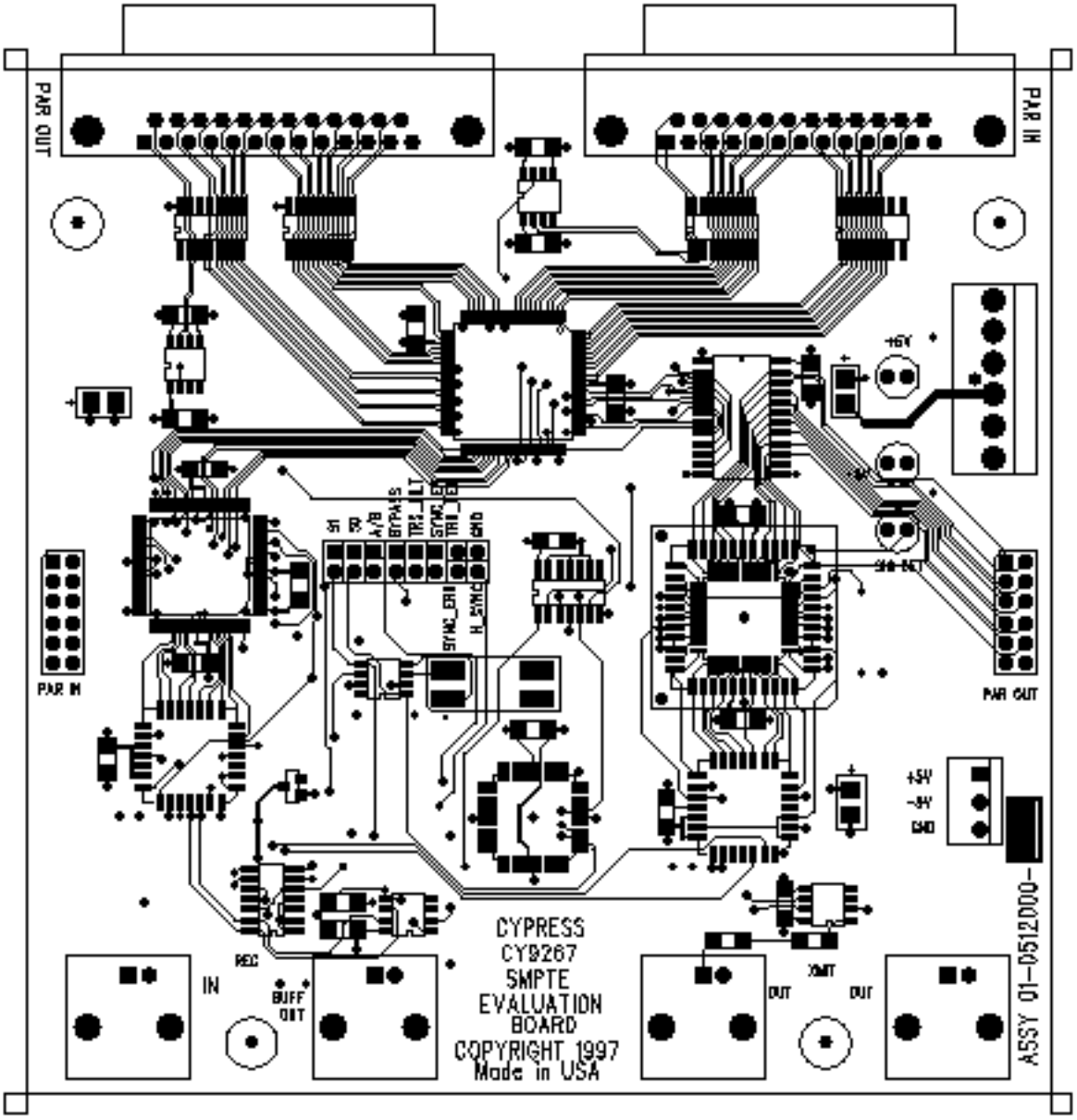

Figure 15. Top Layer Traces and Silkscreen (sheet 2 of 6)

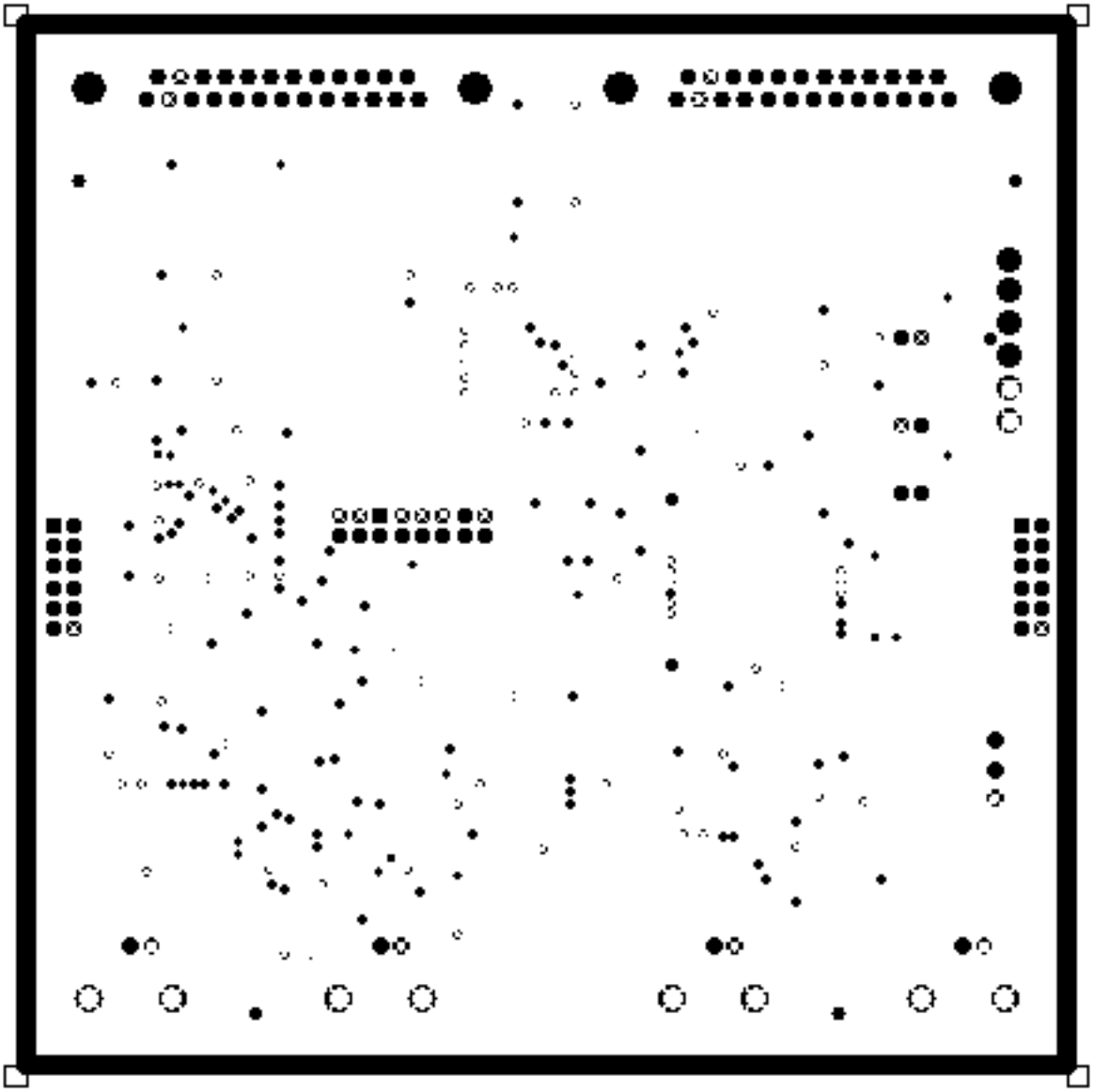

Figure 16. Ground Layer (sheet 3 of 6)

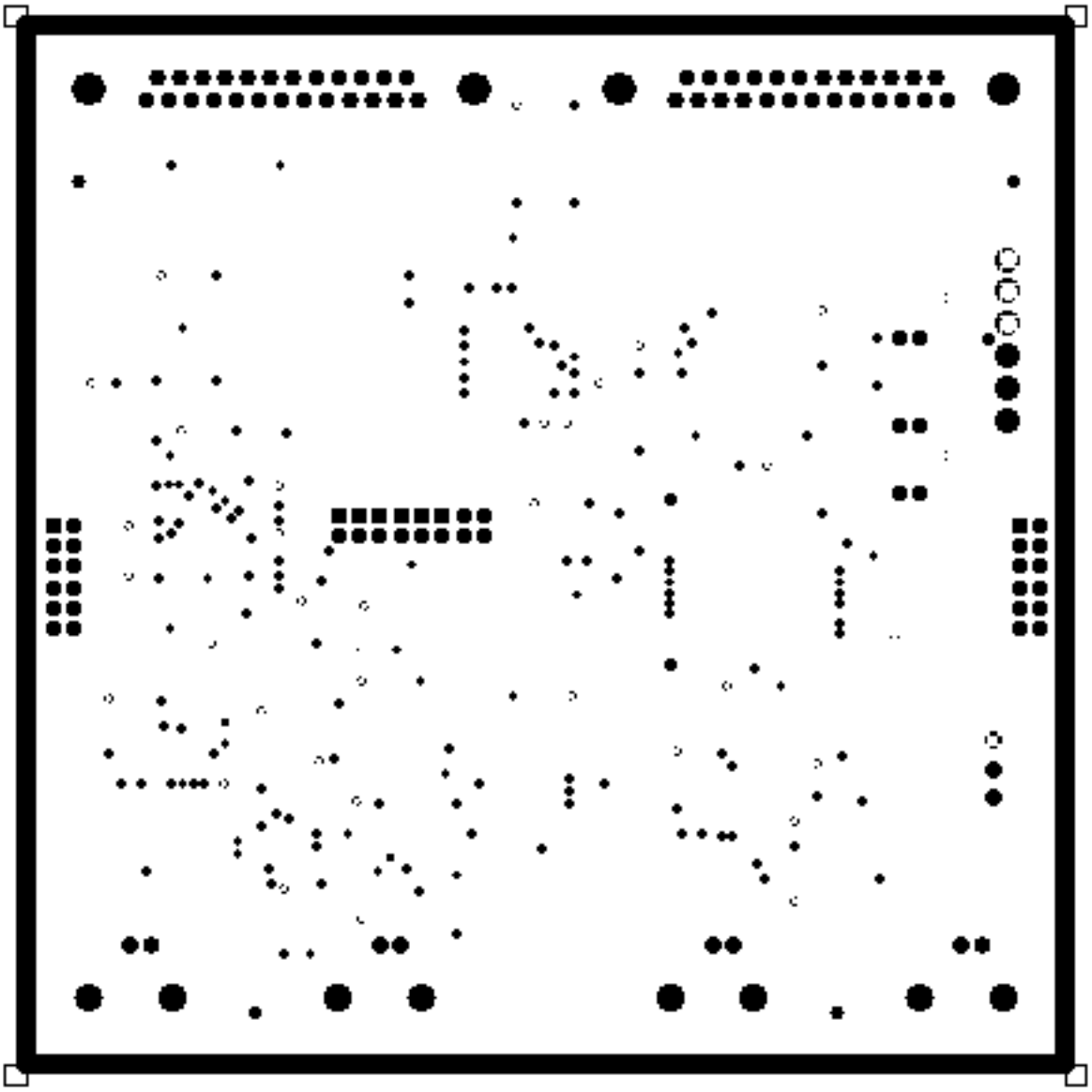

Figure 17. Power Layer (sheet 4 of 6)

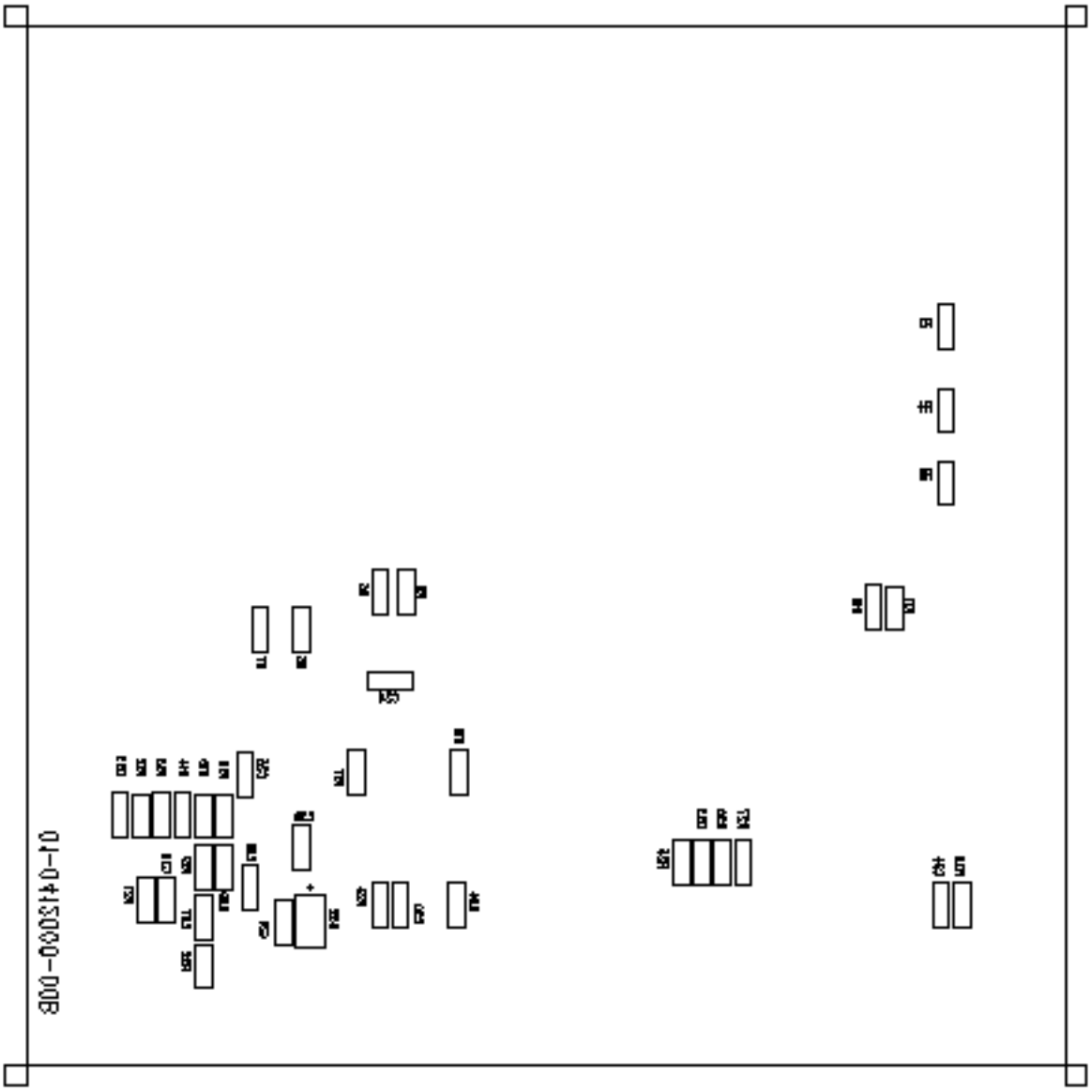

Figure 18. Bottom Layer Silkscreen (sheet 5 of 6)

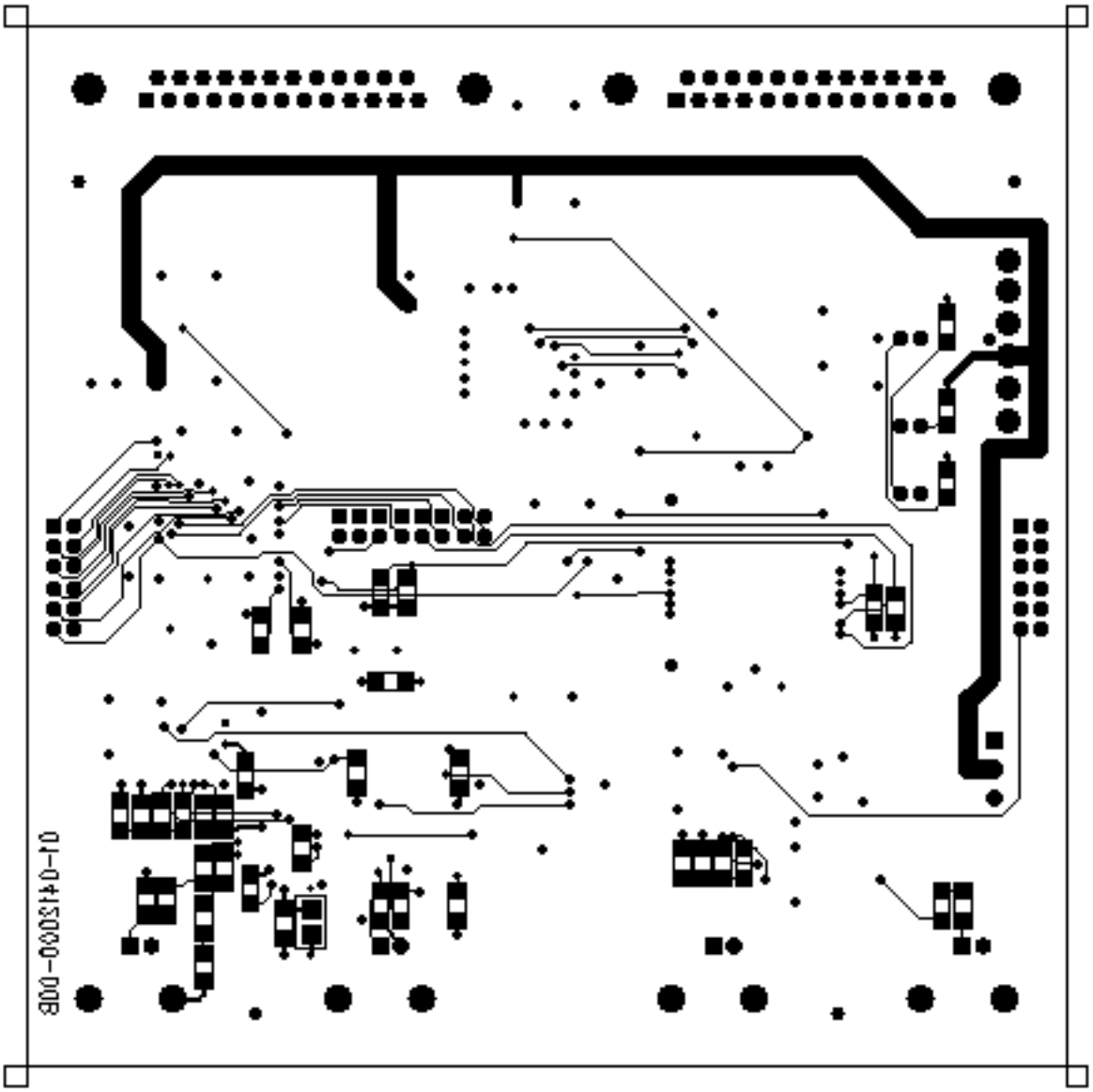

Figure 19. Bottom Layer (sheet 6 of 6)