Connecting CY7B951/CY7B952 to 3.3V Framers

Overview

This document describes how to connect the 5V PECL outputs of the CY7B951 or CY7B952 to 3.3V PECL inputs, and also how to connect the 5V PECL inputs of the CY7B951 or CY7B952 to 3.3V PECL outputs of some framer chips. CY7B951 and CY7B952 are clock and data recovery chips for 155.52-Mbps and 51.84-Mbps signals.

TSER± Connection

The PECL inputs of the CY7B951 or CY7B952 has a minimum V_{ILE} specification of 2V. If either Rin+ or Rin– of the differential pair is above 2V, the input buffer circuit will operate correctly. *Figure 1a* shows a set-up that will interface the 3.3V PECL output to the Tser± input of the CY7B951 and CY7B952. The 3-resistor Totem Pole arrangement allows the framer output to shift up in voltage level. This set-up provides enough margin so that 5% resistors are adequate.

In this set-up, the output of the framer is correctly biased at:

$$V_{term} = \frac{3.3V \times 100}{100 + 39 + 68} = 1.61V \quad \text{Eq. 1}$$

and the input to Rin± is correctly biased at:

$$V_{term} = \frac{3.3V \times (100 + 39)}{100 + 39 + 68} = 2.22V \quad \text{Eq. 2}$$

The framer output will swing from 1.61V to 2.4V. This 0.79V differential swing of the 3.3V PECL framer will be reduced because of the potential-dividing effect of the level-shifter:

$$V_{swing} = \frac{790mV \times 68}{39 + 68} = 502mV \quad \text{Eq. 3}$$

Since V_{swing} is bigger than the 50mV minimum V_{diff} requirement of the CY7B951 and CY7B952, this set-up will work.

RCLK±, RSER±, and TCLK± Connections

The CY7B951 and the CY7B952 PECL outputs have to be biased to Vcc – 2V. The 3.3V PECL inputs of the framer chip are best to see a PECL cross-over at 2.05V. *Figure 1b* shows the set-up for interfacing the two chips.

In this set-up, the PECL outputs of the CY7B951 and CY7B952 are correctly biased at:

$$V_{term} = \frac{5V \times (56 + 75)}{82 + 56 + 75} = 3.08V \quad \text{Eq. 4}$$

The PECL cross-over point as seen by the 3.3V PECL chip is the down-shifted version of the CY7B951 and CY7B952 PECL cross-over point which is typically at (Vcc – 1.33V):

$$V_{crossover} = \frac{(5V - 1.33V) \times 75}{56 + 75} = 2.1V \quad \text{Eq. 5}$$

The 0.8V differential Swing of the CY7B951 and CY7B952 PECL outputs will be reduced to:

$$V_{swing} = \frac{800mV \times 75}{56 + 75} = 458mV \quad \text{Eq. 6}$$

Since this is bigger than the 200-mV minimum V_{diff} requirement of most framer chips, this set-up will work.

General Layout Recommendations

In additional to the above 5V PECL to 3.3V PECL biasing scheme, the following layout recommendation schemes should also be followed to guarantee correct operation of the clock and data recovery device.

1. Tie all three Vcc together on the COMPONENT side of the board. A low inductive path between the three Vcc pins is essential to the operation of the device. There should NOT be any via in series with the Vcc path between pin 6, 18, and 20 of the CY7B951 and CY7B952.

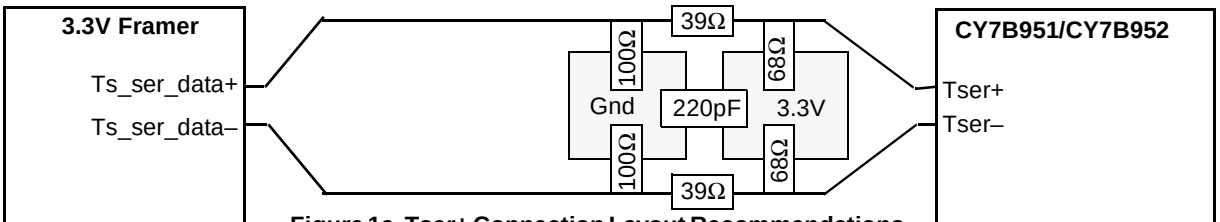

Figure 1a. Tser± Connection Layout Recommendations

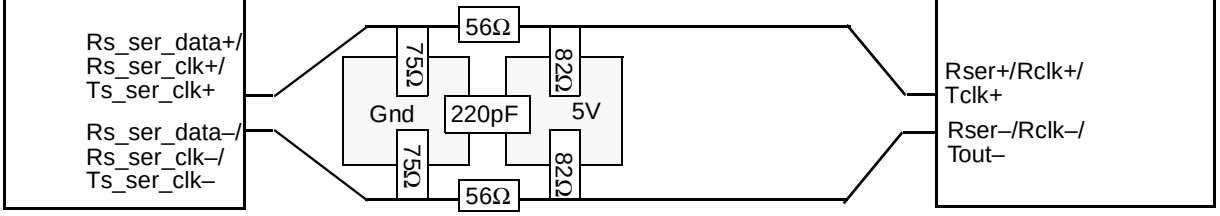

Figure 1b. Rclk±, Rser±, and Tclk± Connections Layout Recommendations

2. Use at least a 220-pF and a 0.1-μF capacitor to bypass high frequency noise and to satisfy the device's instantaneous current needs.
3. Termination /biasing resistors should be placed as close to the terminating side as possible to absorb reflections.