Protection, Decoupling, and Filtering of Cypress CMOS Circuits

This application note explains how to protect your ICs with a low-cost zener diode and why it is good insurance against inadvertent voltage transients. Also explained is the reason why decoupling and high-frequency-filtering capacitors are required. A method is provided for determining the capacitors' values.

Zener Diode Protection

Linear power supplies can cause large voltage transients. The transient is negative when it is caused by the collapse of a magnetic field and is positive when the supply is turned on.

Some commercially available laboratory bench supplies behave the same way. When they turn on, they can overshoot several volts. When they turn off, lead inductance can cause a negative transient voltage at the V_{CC} pin. If there is enough energy, this inductance can break down internal gate oxides, destroying or weakening the IC to the extent that it might fail later.

You can avoid this problem by adding a 20¢ zener diode (also called a voltage-regulator diode) between V_{CC} and ground. Connect the diode's cathode to V_{CC} and the anode to ground (see *Figure 1*). A 400-mW, 6.2V 1N525 or equivalent is recommended. You can also use the 1N753, a 500-mW, 6.2V zener diode.

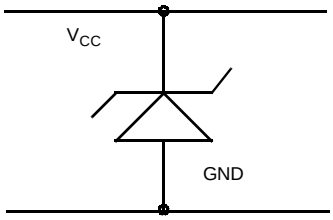

Figure 1. Zener Diode Connection

If a voltage greater than the zener voltage (6.2V) occurs on V_{CC}, the diode breaks down, clamping the voltage to 6.2V and shunting the current to ground (see *Figure 2*). The diode can be destroyed if the current multiplied by the zener voltage exceeds the diode's power rating. Because zener diodes *always* fail shorted, they cause the power supply to "crowbar" and thus protect the ICs.

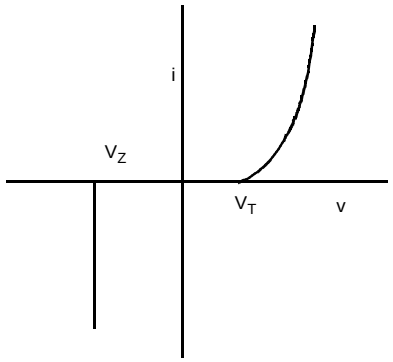

Figure 2. Zener Diode Characteristic

A negative voltage on the V_{CC} line puts a forward bias on the diode. This turns on the diode, which clamps the voltage to approximately –0.8V. If the negative voltage multiplied by the current exceeds the diode's power rating, the diode fails shorted, as in the reversed-bias case, and protects the ICs.

High-Frequency Filtering

In addition to the protection offered by zener diodes, decoupling and high-frequency filter capacitors are required on high-performance CMOS circuits. To use these capacitors effectively, you must understand why they are required.

To realize the fast rise and fall times that Cypress CMOS integrated circuits are capable of achieving, the power-distribution system must be able to supply the instantaneous current required when the device outputs switch from LOW to HIGH. The energy converted to current is stored as charge on the local decoupling capacitors. They decouple or isolate the circuit from the power-distribution system. It is standard practice to use one decoupling capacitor for each IC that drives a transmission line and one capacitor for every three devices that do not.

The PCB trace inductance plus the IC lead inductance can "current-starve" the output circuits, causing rise-time degradation. Remember that the current through an inductor cannot change instantaneously. Therefore, you must minimize any series inductance, including the lead inductance of the decoupling capacitors.

Decoupling-Capacitor Calculations

To determine the value of the decoupling capacitor, you must estimate the instantaneous current required when all the outputs of an IC switch from LOW to HIGH, assuming a reasonable droop of the voltage on the capacitor. The charge stored on the local decoupling capacitor is

$Q = CV$

Differentiating yields

$$i(t) = \frac{dQ}{dt} = C\frac{dV}{dt} \quad \text{Eq. 1}$$

The characteristic impedance of a typical transmission line is 50Ω. Lines with a heavy capacitive load have lower characteristic impedances.

Next, assume that the IC is a nine-output FIFO, such as the CY7C429. The outputs reach

$V_{CC} - V_t = 5V - 1V = 4V$

Each output requires 4V/50Ω = 80 mA. Because the FIFO has nine outputs, it requires a total of 720 mA during the rise times of the outputs.

Solving *Equation 1* for C yields

$$C = i\frac{dt}{dv} \quad \text{Eq. 2}$$

The last step is to assume a reasonable, tolerable droop in the capacitor voltage. Assume dV = 100 mV. Additionally, the signal rise and fall times are 2 ns. Substituting these values in *Equation 2* yields

$$= \frac{720 \times 10^{-3} \times 2 \times 10^{-9}}{100 \times 10^{-3}}$$

$$14.4 \times 10^{-9}$$

$$0.0144\mu F$$

It is standard practice to use 0.01 to 0.1-µF decoupling capacitors. A 0.1-µF capacitor can supply 5A under the conditions assumed in the preceding calculations. Another way to look at the situation is that a 0.1-µF capacitor supplies 720 mA of instantaneous current in 2 ns with only 14.4 mV of voltage droop across the capacitor.

Decoupling capacitors for high-speed Cypress CMOS circuits should be of the high-K ceramic type with a low Effective Series Resistance (ESR). Capacitors using Z5U dielectric are a good choice.

High-Frequency Filter Capacitors

The 0.1 to 0.01-µF decoupling capacitors usually do not provide high-frequency decoupling or filtering. These capacitors do not behave like capacitors at high frequencies because their series resonance frequency is not high enough. This is primarily because of lead inductance in their construction, which is a result of the capacitor's relatively large value.

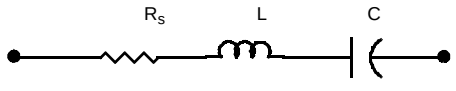

Figure 3. Simplified Capacitor Equivalent Circuit

For high-frequency filter analysis, you can use the simplified capacitor equivalent circuit shown in *Figure 3*. R_S is the ESR, L is the Effective Series Inductance (ESL), and C is the capacitance.

The impedance of the simplified equivalent circuit is:

$$Z_c = R_s + j\omega L + \frac{1}{j\omega C} \quad \text{Eq. 3}$$

$$Z_c = R_s + j\left[\omega L - \frac{1}{\omega C}\right] \quad \text{Eq. 4}$$

The magnitude of the impedance is

$$Z_c = \sqrt{R_s^2 + \left[\omega L - \frac{1}{\omega C}\right]^2} \quad \text{Eq. 5}$$

At the series resonant frequency:

$$\omega L = \frac{1}{\omega C}$$

or,

$$\omega = \frac{1}{\sqrt{LC}}$$

At the resonant frequency, $Z_c = R_S$, which is the minimum impedance.

Figure 4 shows how the impedance varies with frequency. The series resistance usually increases as the capacitance decreases. Also, as the capacitance decreases, the inductance typically decreases, which means that the resonant frequency increases. This is usually due to the capacitor's physical construction. Note that a surface-mounted capacitor's lead inductance is at least an order of magnitude less than that of an axial-lead capacitor.

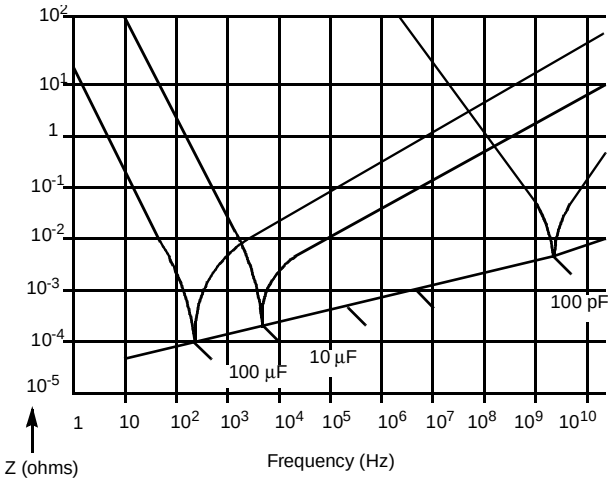

Figure 4. Capacitor Impedance Versus Frequency

The next step in high-frequency filter analysis is to determine a typical system's expected high-frequency components. Begin by assuming that the circuit is driven by a series of digital pulses with finite rise and fall times, then perform a Fourier transform on the series to determine their frequency components.

Fourier Transform of a Periodic Pulse

Figure 5 illustrates a periodic pulse of amplitude A, period T, rise and fall times of t_r, and pulse width of T_p, as measured between the 50-percent-amplitude points.

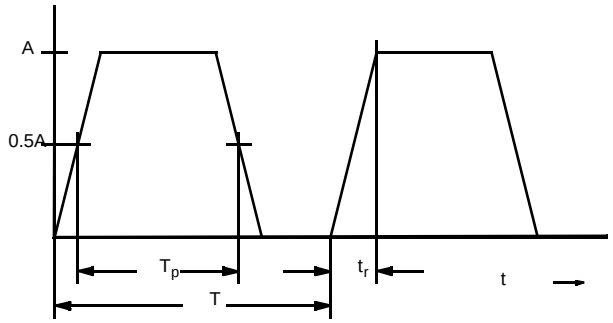

Figure 5. Periodic Pulse Waveform

The approximate frequency-domain transform appears in *Figure 6*. The amplitude of the frequency-domain voltage is a function of the signal's amplitude and duty cycle in the time domain. The fundamental frequency, F_0, is related to the pulse train's period. The first harmonic, F_1, is of equal energy and is a function of the pulse width. The second harmonic, F_2, contains half the energy of F_0 and is a function of the pulse rise time.

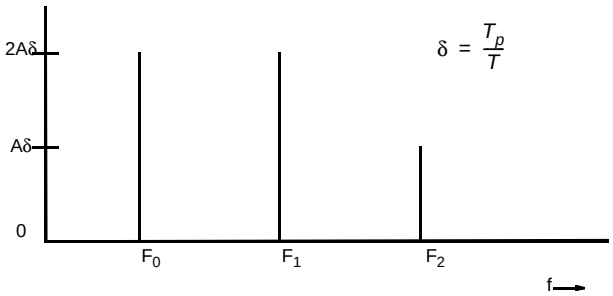

Figure 6. Fourier Transform of Periodic Pulse

The rise and fall times of Cypress's CMOS and BiCMOS circuits are 2 ns, by design. If a Cypress PLD is driving the write- or read-strobe inputs of a CY7C429-20 FIFO at the maximum frequency of 33.3 MHz (T = 30 ns) with a 10-ns/30-ns duty cycle signal (T_p = 10 ns), the following signal frequencies are generated:

$$F_0 = \frac{1}{\pi T} = \frac{1}{3.1416 \times 30 \times 10^{-9}} = 10.61MHz$$

$$F_1 = \frac{1}{\pi T_p} = \frac{1}{3.1416 \times 10 \times 10^{-9}} = 31.83MHz$$

$$F_2 = \frac{1}{\pi t_r} = \frac{1}{3.1416 \times 2 \times 10^{-9}} = 159.15MHz$$

Within the IC, signal rise and fall times can be as fast as 300 ps (picoseconds), which means that F2 = 1.061 GHz (1,061 MHz). In some ICs short timing pulses are generated internally, but they are usually longer than the 300-ps rise time, so the preceding F2 is the highest harmonic present.

Because the IC's data outputs can normally change no faster than those of the inputs, the outputs do not generate additional higher-frequency harmonics.

Parallel the Filter Capacitors

It will not be possible to find a capacitor with three series resonant frequencies that correspond to F0, F1, and F2. Instead, select one capacitor with a resonant frequency greater than 160 MHz and connect it in parallel with the decoupling capacitor, between V_{CC} and ground, as close to the IC as possible. It will act like a bandpass filter, shunting the unwanted, high frequency signals to ground. The sum of the values of the capacitors should be greater than or equal to the value of capacitance given by *Equation 2*.

The AVX Corporation, Myrtle Beach, South Carolina (803-448-9411), makes a series of "RF/Microwave NPO Capacitors." Their "Ultra Low ESR, 'U' Series" have an ESR of 0.06 Ohm at 500 MHz. A value of 470 pF in the EIA standard size 1210 "chipcap" is recommended. Its series resonant frequency is approximately 180 MHz.

Low-Frequency Filter Capacitors

A solid tantalum capacitor of 10 mF is recommended for every 50 to 100 ICs to reduce power-supply ripple. Place this capacitor as close as physically possible to where the V_{CC} and ground enter the PCB or module.