



Thermal Management and Component Reliability

One of the key variables determining the long-term reliability of an integrated circuit is the junction temperature of the device during operation. Long-term reliability of the semiconductor chip degrades proportionally with increasing temperatures following an exponential function described by the Arrhenius equation of the kinetics of chemical reactions. The

slope of the logarithmic plots is given by the activation energy of the failure mechanisms causing thermally activated wear out of the device (see *Figure 1*).

Typical activation energies for commonly observed failure mechanisms in CMOS devices are shown in *Table 1*.

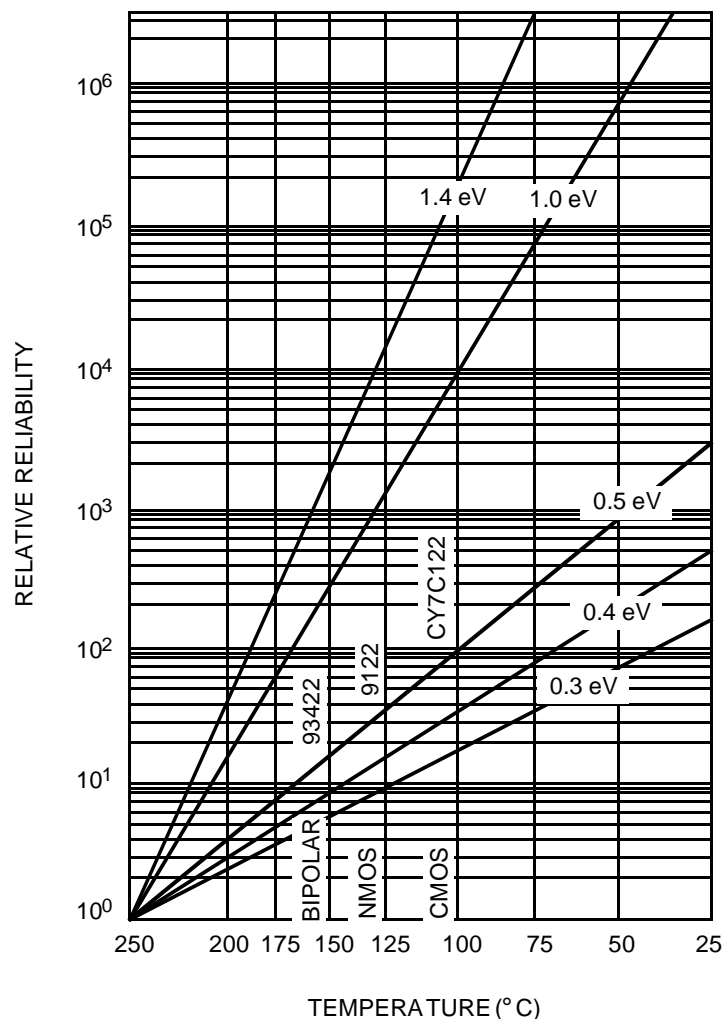


Figure 1. Arrhenius plot, which assumes a failure rate proportional to $\text{EXP}(-E_A/kT)$ where E_A is the activation energy for the particular failure mechanism

Table 1. Failure Mechanisms and Activation Energies in CMOS Devices

Failure Mode	Approximate Activation Energy (Eq)
Oxide Defects	0.3 eV
Silicon Defects	0.3 eV
Electromigration	0.6 eV
Contact Metallurgy	0.9 eV
Surface Charge	0.5-1.0 eV
Slow Trapping	1.0 eV
Plastic Chemistry	1.0 eV
Polarization	1.0 eV
Microcracks	1.3 eV
Contamination	1.4 eV

To reduce thermally activated reliability failures, Cypress Semiconductor has optimized both their low-power-generating CMOS device fabrication process and their high-heat-dissipation packaging capabilities. *Table 2* demonstrates this optimized thermal performance by comparing bipolar, NMOS, and Cypress high-speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions.

Table 2. Thermal Performance of Fast 1K SRAMs in Plastic Packages

Technology	Bipolar	NMOS	Cypress CMOS
Device Number	93422	9122	7C122
Speed (ns)	30	25	25
I _{CC} (mA)	150	110	60
V _{CC} (V)	5.0	5.0	5.0
P _{MAX} (mW)	750	550	300
Package RTH (JA) (°C/W)	120	120	70
Junction Temperature (°C) at Datasheet P _{MAX} [1]	160	136	91

During its normal operation, the Cypress 7C122 device experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0-eV activation energy failure mechanism, this translates into an improvement in excess of two orders of magnitude (100x) over the bipolar 93422 device, and more than one order of magnitude (30x) over the NMOS 9122 device.

Note:

1. T_{ambient} = 70°C

Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

Thermal Resistance (θ_{JA}, θ_{JC})

Thermal resistance is a measure of the ability of a package to transfer the heat generated by the device inside it to the ambient.

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and θ_{JA} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation

$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T_A = Ambient temperature at which the device is operated; Most common standard temperature of operation is room temperature to 70°C.

T_J = Junction temperature of the IC chip.

T_C = Temperature of the case (package).

P = Power at which the device operates.

θ_{JC} = Junction-to-case thermal resistance. This is mainly a function of the thermal properties of the materials constituting the package.

θ_{JA} = Junction-to-ambient thermal resistance. The junction-to-ambient environment is a still-air environment.

θ_{CA} = Case-to-ambient thermal resistance. This is mainly dependent on the surface area available for convection and radiation and the ambient conditions among other factors. This can be controlled at the user end by using heat sinks providing greater surface area and better conduction path or by air or liquid cooling.

Thermal Resistance: Finite Element Model

θ_{JC} and θ_{JA} values given in the following figures and listed in the following tables have been obtained by simulation using the Finite element software ANSYS^[2]. SDRG-IDEAS Pre and Post processor software^[3] was used to create the finite element model of the packages and the ANSYS input data required for analysis.

SEMI Standard (Semiconductor Equipment and Materials International) method SEMI G30-88^[4] states "heat sink" mounting technique to be the "reference" method for θ_{JC} estimation of ceramic packages. Accordingly, θ_{JC} of packages has been obtained by applying the boundary conditions that correspond to the heat sink mounted on the packages in the simulation.

For θ_{JA} evaluation, SEMI standard specification SEMI G38-87 suggests using a package-mounting arrangement that approximates the application environment. So, in evaluating the θ_{JA} , package on-board configuration is assumed.

Model Description

- One quarter of the package is mounted on a FR-4 PC board.
- Leads have been modeled as a continuous metallic plane, and equivalent thermal properties have been used to account for the plastic (or the glass in the case of ceramic packages) that fills the space between the leads.
- 1W power dissipation over the entire chip is assumed.
- 70°C ambient condition is considered.

Comparison of Simulation Data with Measured Data

In the case of ceramic packages, it is not unusual to see significant differences in θ_{JC} values when a heat sink is used in the place of fluid bath.^[5] However, SEMI G30-88 test method recommends the heat sink configuration for θ_{JC} evaluation.

θ_{JA} values from simulation compare within 12 percent of the measured values. θ_{JA} values obtained from simulation seem to be *conservative* with an accuracy of about +12 percent.

Measured values given in Table 3 used the Temperature Sensitive Parameter method described in MIL STD 883C, method 1012.1. The junction-to-ambient measurement was made in a still-air environment where the device was inserted into a low-cost standard-device socket and mounted on a standard 0.062" G10 PC board.

Table 3. 24-Lead Ceramic and Plastic DIPs

Package	Cavity/PAD Size (mils)	θ_{JA} (°C/W)		
		Measured	Simulation	% Diff.
24LCDIP ^[6]	170 x 270	64	67	5
24LPDIP ^[7]	160 x 210	72	82	12

Notes:

2. ANSYS Finite Element Software User Guides
3. SDRG-IDEAS Pre and Post Processor User Guide
4. SEMI International Standards, Vol. 4, Packaging Handbook, 1989.
5. "Thermal resistance measurements and finite calculations for ceramic hermetic packages." James N. Sweet et. al., SEMI-Therm, 1990.
6. 24LCDIP = 24-lead cerDIP
7. 24LPDIP = 24-lead plastic DIP

Thermal Resistance of Packages with Forced Convection Air Flow

One of the methods adopted to cool the packages on PC boards at the system level is to use forced air (fans) specified in linear feet per minute or LFM. This helps reduce the device operating temperature by lowering the case to ambient thermal resistance. Available surface area of the package and the orientation of the package with respect to the air flow affect the reduction of thermal resistance that can be achieved. A general rule of thumb is:

- For plastic packages:
 - 200 LFM air flow can reduce θ_{JA} by 20 to 25%
 - 500 LFM air flow can reduce θ_{JA} by 30 to 40%
- For ceramic packages:
 - 200 LFM air flow can reduce θ_{JA} by 25 to 30%
 - 500 LFM air flow can reduce θ_{JA} by 35 to 45%

If θ_{JA} for a package in still air (no air flow) is known, approximate values of thermal resistance at 200 LFM and 500 LFM can be estimated. For estimation, the factors given in Table 4 can be used as a guideline.

Table 4. Factors for Estimating Thermal Resistance

Package Type	Air Flow Rate (LFM)	Multiplication Factor
Plastic	200	0.77
Plastic	500	0.66
Ceramic	200	0.72
Ceramic	500	0.60

Example:

θ_{JA} for a plastic package in still air is given to be 80°C/W. Using the multiplication factor from Table 4:

- θ_{JA} at 200 LFM is $(80 \times 0.77) = 61.6^\circ\text{C/W}$
- θ_{JA} at 500 LFM is $(80 \times 0.66) = 52.8^\circ\text{C/W}$

θ_{JA} for a ceramic package in still air is given to be 70°C/W. Using Table 4:

- θ_{JA} at 200 LFM is $(70 \times 0.72) = 50.4^\circ\text{C/W}$
- θ_{JA} at 500 LFM is $(70 \times 0.60) = 42.0^\circ\text{C/W}$

Presentation of Data

The following figures and tables present the data taken using the aforementioned procedures. The thermal resistance values of Cypress standard packages are graphically illustrated in *Figure 2* through *6*. Each envelope represents a spread of typical Cypress integrated circuit chip sizes (upper boundary=5000 mils², lower boundary = 100,000 mils²) in their thermally optimized packaging environments. These graphs should be used in conjunction with *Table 10*, which lists the die sizes of Cypress devices.

Table 5 through *9* give the thermal resistance values for other package types not included in the graphs. The letter in the header (*D*, *P*, *J*, etc.) of these tables refer to the package designators as detailed in the Package Diagrams section of this catalog. The numeric values given in the table (e.g., 20.3) refer to the lead count (20) and package width in inches (.3).

If no decimal appears, the reader must refer to the package diagrams.

Packaging Materials

Cypress plastic packages incorporate

- High thermal conductivity copper lead frame
- Molding compound with high thermal conductivity
- Gold bond wires

Cypress cerDIP packages incorporate

- High conductivity alumina substrates
- Silver-filled glass as die attach material
- Alloy 42-lead frame
- Aluminum bond wires
- Silver-filled conductive epoxy as die attach material

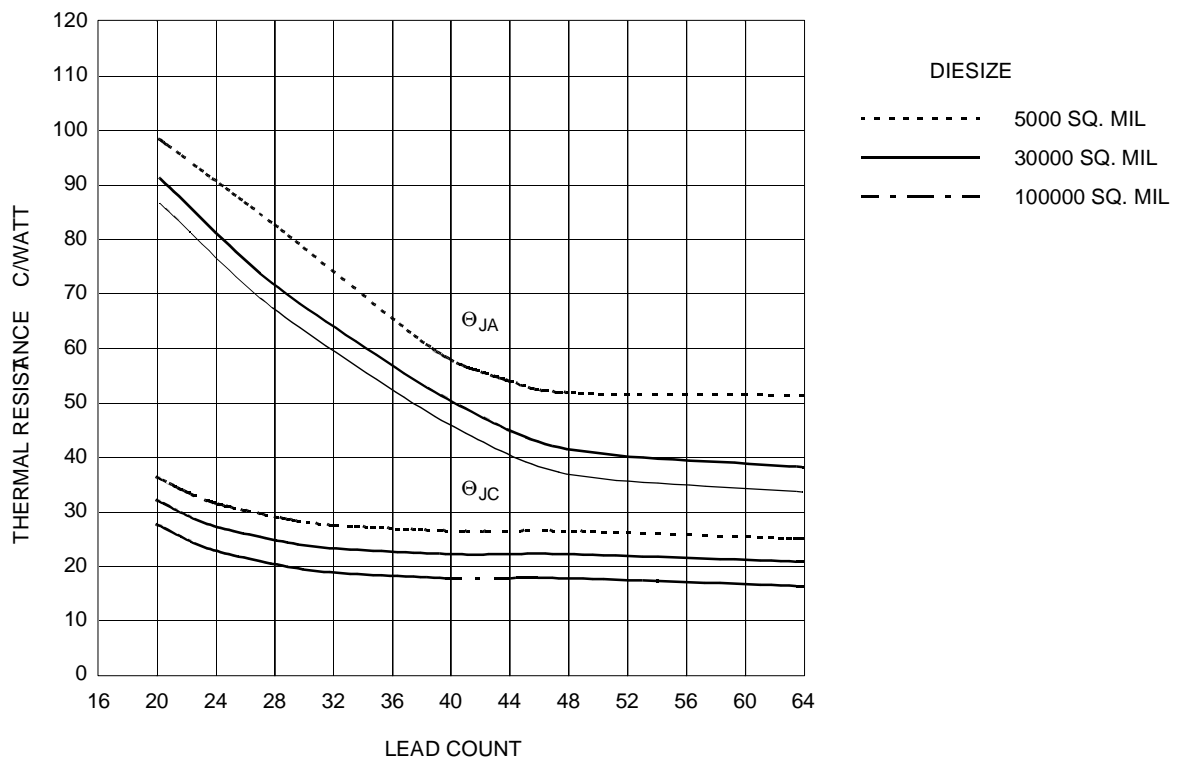


Figure 2. Thermal Resistance of Cypress Plastic DIPs (Package type "P")

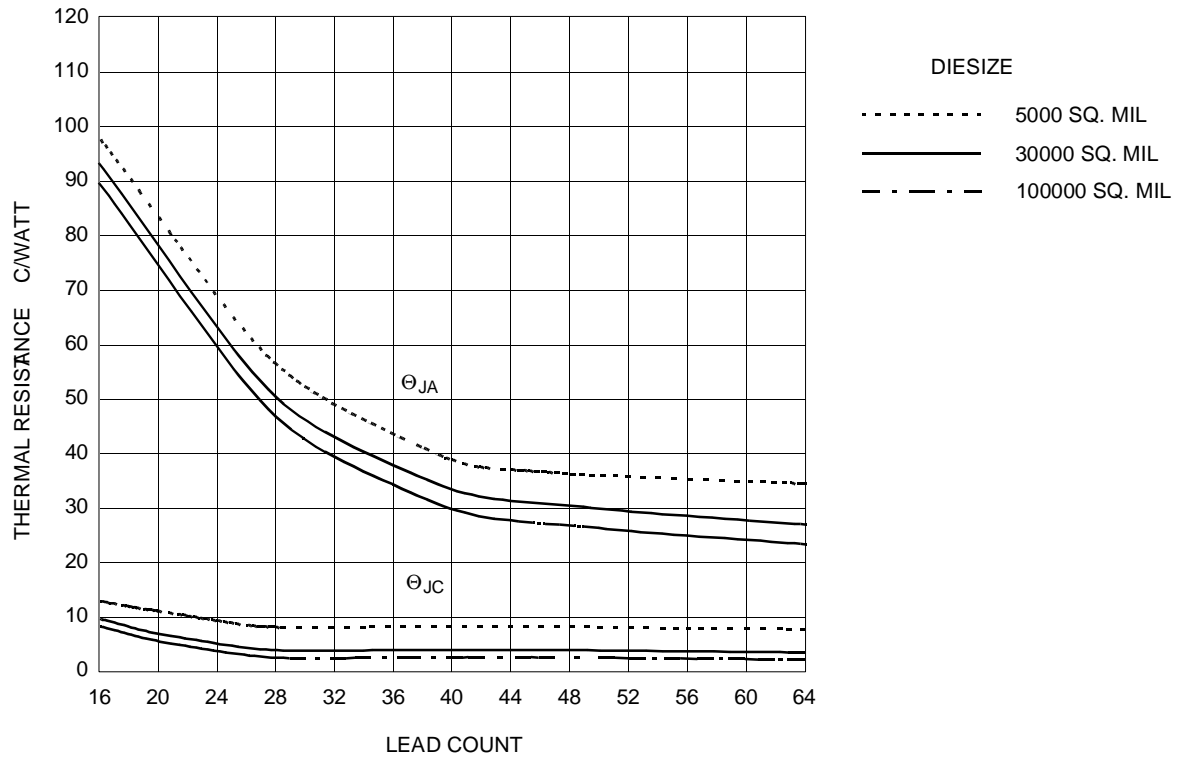


Figure 3. Thermal Resistance of Cypress Ceramic DIPs (Package type "D" and "W")

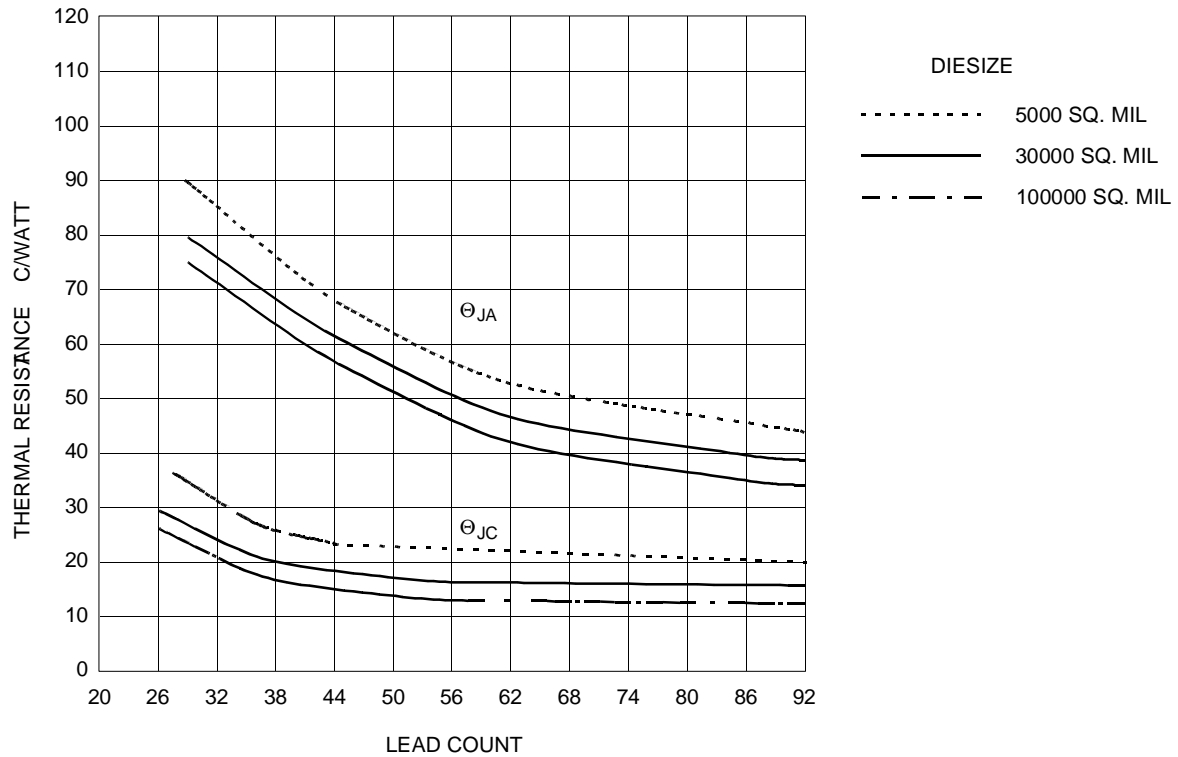


Figure 4. Thermal Resistance of Cypress PLCCs (Package type "J")

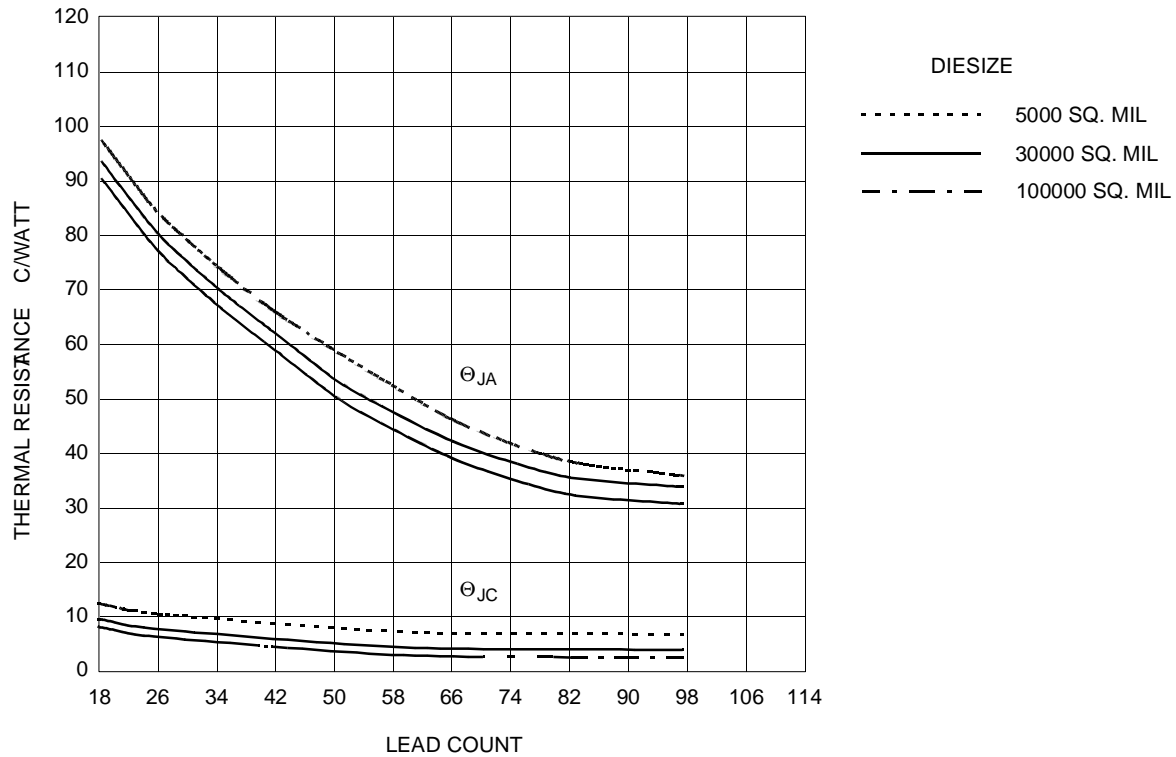


Figure 5. Thermal Resistance of Cypress LCCs (Package type "L" and "Q")

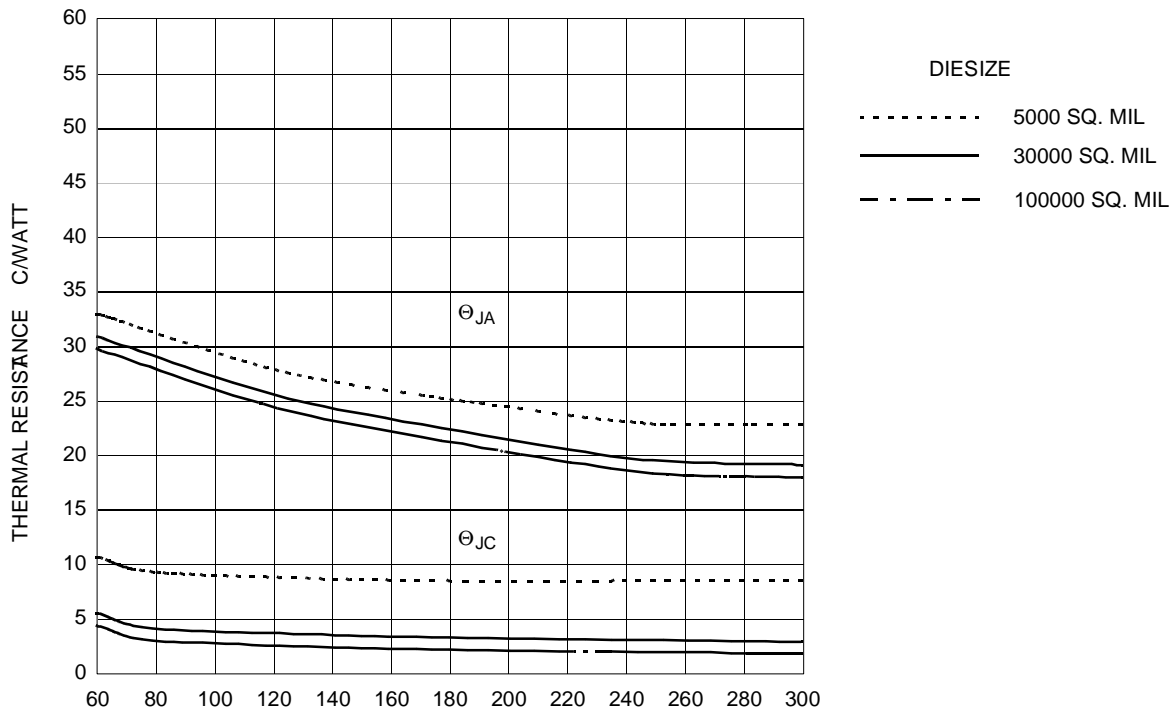


Figure 6. Thermal Resistance of Cypress Ceramic PGAs

Table 5. Plastic Surface Mount SOIC, SOJ^[8,9]

Package Type "S" and "V"	Paddle Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 170	Copper	98 x 84	8,232	19.0	120
18	140 x 170	Copper	98 x 84	8,232	18.0	116
20	180 x 250	Copper	145 x 213	30,885	17.0	105
24	180 x 250	Copper	145 x 213	30,885	15.4	88
24	170 x 500	Copper	141 x 459	64,719	14.9	85
28	170 x 500	Copper	145 x 213	30,885	16.7	84
28	170 x 500	Copper	141 x 459	64,719	14.4	80

Table 6. Plastic Quad Flatpacks

Package Type "N"	LF Material	Paddle Size (mil)	Die Size (mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
100	Copper	310 x 310	235 x 235	17	51
144	Copper	310 x 310	235 x 235	18	41
160	Copper	310 x 310	230 x 230	18	40
184	Copper	460 x 460	322 x 311	15	38.5
208	Copper	400 x 400	290 x 320	16	39

Note:

8. The data in *Table 6* was simulated for SOIC packaging.

9. SOICs and SOJs have very similar thermal resistance characteristics. The thermal resistance values given above apply to SOJ packages also.

Table 7. Ceramic Quad Flatpacks

Package Type "H" and "Y"	Cavity Size (mil)	LF Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
28	250 x 250	Alloy 42	123 x 162	19,926	9.2	96
28	250 x 250	Alloy 42	150 x 180	27,000	8.9	93
32	316 x 317	Alloy 42	198 x 240	47,520	7.5	72
44	400 x 400	Alloy 42	310 x 250	77,500	5.9	55
52	400 x 400	Alloy 42	250 x 310	77,500	5.9	55
68	400 x 400	Alloy 42	310 x 250	77,500	5.4	33
84	450 x 450	Alloy 42	310 x 250	77,500	5.4	29

Table 8. Cerpacks

Package Type "K" and "T"	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} (°C/W)	θ_{JA} (°C/W still air)
16	140 x 200	Alloy 42	100 x 118	11,800	10	107
18	140 x 200	Alloy 42	100 x 118	11,800	10	104
20	180 x 265	Alloy 42	128 x 170	21,760	9	102
24	170 x 270	Alloy 42	128 x 170	21,760	10	102
28	210 x 210	Alloy 42	150 x 180	27,000	9	98
32	210 x 550	Alloy 42	141 x 459	64,719	7	81

Table 9. Miscellaneous Packaging

Package Type	Cavity Size (mil)	Leadframe Material	Die Size (mil)	Die Area (sq. mil)	θ_{JC} ($^{\circ}\text{C/W}$)	θ_{JA} ($^{\circ}\text{C/W}$ still air)
24 VDIP ^[10]	500 x 275	Alloy 42	145 x 213	30,885	6	57
68 CPGA ^[11]	350 x 350	Kovar Pins	323 x 273	88,179	3	28

Note:

10. VDIP = "PV" package.

11. CPGA = "G" package.

Table 10. Die Sizes of Cypress Devices

Part Number	Size (mil ²)
SRAMs	
CY2147	10132
CY2148	9983
CY2149	9983
CY27LS03	4130
CY27S03A	4130
CY27S07A	4130
CY6116	20007
CY6116A	20007
CY6117	20007
CY6117A	20007
CY74S189	4130
CY7B134	76152
CY7B1342	76152
CY7B135	76152
CY7B138	76152
CY7B139	76152
CY7B144	76152
CY7B145	76152
CY7B160	27244
CY7B161	27244
CY7B162	27244
CY7B164	27244
CY7B166	27244
CY7B173	102200
CY7B174	102200
CY7B180	54600
CY7B181	54600
CY7B185	27244
CY7B186	27244
CY7B191	73152
CY7B192	73152
CY7B194	73152
CY7C122	6300
CY7C123	6300

Table 10. Die Sizes of Cypress Devices (continued)

CY7C128	20007
Part Number	Size (mil ²)
CY7C128A	17400
CY7C130	36636
CY7C131	36636
CY7C132	36636
CY7C136	36636
CY7C140	36636
CY7C141	36636
CY7C142	36636
CY7C146	36636
CY7C147	10132
CY7C148	9983
CY7C149	9983
CY7C150	6634
CY7C157	86460
CY7C161A	30885
CY7C162A	30885
CY7C164A	30885
CY7C166A	30885
CY7C167	21228
CY7C167A	21228
CY7C168	21228
CY7C168A	21228
CY7C169	21228
CY7C169A	21228
CY7C170	21228
CY7C170A	21228
CY7C171	21228
CY7C171A	21228
CY7C172	21228
CY7C172A	21228
CY7C183	65636
CY7C184	65636
CY7C185	30885
CY7C186	30885
CY7C187	30885

Table 10. Die Sizes of Cypress Devices (continued)

CY7C189	4130
Part Number	Size (mil ²)
CY7C190	4130
CY7C191	68150
CY7C192	68150
CY7C194	68150
CY7C196	68150
CY7C197	68150
CY7C198	68150
CY7C199	68150
CY7C191 (RAM2.5)	51590
CY7C192 (RAM2.5)	51590
CY7C194 (RAM2.5)	51590
CY7C196 (RAM2.5)	51590
CY7C197 (RAM2.5)	51590
CY7C198 (RAM2.5)	51590
CY7C199 (RAM2.5)	51590
CY7C9122	6300
CY93422A	6300
PROMs	
CY7C225	11815
CY7C235	13900
CY7C245	19321
CY7C245A	9394
CY7C251	49536
CY7C254	49536
CY7C261	28290
CY7C263	28290
CY7C264	28290
CY7C265	28290
CY7C266	28290
CY7C268	29400
CY7C269	29400
CY7C271	38750
CY7C274	38750
CY7C277	38750
CY7C279	38750
CY7C281	13900
CY7C282	13900
CY7C285	43875
CY7C286	43875
CY7C287	43875
CY7C289	43875
CY7C291	19182
CY7C291A	9394

Table 10. Die Sizes of Cypress Devices (continued)

CY7C292	19321
Part Number	Size (mil ²)
CY7C292A	9394
CY7C293A	9394
PLDs	
CY7C330	20088
CY7C331	16536
CY7C332	19116
CY7C335	23111
CY7C341	136320
CY7C342	83475
CY7C342B	49104
CY7C343	43953
CY7C344	21977
CY7C361	25872
PAL16L8	13552
PAL16R4	13552
PAL16R6	13552
PAL16R8	13552
PAL22V10C	18834
PAL22VP10C	18834
PALC16L8	9700
PALC16R4	9700
PALC16R6	9700
PALC16R8	9700
PALC22V10	19926
PALC22V10B	13284
PALC22V10D	12954
PLD20G10C	18834
PLDC18G8	7744
PLDC20G10	19926
PLDC20G10B	13284
PLDC20RA10	13284
FIFOs	
CY3341	8064
CY7C401	8064
CY7C402	8064
CY7C403	8064
CY7C404	8064
CY7C408A	16268
CY7C409A	16268
CY7C420	41019
CY7C421	41019
CY7C424	41019
CY7C425	41019

Table 10. Die Sizes of Cypress Devices (continued)

Document #: 38-00190

CY7C428	41019
Part Number	Size (mil²)
CY7C429	41019
CY7C432	50040
CY7C433	50040
CY7C439	47160
CY7C441	44756
CY7C443	44756
CY7C451	44756
CY7C453	44756
CY7C460	89445
CY7C462	89445
CY7C464	89445
CY7C470	89445
CY7C472	89445
CY7C474	89445
Logic	
CY2909A	7968
CY2910A	21750
CY2911A	7968
CY7C2901	11800
CY7C510	30704
CY7C516	29000
CY7C517	29000
CY7C901	11800
CY7C909	7968
CY7C910	21750
CY7C9101	36108
CY7C911	7968
ECL	
CY100E301L	14875
CY100E302L	14875
CY100E422	6960
CY100E474	10830
CY100E494	29575
CY10E301L	14875
CY10E302L	14875
CY10E422	6960
CY10E474	10830
CY10E494	29575
Bus Interface	
CY7C964	21460
VAC068	101060
VIC068A	103620
VIC64	103620