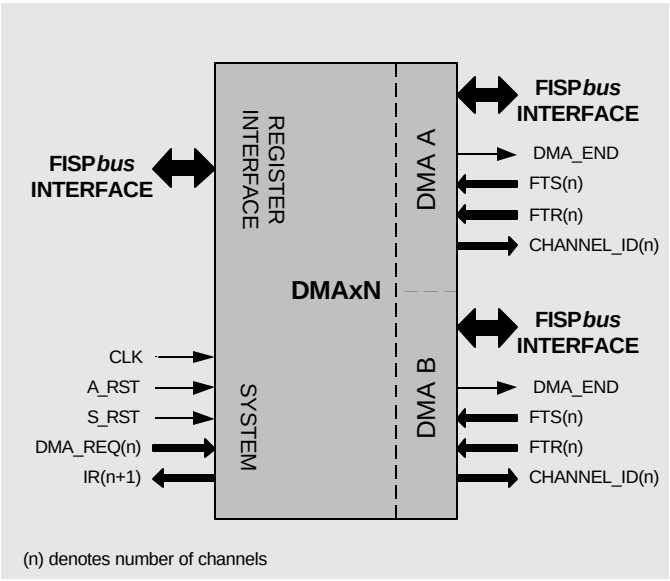
Inventra™ DMAxN-B1
Multi-Channel DMA Controller

FISPbus Peripherals FPGA/CPLD IP

D A T A S H E E T



DMAxN Core Block Diagram

DMAxN key features:

- Multi-channel DMA controller with two DMA FISPbus interfaces
- Address and data width and number of channels configurable
- Fixed or Incrementing address for source and destination
- Automatic packing, unpacking and realignment of data in the controller
- Simple FTS/FTR handshakes with other FISP products to maximize bus bandwidths
- DMA End strobes signal end of DMA to both source and destination slave devices
- Generic 'FISPbus' microprocessor interface

Overview

The DMAxN-B1 is an implementation of the Inventra™ DMAxN soft core as a netlist for the Cypress Delta39K™ family of complex PLDs (CPLDs).

The DMAxN core is a multi-channel DMA controller with two DMA FISPbus interfaces, which may be 8, 16, 32 or 64 bits wide depending on the implementation. The number of channels also depends on the implementation. In the DMAxN-B1, one DMA interface is 8 bits wide and the other 16 bits wide, and there is one DMA channel.

All channels transfer between the two DMA interfaces in either direction. The core allows fixed or incrementing addresses for source and destination, and has automatic packing, unpacking and realignment of data in the controller to match source and destination bus widths and start addresses. DMA end strobes signal end of DMA to both source and destination slave devices.

The DMAxN connects to all other FISPbus products including priority and round-robin based FISPbus arbiters. Bus bandwidths can be maximized through simple FTS/FTR handshakes with other FISP products.

The DMAxN-B1 deliverables comprise modified .vif files for each component (toplevel and submodules), wrappers for the .vif files in Verilog and VHDL, a compiled testbench and netlist simulation model for use with ModelSim, and supporting documentation.

CPLD Specifics	
Core Block	Inventra™ DMAxN
Supported Family	Cypress Delta39K™ CPLD 0.18µm SRAM process
Device tested	CY39100V676-200MBC
DMA Channels	1
Data Bus Width	**DMA A** 16 bits; **DMA B** 8 bits
Post-Layout Performance	57MHz
Utilization Parameters	
Macrocells used	248/1536
Channel Memory Blocks used	0/12
Cluster Memory Blocks used	0/24
I/O ports used (unidirectional)	163/294

CPLD IP Deliverables:

- .vif database files for Delta39K™ CPLDs
- Wrappers for the .vif files in both Verilog and VHDL
- Compiled testbench and netlist simulation model for use with ModelSim
- Core specification
- Readme/help file

DMAxN Description

The DMAxN supports multiple DMA channels, each transferring data in either direction across two bus master interfaces, A and B, with different address and data widths. A third interface, the Register Interface, is a bus slave and handles all accesses to internal registers.

The DMA controller decouples the accesses between the two DMA interfaces, A and B, by buffering the data internally. It performs all the data reformatting required to match the data widths of each bus and aligns the data to the byte address at each interface. Single-bus DMA is achieved by connecting both interfaces to the same bus.

Each channel is programmed with the starting address for each interface, the number of bytes to transfer and the direction of the transfer. Channels can be configured to transfer data in either direction.

DMA starts when a channel's DMA_Req goes active or a start command is issued to the channel's command register. From then on, the channel FSM generates a read or write request at each appropriate interface, until all requested bytes are transferred.

Multiple DMAs may take place simultaneously. Contention between channels at each interface is handled by internal arbitration based either on a round robin scheme or channel priority. In priority mode, the lower number channel has the higher priority.

Once DMA is initiated the DMA Controller starts reading from the source and accumulating data in the internal buffer. When enough data has been received to allow correct byte alignment at the destination, writes to the destination begin. If either slave is not ready, the transfers are held by waits on the corresponding bus.

The FTS (Free To Send) and FTR (Free To Receive) signals on the FISPbus inform the DMA Controller that the slave is ready to transfer with no waits. They further qualify the initiation of an access to ensure a quick response with minimum time on the bus. A DMA END strobe is generated with the last read or write at each interface to inform the slave device that DMA transfer is ended. An interrupt is also generated at the end of any DMA.

Accesses use the whole bus width where possible. Partial width accesses can happen at the start or end of DMA depending on the start byte addresses and number of bytes remaining to transfer. Both source or destination addresses may be fixed.

DMA normally ends when all the bytes specified in the byte count have been transferred. It is possible to terminate the DMA early by a command to the channel control registers. A status bit indicates when the DMA has been terminated before all bytes are transferred.

The design is completely synchronous, using a single clock.

More detailed information is given in the DMAxN Product Specification, which describes interface signal timing and software register interfacing.

FISPbus Interface

The FISPbus interface is a generic microprocessor interface specification developed specifically for Inventra's telecom cores. It provides the user with an easy to use, fully featured, on-chip bus structure. The FISPbus interface allows direct interconnection of multiple cores, as well as indirect connection to a microprocessor (or other bus standard) via a Microprocessor Personality Module (MPM) core. Further information is given in the FISPbus Engineering Specification.

The DMAxN's DMA Interfaces are both type FB Master / 4. The Register Interface is type FB Slave / 4 / 2 Full.

Applications

Applications for the DMAxN include microprocessor peripherals, memory management units and communications processors.

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