Inventra™ HDLC-CORE-B1
Single Channel HDLC Core

HDLC Functions FPGA/CPLD IP

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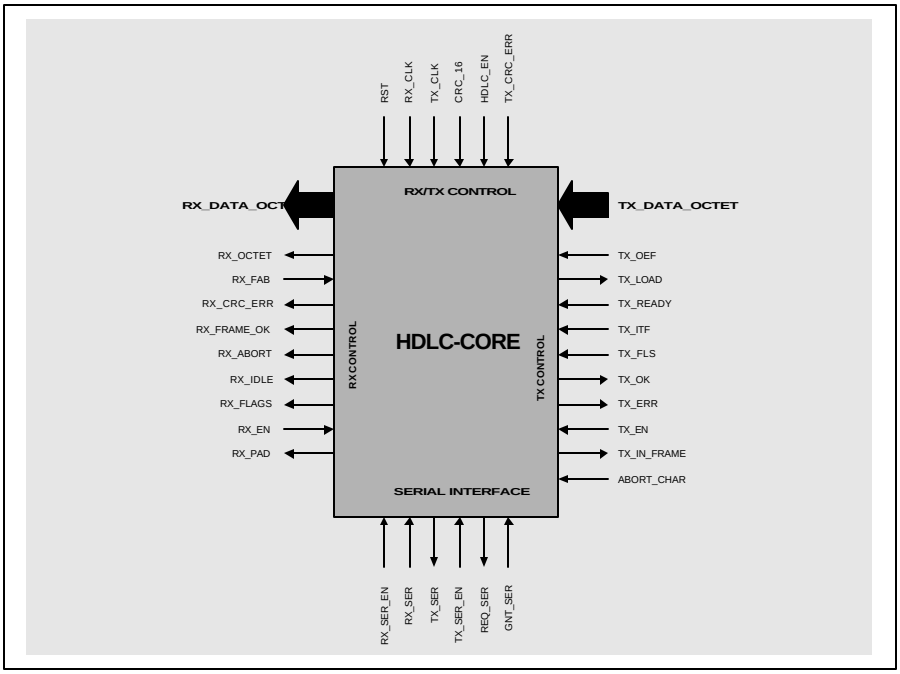

HDLC-CORE Core Interfacing

HDLC-CORE key features:

- HDLC processor
- Flag generation & detection
- 16 or 32-bit CRC generation & detection
- Frame Abort character generation & detection
- Zero insertion & detection
- Non octet-aligned frame reception
- PCM-style serial interface
- DMA capable, interfacing either with a standard DMA controller or a Linked List Access Controller
- 'FISPbus' microprocessor interface capable
- GCI serial interface capable
- Adaptable to match industry standard devices

Overview

The HDLC-CORE-B1 is an implementation of the Inventra™ HDLC-CORE soft core as a netlist for the Cypress Delta39K™ family of complex PLDs (CPLDs).

The HDLC-CORE is a single-channel HDLC controller core. The device contains a full-duplex transceiver with independent receive and transmit sections for bit-level HDLC protocol operations. Applications include Q.921 LAPD processors, Q.922 Frame relay processors, X.25 LAPB processors and Signaling System #7 processors.

The HDLC-CORE is designed to be used in conjunction with a control section containing the microprocessor registers plus (optionally) additional logic for performing address octet matching and minimum-length frame checking logic.

The HDLC-CORE-B1 deliverables comprise modified .vif files for each component (toplevel and submodules), wrappers for the .vif files in Verilog and VHDL, a compiled testbench and netlist simulation model for use with ModelSim, and supporting documentation.

CPLD Specifics	
Core Block	Inventra™ HDLC-CORE
Supported Family	Cypress Delta39K™ CPLD 0.18µm SRAM process
Device tested	CY39100V676-200MBC
Post-Layout Performance	83MHz with 32bit CRC
Utilization Parameters	
Macrocells used	164/1536
Channel Memory Blocks used	0/12
Cluster Memory Blocks used	0/24
I/O ports used (unidirectional)	49/294

CPLD IP Deliverables:

- .vif database files for Delta39K™ CPLDs
- Wrappers for the .vif files in both Verilog and VHDL
- Compiled testbench and netlist simulation model for use with ModelSim
- Core specification
- Readme/help file

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HDLC-CORE Description

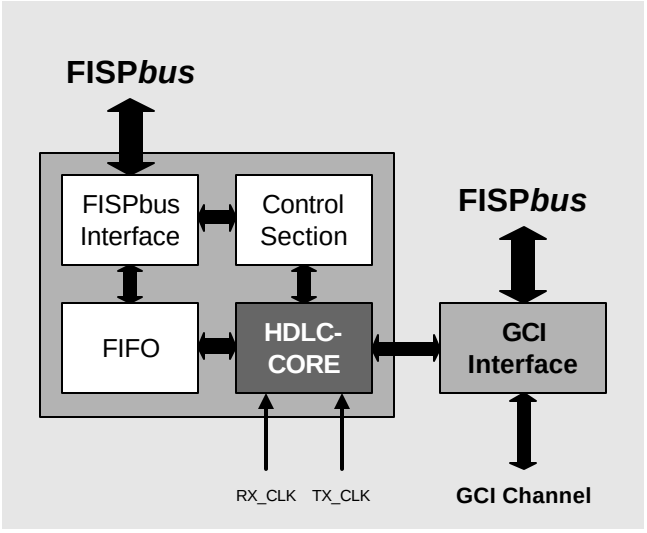
The HDLC-CORE is a single channel HDLC controller core. The device contains a full duplex transceiver, with independent receive and transmit sections for bit-level HDLC protocol operations.

The device is designed to be used in conjunction with a control section containing the microprocessor registers, and any additional logic required to perform address octet matching and/or minimum length frame checking. The adjacent diagram shows an HDLC-CORE controller being used in conjunction with a control section, a FISP*bus* generic microprocessor interface, and a GCI interface.

The design is completely synchronous, with separate clock inputs for receive and transmit allowing the two sections to operate asynchronously, should that be required.

The HDLC protocol encapsulates user data within frames. The start and end of frames are marked by a flag byte. The data between the start and end flags consists of an address field, control field, information field and a Frame Check Sequence (FCS) field.

The flag is the unique bit-pattern '01111110' (7E hex), and is used to mark both the start and the end of a frame. Transmitted user data is automatically framed by the HDLC-CORE, and received flags are removed from the data stream upon reception. Flags are searched for by the receiver, on a bit by bit basis, and can be recognized at any point in the receive bit stream. To prevent the flag pattern from being duplicated by the user data, extra zeros are automatically inserted on transmission, and removed from the data upon reception, by the HDLC-CORE.



The frame address is contained in the first field following the start flag. Additional address matching circuitry can be used by the HDLC-CORE to examine the complete address field of incoming frames and ignore or re-route frames accordingly.

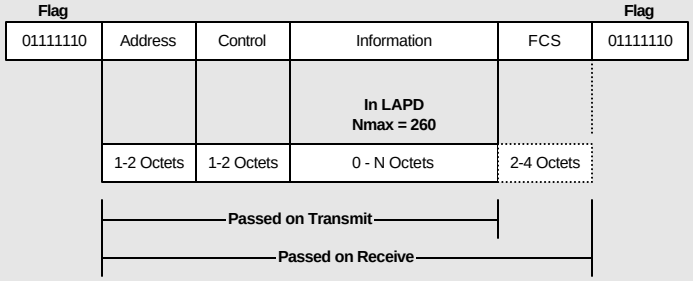
The information field contains the user data and may be null. This field may also not be an integer number of octets long. Note that the HDLC-CORE only transmits octet aligned data: however, when it receives non octet-aligned data, it pads the last octet.

The Frame Check Sequence (FCS) field is contained in the last two octets before the end flag in a frame. The field is computed using a Cyclic Redundancy Check (CRC) polynomial. This is used to perform error detection on the address, control and information fields.

The standard CRC-CCITT polynomial is used in both the receive and transmit directions. The HDLC-CORE core also provides support for a non-standard 32-bit CRC (CRC-32) which may be used instead. CRC generation and checking is performed automatically by the HDLC-CORE.

More detailed information is given in the HDLC-CORE Product Specification, which describes interface signal timing and software register interfacing.

HDLC Frame Format



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