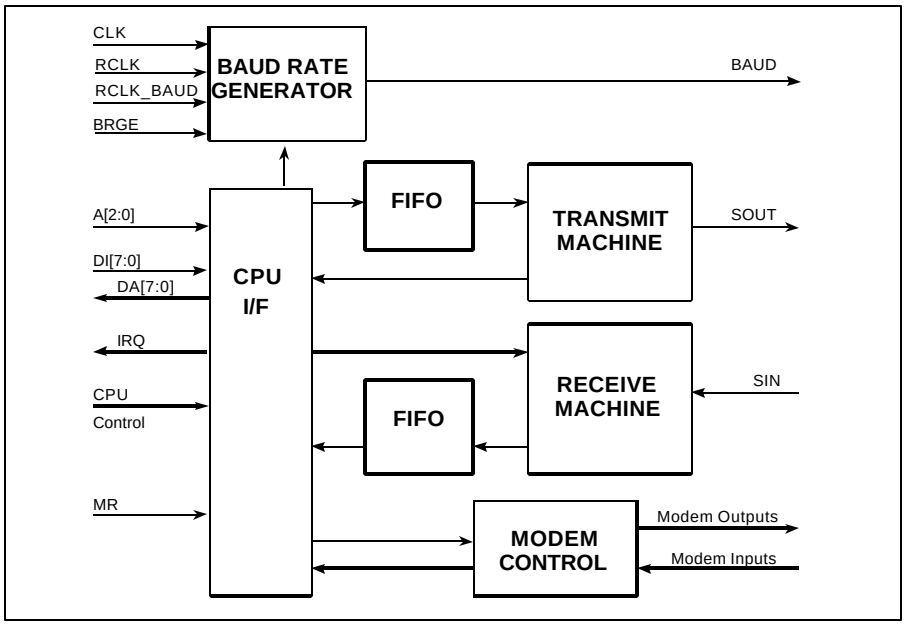
Inventra™ M16550A-B1 UART with FIFOs

Serial Communications FPGA/CPLD IP

D A T A S H E E T



M16550A Core Block Diagram

M16550A key features:

- Software compatible with the NSC NS16550A
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generator
- Diagnostic loop-back mode
- Scratch register
- Two 16-byte FIFOs

Overview

The M16550A-B1 is an implementation of the Inventra™ M16550A soft core as a netlist for the Cypress Delta39K™ family of complex PLDs (CPLDs).

The M16550A is a high-performance universal asynchronous receiver/transmitter (UART) with two 16-bit FIFOs - one for transmit and one for receive. It also includes a 16-bit programmable baud rate generator and an 8-bit scratch register, eight modem control lines and two DMA handshake lines which are used to indicate when the FIFOs are ready to transfer data to the CPU.

The M16550A is fully programmable through its 8-bit CPU interface. It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits. If enabled, the parity can be odd, even or forced to a defined state. Interrupts can be generated from any of 10 sources.

The M16550A-B1 deliverables comprise modified .vif files for each component (toplevel and submodules), wrappers for the .vif files in Verilog and VHDL, a compiled testbench and netlist simulation model for use with ModelSim, and supporting documentation.

CPLD Specifics	
Core Block	Inventra™ M16550A
Supported Family	Cypress Delta39K™ CPLD 0.18µm SRAM process
Device tested	CY39100V676-200MBC
Post-Layout Performance	47MHz
Utilization Parameters	
Macrocells used	346/1536
Channel Memory Blocks used	3/12
Cluster Memory Blocks used	0/24
I/O ports used (unidirectional)	43/294

CPLD IP Deliverables:

- .vif database files for Delta39K™ CPLDs
- Wrappers for the .vif files in both Verilog and VHDL
- compiled testbench and netlistsimul-ation model for use withModelSim
- Core specification
- Readme/help file

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M16550A Features

Transmit Operation

Transmission is initiated by writing the data to be sent to the TX Holding Register or to the TX FIFO (if enabled). The data is then transferred to the TX Shift Register. The bits to be transmitted are then shifted out of the TX Shift Register using the output from the Baud Rate Generator as the clock.

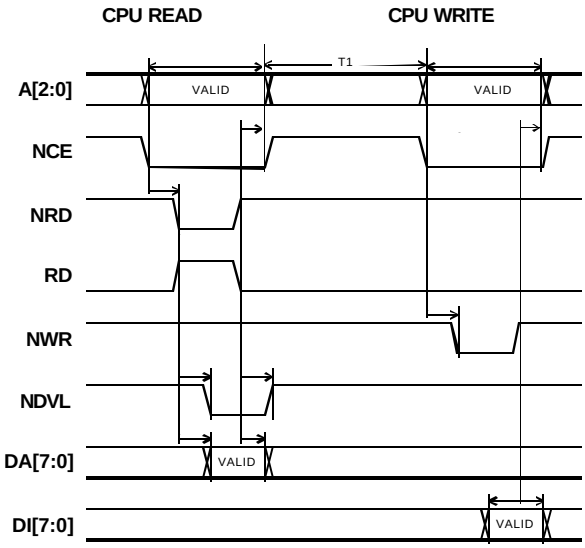
With the FIFO enabled, the M16550A can store up to 16 bytes for transmission at a time.

Receive Operation

Data is sampled into the RX Shift Register using RCLK. A filter is then used to remove spurious inputs. When the complete word has been clocked into the receiver, the data bits are transferred to the RX Buffer Register or to the RX FIFO (if enabled) to be read by the CPU.

With the FIFO enabled, the M16550A can store up to 16 bytes of received data at a time.

CPU Read/Write Timing



Note: T1 must be greater than 2 cycles of FCLK.

Core Signals

CPU INTERFACE SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
CLK	Input	Clock Input for Baud Rate Generator. Common values are 3.072 and 1.8432 MHz, however maximum speed is limited only by the technology used.
FCLK	Input	Fast Clock. Used to clock everything except the Baud Rate Generator.
MR	Input	Master Reset, active high.
NCE	Input	Chip Enable, active low.
A[2:0]	Input	Address lines.
RD	Input	I/O Read Strobe, active high. Latches the data that is read back. Available separately for use with scan test tools.
NRD	Input	I/O Read Strobe, active low. The register selected by A[2:0] & DLAB (LCR[7]) is read. The status will not change until the rising edge of NRD.
NWR	Input	I/O Write Strobe, active low. The register selected by A[2:0] & DLAB (LCR[7]) is written on the rising edge of NWR.
DI[7:0]	Input	Data Bus Input. Must be valid during write cycles.
TX_CLOCK	Input	Clock for transmit engine.
RX_CLOCK	Input	Clock for receive engine.
IRQ	Output	Interrupt Request. Goes high whenever one of the enabled interrupts becomes valid.
RXRDY	Output	DMA Handshake. Goes low when the RX FIFO contains data.
TXRDY	Output	DMA Handshake. Goes low when the TX FIFO requires data.
NDVL	Output	Output Valid, Bidirectional Buffer Control. Goes low when NCE and NRD are both active to indicate that the output data bus is valid.
DA[7:0]	Output	Data Bus Output. Register returned depends on the state of A[2:0] & DLAB (LCR[7]).
SERIAL INTERFACE SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
BAUD	Output	Receive/Transmit clock, derived from CLK divided by the value in the divisor latch DLL & DLM.
RCLK	Input	Receiver Clock.
RCLK _BAUD	Input	RCLK Select. When tied high, RCLK is connected to BAUD; when tied low, RCLK is connected to an external clock.
SIN	Input	Serial Input. Data is clocked in using RCLK/16.
SOUT	Output	Serial Output. Data is clocked out using output from Baud Rate Generator, divided by16.
NDCD	Input	Data Carrier Detect, MSR[7] status bit. Active low.
NRI	Input	Ring Indicator, MSR[6] status bit. Active low.
NDSR	Input	Data Set Ready, MSR[5] status bit. Active low.
NCTS	Input	Clear To Send, MSR[4] status bit. Active low.
NOUT2	Output	General Control, MSR[3] control bit. Active low.
NOUT1	Output	General Control, MSR[2] control bit. Active low.
NRTS	Output	Request To Send, MSR[1] control bit. Active low.
NDTR	Output	Data Terminal Ready, MSR[0] control bit. Active low.

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