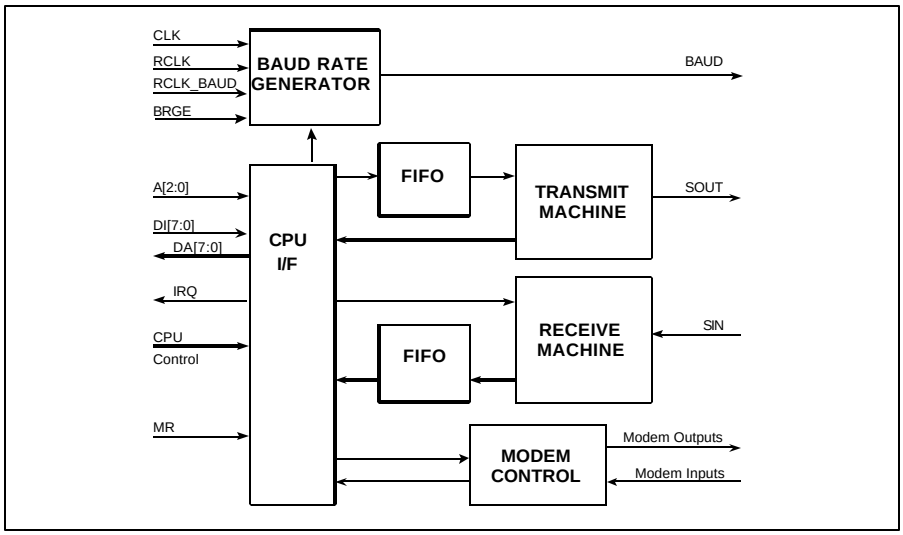
Inventra™ M16x50-B1
Enhanced 16550A-Compatible UART

Serial Communications FPGA/CPLD IP

D A T A S H E E T



M16x50 Core Block Diagram

M16x50 key features:

- Compatible with Inventra™ M16C450 and M16550A UARTs
- Hardware & Software Flow Control
- IrDA Modulation/Demodulation
- Transmit FIFO Threshold
- Configurable FIFO Depth
- CTS and RTS Interrupts
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Diagnostic loop-back mode

Overview

The M16x50-B1 is an implementation of the Inventra™ M16x50 soft core as a netlist for the Cypress Delta39K™ family of complex PLDs (CPLDs).

The M16x50 core is an extension of the Inventra™ M16550A UART with FIFOs, with enhancements that emulate features found in similar discrete devices with a range of part numbers. Some of the enhancements are enabled by software and are always present in the design: some – such as maximum FIFO size – are configurable and are selected on compilation.

In common with the M16550A, the M16x50 offers programmable word length, stop bits and parity bit. A 16-bit programmable baud rate generator is included, together with separate transmit and receive FIFOs. The M16x50 also includes two DMA handshake lines, which are used to indicate when the FIFOs are ready to transfer data.

Interrupts can be generated from any of 10 sources.

The M16x50-B1 deliverables comprise modified .vif files for each component (toplevel and submodules), wrappers for the .vif files in Verilog and VHDL, a compiled testbench and netlist simulation model for use with ModelSim, and supporting documentation.

CPLD Specifics	
Core Block	Inventra™ MI6x50
Supported Family	Cypress Delta39K™ CPLD 0.18µm SRAM process
Device tested	CY39100V676-200MBC
Post-Layout Performance	30MHz for 16byte FIFO 27.7MHz for 32byte FIFO 24.4MHz for 64byte FIFO 22.7MHz for 128byte FIFO
Utilization Parameters	
Macrocells used	403/1536 for 16byte FIFO 411/1536 for 32byte FIFO 419/1536 for 64byte FIFO 427/1536 for 128byte FIFO
Channel Memory Blocks used	3/12
Cluster Memory Blocks used	0/24
I/O ports used (unidirectional)	43/294

CPLD IP Deliverables:

- .vif database files for Delta39K™ CPLDs
- Wrappers for the .vif files in both Verilog and VHDL
- Compiled testbench and netlist simulation model for use with ModelSim
- Core specification
- Readme/help file

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M16x50 Features

MODES OF OPERATION The M16x50 has M16C450 and M16550A modes of operation. After a hardware reset, the M16x50 will be in M16C450 mode. It can then have its FIFOs enabled and enter M16550A mode. The M16x50 then adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

FLOW CONTROL The M16x50 offers both hardware flow control (in which the transmission and reception of data characters is controlled via the RTS and CTS modem status signals) and software flow control (in which transmission and reception are controlled via the transmission of 'XON/XOFF' characters).

Hardware transmission and reception flow control can be enabled separately. When hardware transmission flow control is enabled, the M16x50 disables transmission when the CTS modem control signal is sampled inactive. When hardware reception flow control is enabled, the M16x50 forces the RTS signal to its inactive state when the Receive FIFO exceeds a pre-set trigger level.

Software reception flow control works by comparing received data characters with the XOFF character. Software transmission flow control works by sending the XOFF character when the Receive FIFO exceeds its threshold level. As soon as the Receive FIFO has fallen below its threshold level, the XON character is transmitted to re-enable transmission from the other end of the link.

On reset, the XON/XOFF registers are defined by configuration constants. The normal default is to reset them to 00h: this ensures compatibility with existing driver software.

IRDA MODULATION/DEMODULATION The M16x50 includes basic IrDA 1.0 SIR modulation/demodulation. This feature uses the x16 Transmit clock and Receive clock to generate $^{3}/_{16}$ width pulses.

CHARACTER TIMEOUT Two signals – CR and TOT – have been included in the M16x50 in order to support system implementations that use an external timer to detect an end of data packet when no characters have been received for a time-out period. CR is always active, whereas TOT is only active when software flow control is enabled.

Core Signals

CPU INTERFACE SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
CLK	Input	Master clock input.
MR	Input	Master reset (active high).
NCE	Input	Chip enable (active low).
A[2:0]	Input	Address lines.
RNW	Input	Read Not Write control The register selected is defined by A[2:0] & DLAB (LCR[7]).
DI[7:0]	Input	Data bus input. Must be valid during write cycles.
DA[7:0]	Output	Data bus output. Register returned depends on the state of A[2:0] & DLAB (LCR[7]).
NDVL	Output	Data bus output valid (active low). Can be used to control a bi-direct buffer for the data bus.
IRQ	Output	Interrupt request (active high). Goes high whenever one of the enabled interrupts becomes valid.
RXRDY	Output	DMA handshake. Goes low when the RX FIFO contains data.
TXRDY	Output	DMA handshake. Goes low when the TX FIFO requires data.
SERIAL INTERFACE SIGNALS		
BAUD	Output	Baud Rate Generator output clock. When the baud rate generator divisor is 1, this signal is permanently high. For divisors greater than 1, this signal has an output frequency equal to the input frequency of CLK divided by the baud rate generator divisor.
RCLK	Input	External Receive Clock input.
RCLK_ BAUD	Input	Receive Clock Select. When high, the receiver is clocked from the output of the baud rate generator. When low, the receiver is clocked from the RCLK input.
BRGE	Input	Baud Rate Generator Enable (active high). When low, the baud rate generator is held in its current state. This signal can be used to add a pre-scaler to the baud rate generator.
SIN	Input	Serial input. Data is clocked in using the baud rate generator (or RCLK), divided by 16.
SOUT	Output	Serial output. Data is clocked out using the baud rate generator, divided by 16.
NDCD	Input	Data Carrier Detect, MSR[7] status bit (active low).
NRI	Input	Ring Indicator, MSR[6] status bit (active low).
NDSR	Input	Data Set Ready, MSR[5] status bit (active low)
NCTS	Input	Clear To Send, MSR[4] status bit (active low). Also used for hardware flow control.
NOUT1	Output	General control, MSR[2] control bit (active low).
NOUT2	Output	General control, MSR[3] control bit (active low).
NRTS	Output	Request To Send, MSR[1] control bit (active low). Also used for hardware flow control.
NDTR	Output	Data Terminal Ready, MSR[0] control bit (active low).
CR	Output	Character Received. Goes high for 1 Receive clock when a character is received.
TOT	Output	Transmitter Off Transmitted. Goes high after an XOFF character is transmitted.

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