Inventra™ MI2C-B1
I²C Bus Interface

Bus Interface FPGA/CPLD IP

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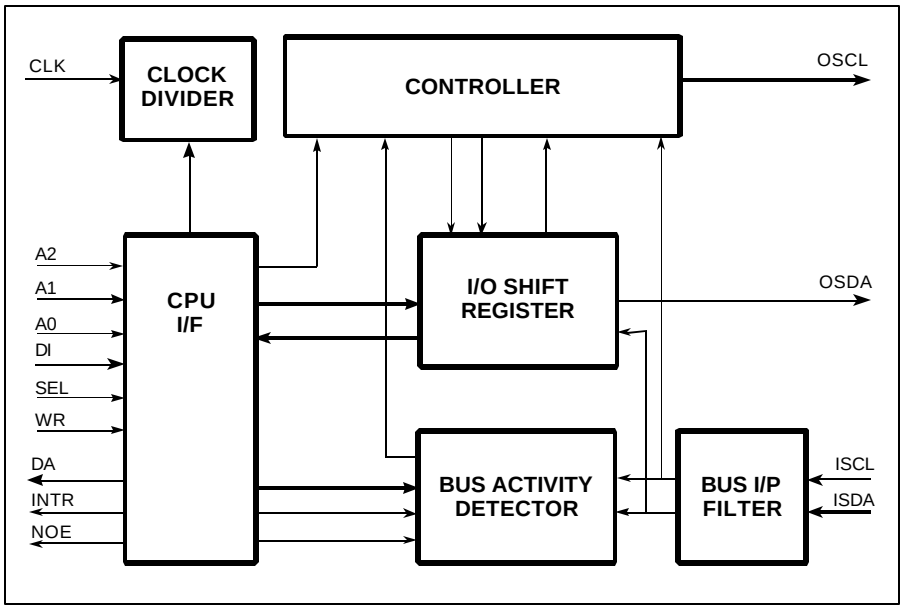

MI2C Core Block Diagram

MI2C key features:

- Master or slave operation
- Multi-master systems supported
- Allows 10-bit addressing with I²C bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s ('fast mode')
- Allows operation from a wide range of input clock frequencies
- Synchronous processor interface

Overview

The MI2C-B1 is an implementation of the Inventra™ MI2C soft core as a netlist for the Cypress Delta39K™ family of complex PLDs (CPLDs).

The MI2C provides an interface between a microprocessor and an I²C bus. It can be programmed to operate as either a master or a slave device and performs arbitration in master mode to allow it to operate in multi-master systems.

In slave mode, it can interrupt the processor when it recognizes its own 7-bit or 10-bit address or the general call address.

The MI2C can be used in any applications which use I²C bus devices. These are primarily in the consumer and telecoms market segments. The I²C bus is also used as a board level communications protocol.

The MI2C-B1 deliverables comprise modified .vif files for each component (toplevel and submodules), wrappers for the .vif files in Verilog and VHDL, a compiled testbench and netlist simulation model for use with ModelSim, and supporting documentation.

CPLD Specifics	
Core Block	Inventra™ MI2C
Supported Family	Cypress Delta39K™ CPLD 0.18µm SRAM process
Device tested	CY39100V676-200MBC
Post-Layout Performance	53MHz
Utilization Parameters	
Macrocells used	153/1536
Channel Memory Blocks used	0/12
Cluster Memory Blocks used	0/24
I/O ports used (unidirectional)	29/294

CPLD IP Deliverables:

- .vif database files for Delta39K™ CPLDs
- Wrappers for the .vif files in both Verilog and VHDL
- Compiled testbench and netlist simulation model for use with ModelSim
- Core specification
- Readme/help file

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MI2C Features

Operating Modes

The MI2C can operate in four modes: Master Transmit; Master Receive; Slave Transmit; and Slave Receive.

The MI2C will automatically enter Slave Transmit mode if it receives its own Slave Address and a Read bit.

It will similarly enter Slave Receive mode if it receives either its own Slave Address and a Write bit, or the General Call Address.

Status Information

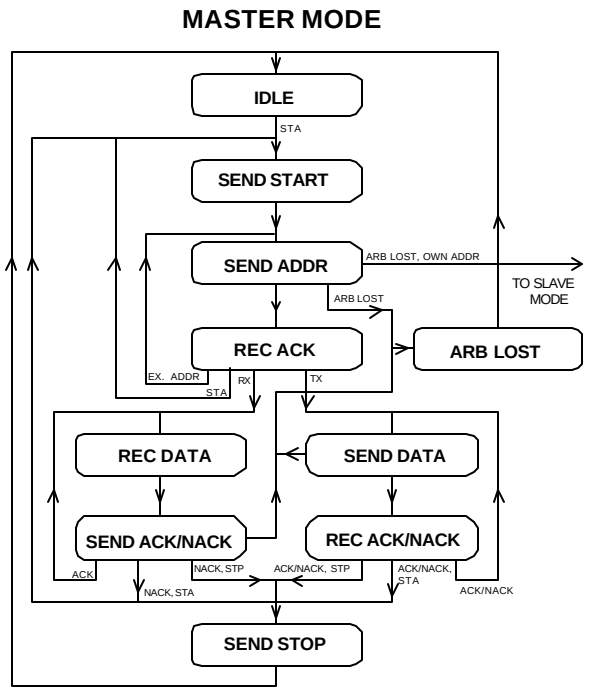
The state of the interface at any time is indicated by the status code recorded in the MI2C's STAT register.

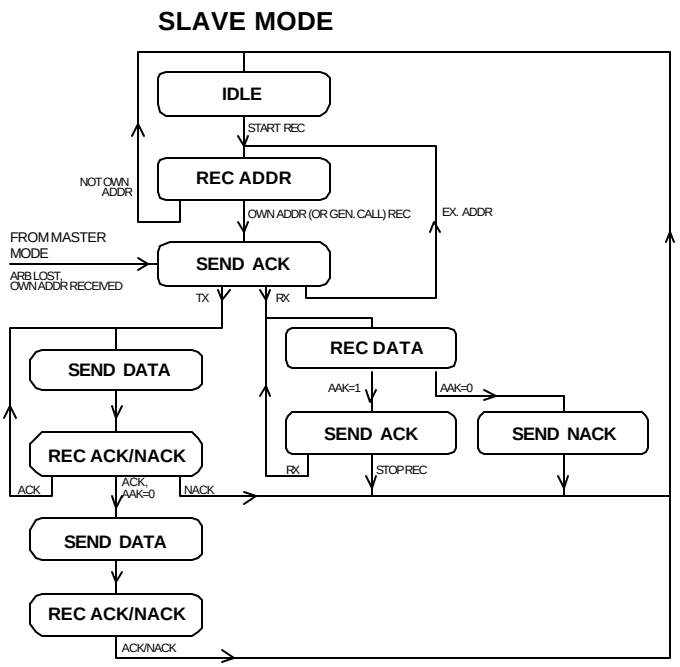
There are 30 status codes corresponding to the different possible states of the MI2C, plus a further code that indicates when no relevant status information is available. The states reported cover all conditions from successful transmission to bus errors and loss of arbitration.

The appropriate microprocessor responses to the reported interface condition and the MI2C actions these invoke are detailed in the MI2C Product Specification.

Core Signals

SIGNAL	TYPE	DESCRIPTION
ISDA	Input	I^2C bus input data line
ISCL	Input	I^2C bus input clock line
DI[7:0]	Input	Processor input data bus
A[2:0]	Input	Processor address lines
SEL	Input	Processor select line
WR	Input	Processor write enable
NRST	Input	Reset, active low
CLK	Input	Clock
NOE	Output	Data bus output enable, active low
DA[7:0]	Output	Processor output data bus
INTR	Output	Processor interrupt line
OSDA	Output	I^2C bus output data line
OSCL	Output	I^2C bus output clock line





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