64K/128K/256K/512K x 72 SRAM Modules

Features

- **Operates at 133 MHz**
- **Uses 128K x 18, or 256K x 18 high performance synchronous SRAMs**
- **168-position Angled DIMM from Amp p/n 179508-2**
- **3.3V inputs/data outputs**

Functional Description

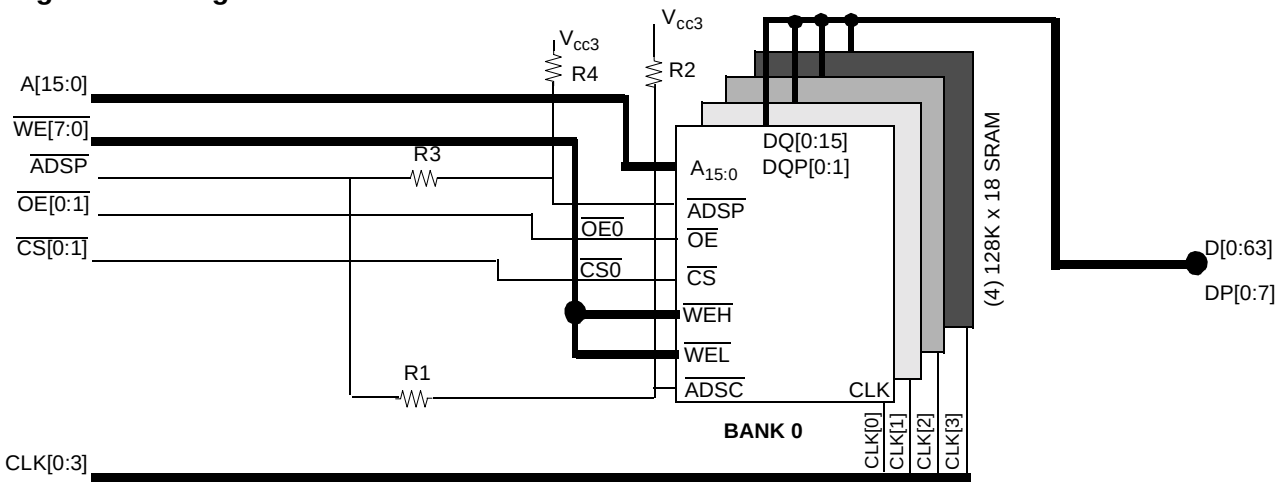
The CYM9265, CYM9266, CYM9267, and the CYM9268 are high-performance synchronous memory modules organized as 64K(9265), 128K(9266), 256K(9267), or 512K(9268) by 72 bits. These modules are constructed from either 128K x 18(9265,9266,9267) or 256K x 18(9268) SRAMs in plastic surface mount packages on an epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

The module is configured as either one or two banks, where each bank has separate chip select and output enable controls. Separate clocks are provided for every pair of SRAMs.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 30 micro-inches of gold flash.

Logic Block Diagram - CYM9265

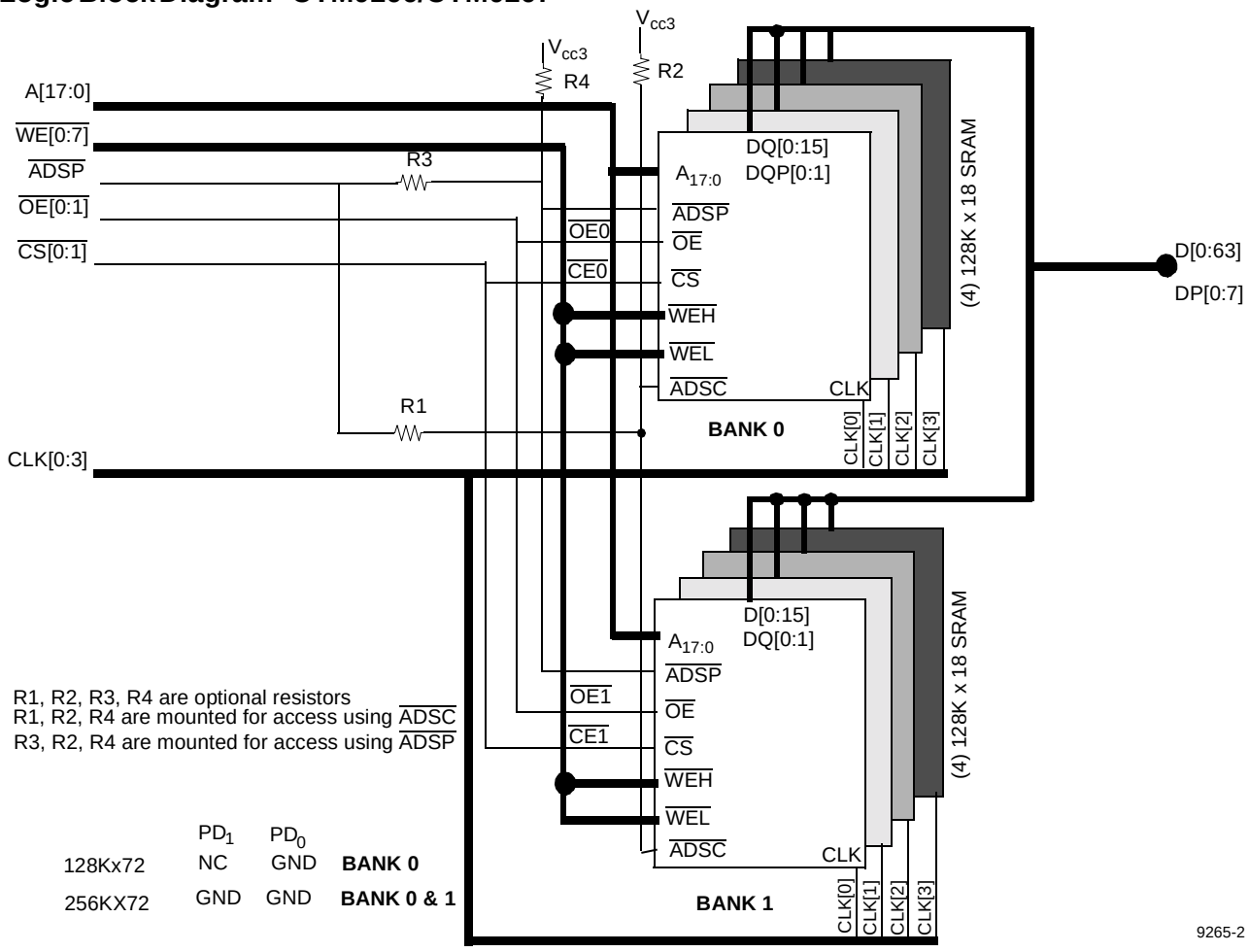


R1, R2, R3, R4 are optional resistors
R1, R2, R4 are mounted for access using $\overline{\text{ADSC}}$
R3, R2, R4 are mounted for access using $\overline{\text{ADSP}}$

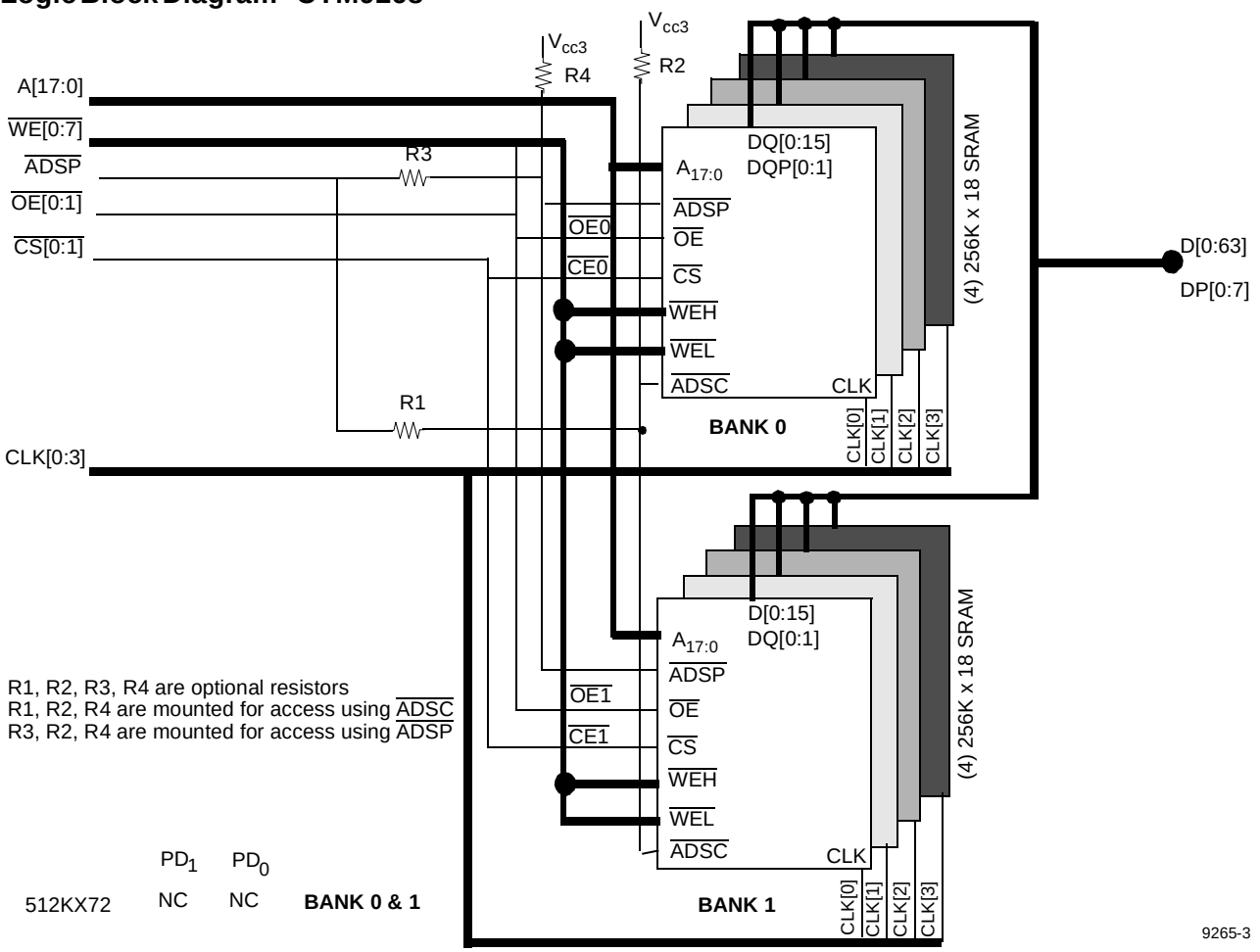
	PD_1	PD_0	
64Kx72	GND	NC	**BANK 0**

9265-1

Logic Block Diagram - CYM9266/CYM9267



Logic Block Diagram - CYM9268

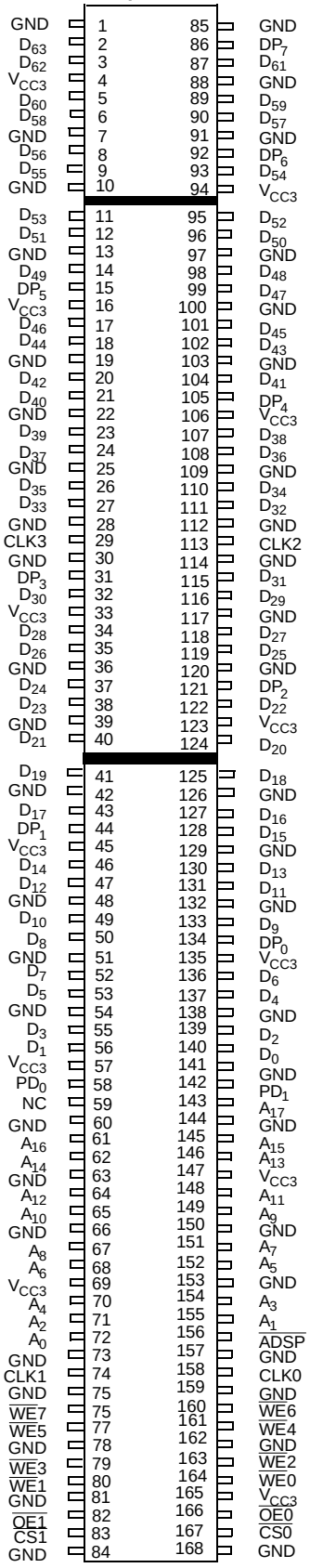


Selection Guide

Part Number	Synchronous Cache Module			
	CYM9265-133 / 100	CYM9266-133 / 100	CYM9267-133 /100	CYM9268-133 /100
Cache Size	64K x 72	128K x 72	256K x 72	512K x 72
SRAMs Used	4 of 128K x 18	8 of 128K x 18	8 of 128K x 18	8 of 256K x 18
System Clock (MHz)	133,100	133,100	133,100	133,100
Data t_{CO}	4.5, 5.5 ns	4.5, 5.5 ns	4.5, 5.5 ns	4.5, 5.5 ns

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



9260-4

Pin Definitions

Signal	Description
V_{CC3}	3V Supply
GND	Ground
A[17:0]	Addresses From Processor
$\overline{OE}$[1:0]	Output Enables For The Two Banks
$\overline{WE}$[7:0]	Byte Write Enables
$\overline{CS}$[1:0]	Chip Select For The Two Banks
PD_0–PD_1	Presence Detect Output Pins
D[63:0]	Data Lines From Processor
DP[7:0]	Data Parity Lines From Processor
CLK[0:3]	Clock Lines To The Module
$\overline{ADSP}$	Address Strobe From The Processor
NC	Signal Not Connected On Module
RSVD	Reserved

Presence Detect Pins

	PD_1	PD_0
CYM9265 - Pipelined 64K x 72	GND	NC
CYM9266 - Pipelined 128K x 72	NC	GND
CYM9267 - Pipelined 256K x 72	GND	GND
CYM9268 - Pipelined 512K x 72	NC	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied..... –0°C to +70°C

3.3V Supply Voltage to Ground Potential..... –0.5V to +4.5V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +4.6V

DC Input Voltage ..... –0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
I_{CC} (9265)	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		1000	mA
I_{CC} (9266)	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		1000	mA
I_{CC} (9267)	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f =f_{MAX} = $1/t_{RC}$		1200	mA
I_{CC} (9268)	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		2400	mA

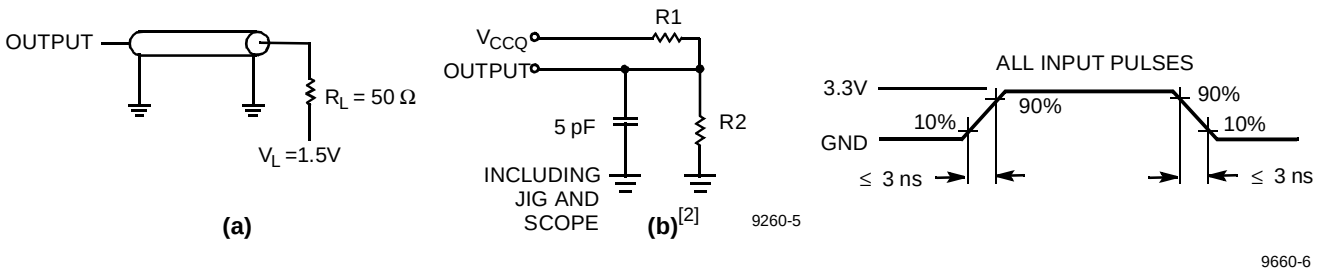
Capacitance[1]

Parameter	Description	Test Conditions	Max.	Max.	Unit
C_A	Address Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9265	24	pF
			9266	14	pF
			9267	20	pF
			9268	40	pF
C_I	Control Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9265	24	pF
			9266	16	pF
			9267	20	pF
			9268	40	pF
C_O	Input/Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9265	9	pF
			9266	5	pF
			9267	8	pF
			9268	16	pF
C_{CLK}	Clock Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9265	6	pF
			9266	3	pF
			9267	5	pF
			9268	10	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3]



Switching Characteristics Over the Operating Range

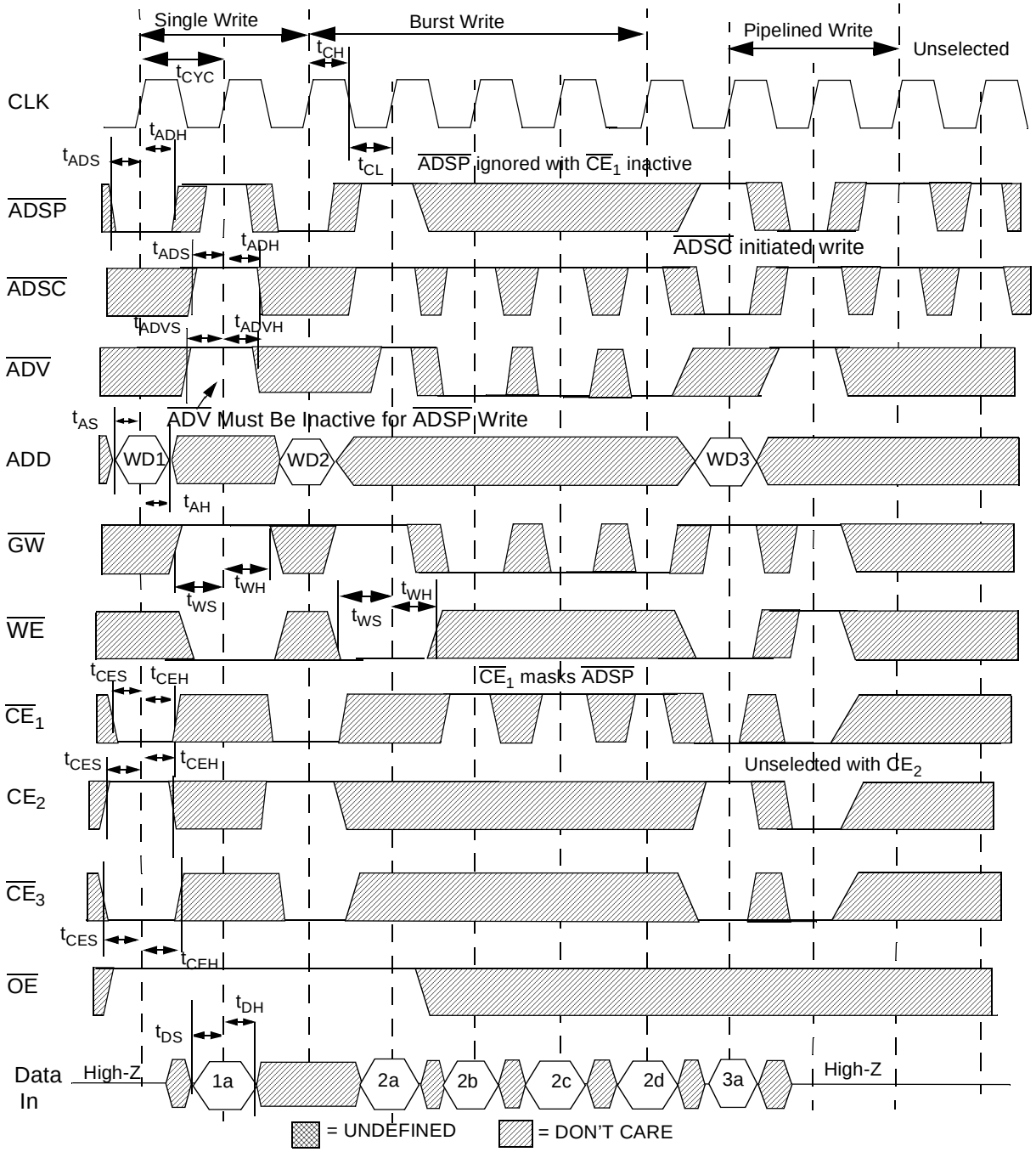
Parameter	Description	CYM9265/66/67/68				Unit
		133 MHz		100 MHz		
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	7.5		10		ns
t_{CH}	Clock HIGH	1.9		3.5		ns
t_{CL}	Clock LOW	1.9		3.5		ns
t_{AS}	Address Set-Up Before CLK Rise	2		2		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		4.5		5.5	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2		3.1		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0. 5		0.5		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2		2		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2		2		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	2		2		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[4]		7		7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		4.5		5.5	ns

Notes:

2. Resistor values for V_{CCQ}=3.3V are R1 = 317Ω and R2 = 351 Ω.
3. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC Test Loads. All measurements are made at room temperature.
4. t_{EOZ} is specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

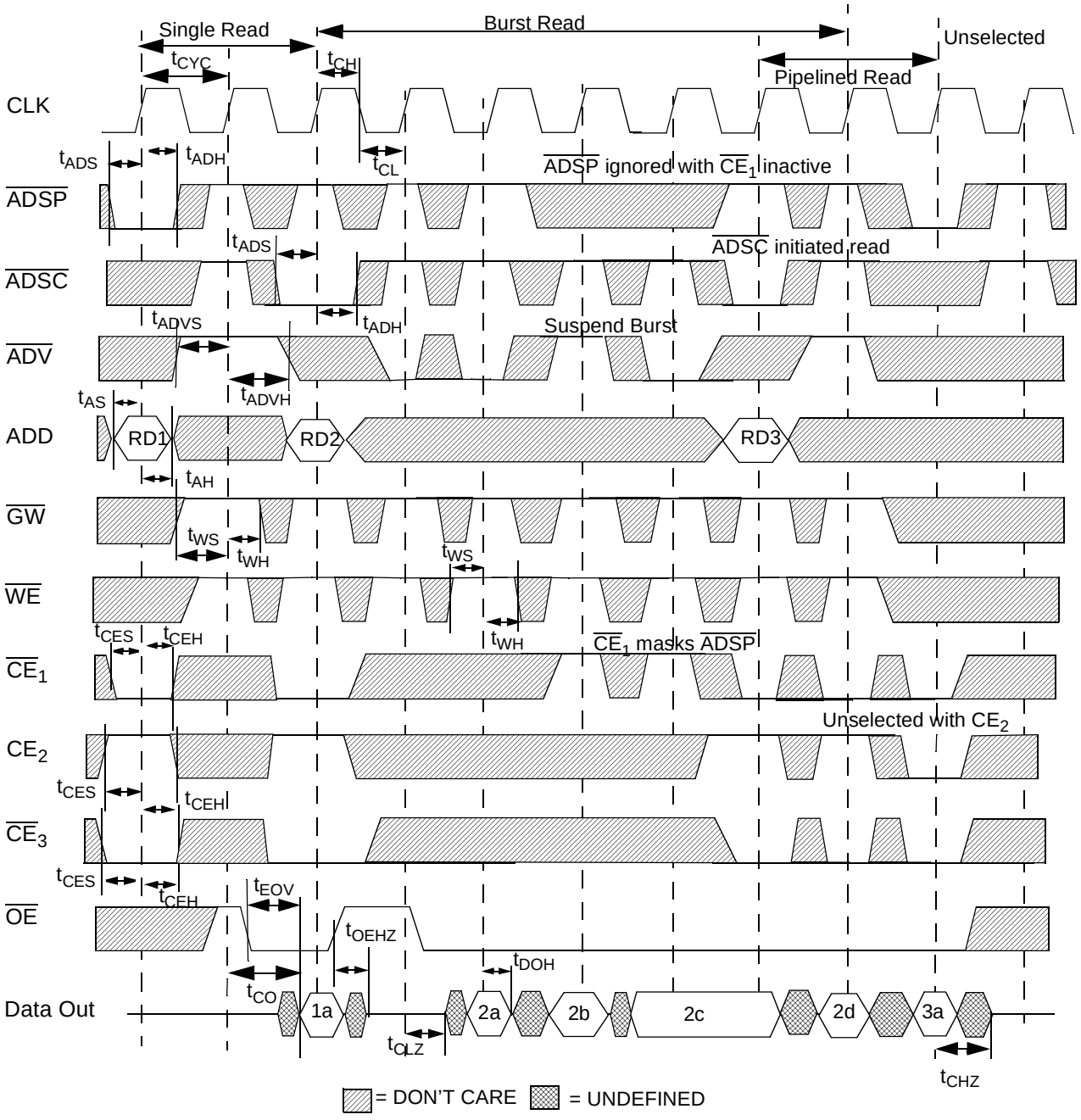
Switching Waveforms

Write



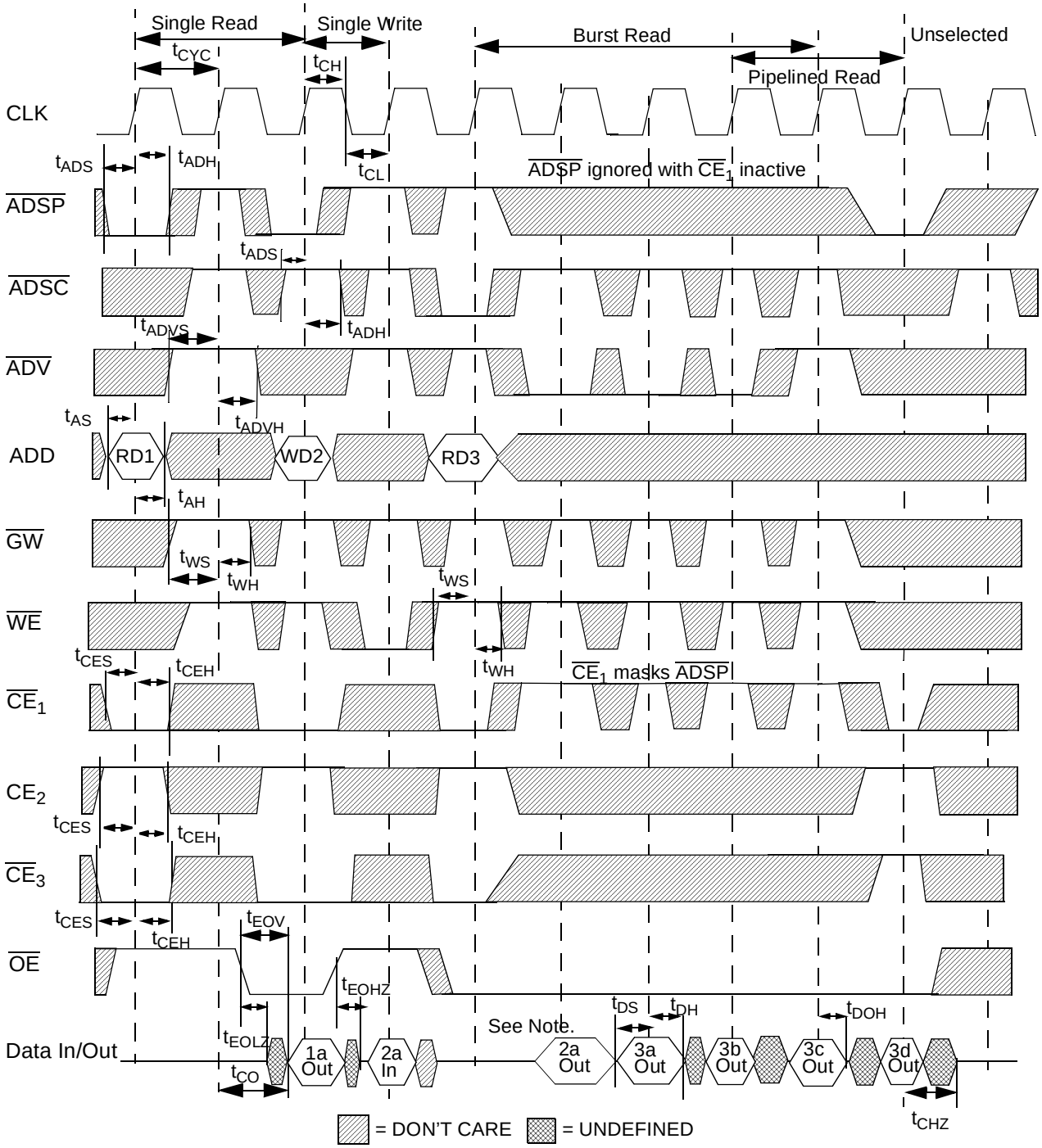
Switching Waveforms (continued)

Read



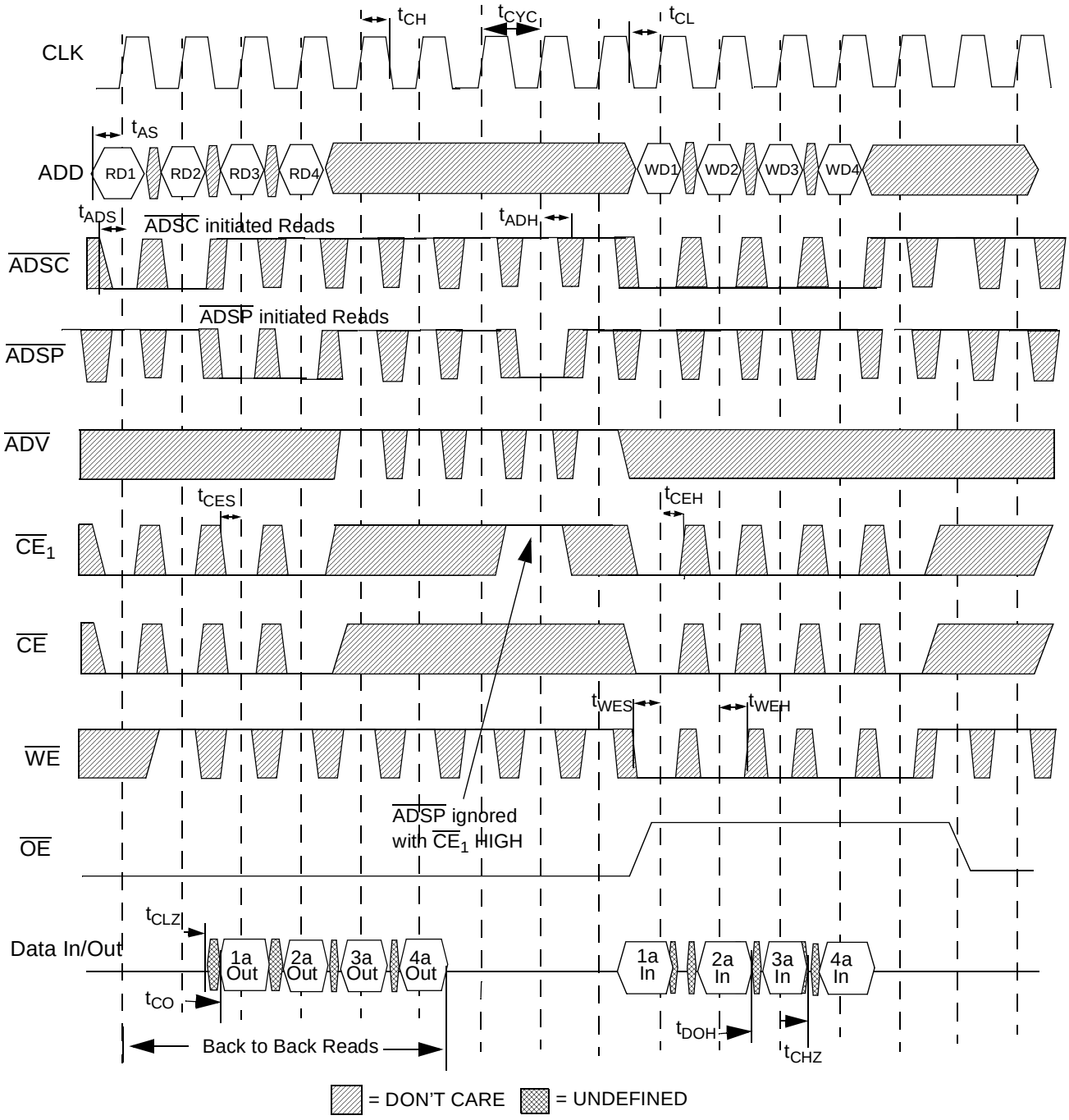
Switching Waveforms (continued)

Read / Write



Switching Waveforms (continued)

Pipeline Timing



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
100	CYM9265PM-100C	PM43	168-Pin Dual-Readout SIMM (DIMM)	Sync 64K x 72	Commercial
	CYM9266PM-100C	PM44	168-Pin Dual-Readout SIMM (SIMM)	Sync 128K x 72	
	CYM9267PM-100C	PM44	168-Pin Dual-Readout SIMM (DIMM)	Sync 256K x 72	
	CYM9268PM-100C	PM44	168-Pin Dual-Readout SIMM (DIMM)	Sync 512K x 72	
133	CYM9265PM-133C	PM43	168-Pin Dual-Readout SIMM (DIMM)	Sync 64K x 72	
	CYM9266PM-133C	PM44	168-Pin Dual-Readout SIMM (SIMM)	Sync 128K x 72	
	CYM9267PM-133C	PM44	168-Pin Dual-Readout SIMM (DIMM)	Sync 256K x 72	
	CYM9268PM-133C	PM44	168-Pin Dual-Readout SIMM (DIMM)	Sync 512K x 72	

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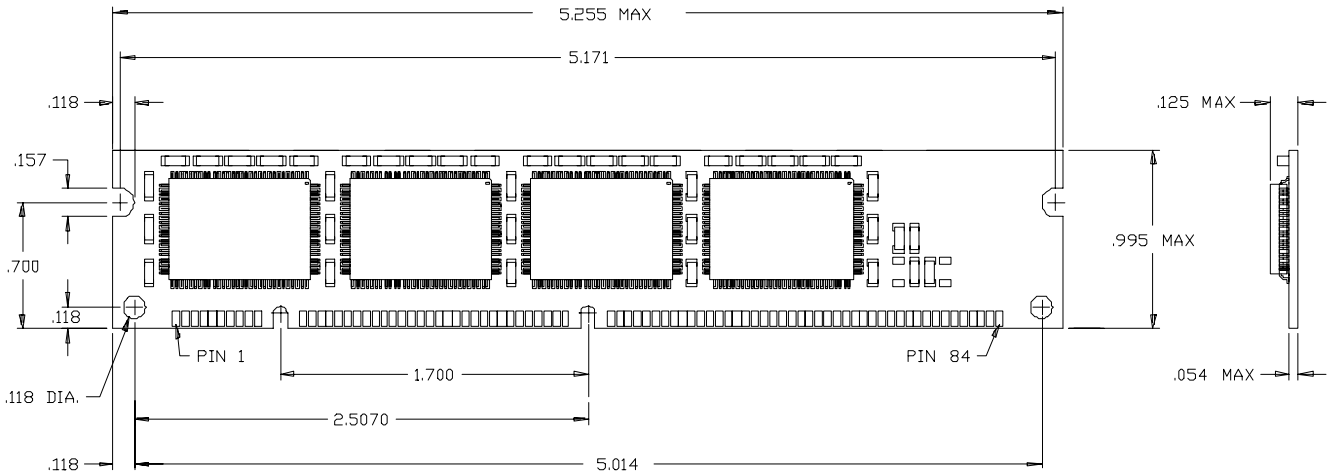
Package Diagrams

168-Pin Single-Sided DIMM PM43



168-Pin Dual Sided DIMM PM44