



**64K x 36 SRAM Module**  
**128K x 36 SRAM Module**  
**256K x 36 SRAM Module**  
**512K x 36 SRAM Module**

**Features**

- Operates at 50 MHz
- Uses 64K x 18 / 128K x 18 or 256K x 18 high-performance synchronous SRAMs
- 144-Position Angled DIMM from Berg p/n 61178
- 3.3V inputs/data outputs

**Functional Description**

The CYM9270, CYM9271B, CYM9272A, and the CYM9273 are high-performance synchronous memory modules organized as 64K(9270), 128K(9271B), 256K(9272A), 512K(9273) by 36 bits. These modules are constructed using either 128K x 18 SRAMs (9270, 9271B, 9272A) or 256K x 18 SRAMs

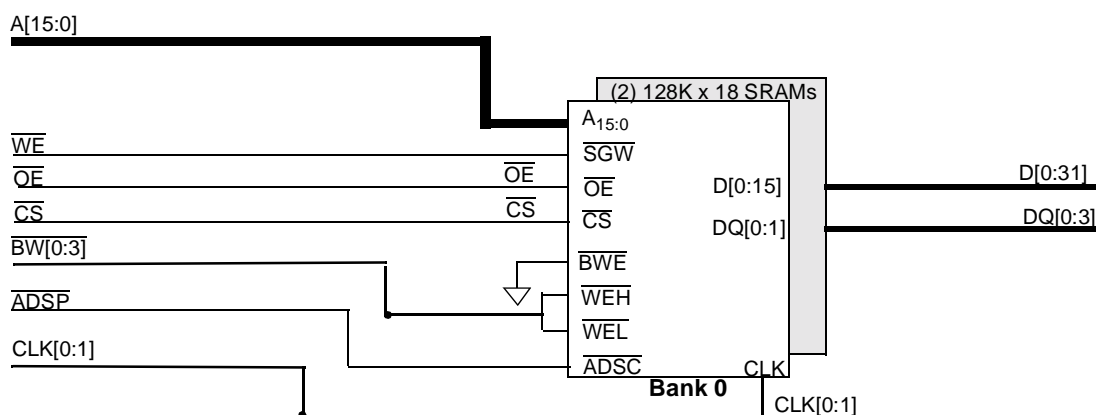
(9273) in plastic surface mount packages on an epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

The modules are configured as single banks or multiple banks depending on the SRAM used to make the module. Separate clock are provided for each of the banks. Separate clocks are provided for each of the SRAMs.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 30 micro-inches of gold flash.

**Logic Block Diagram - CYM9270**

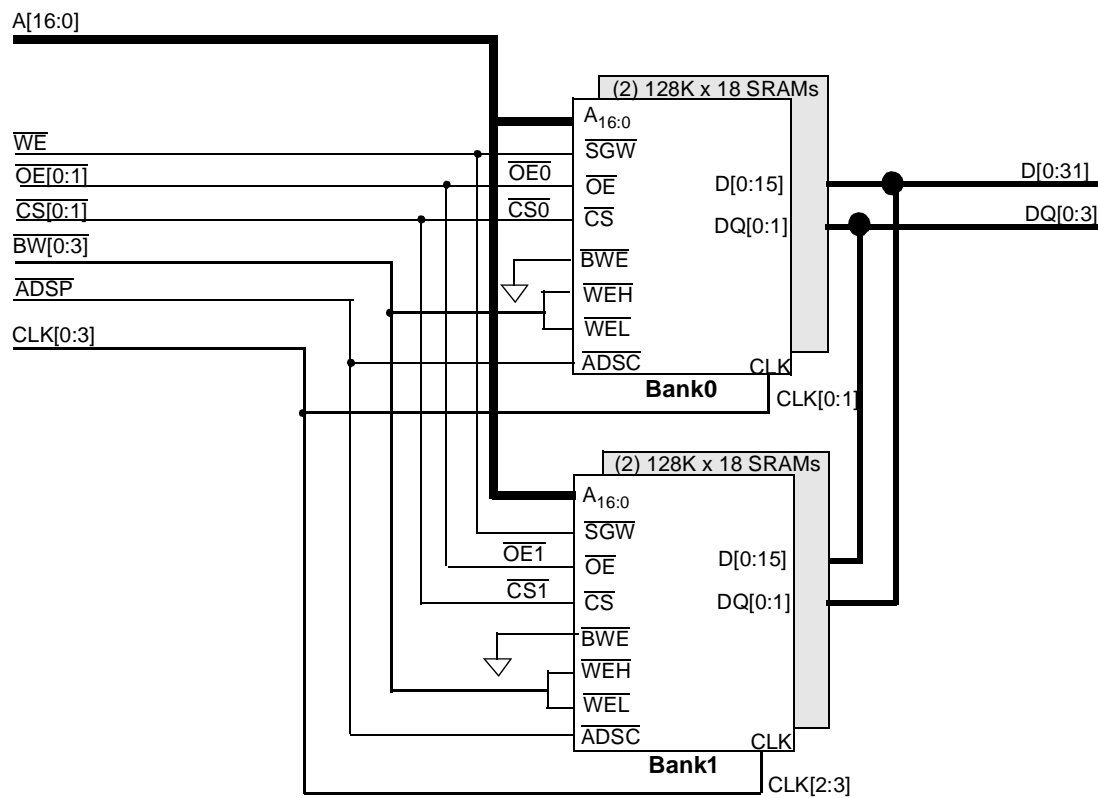


64Kx36 PD<sub>1</sub> PD<sub>0</sub>  
 GND NC **Bank0**

9270



## Logic Block Diagram - CYM9271B/CYM9272A

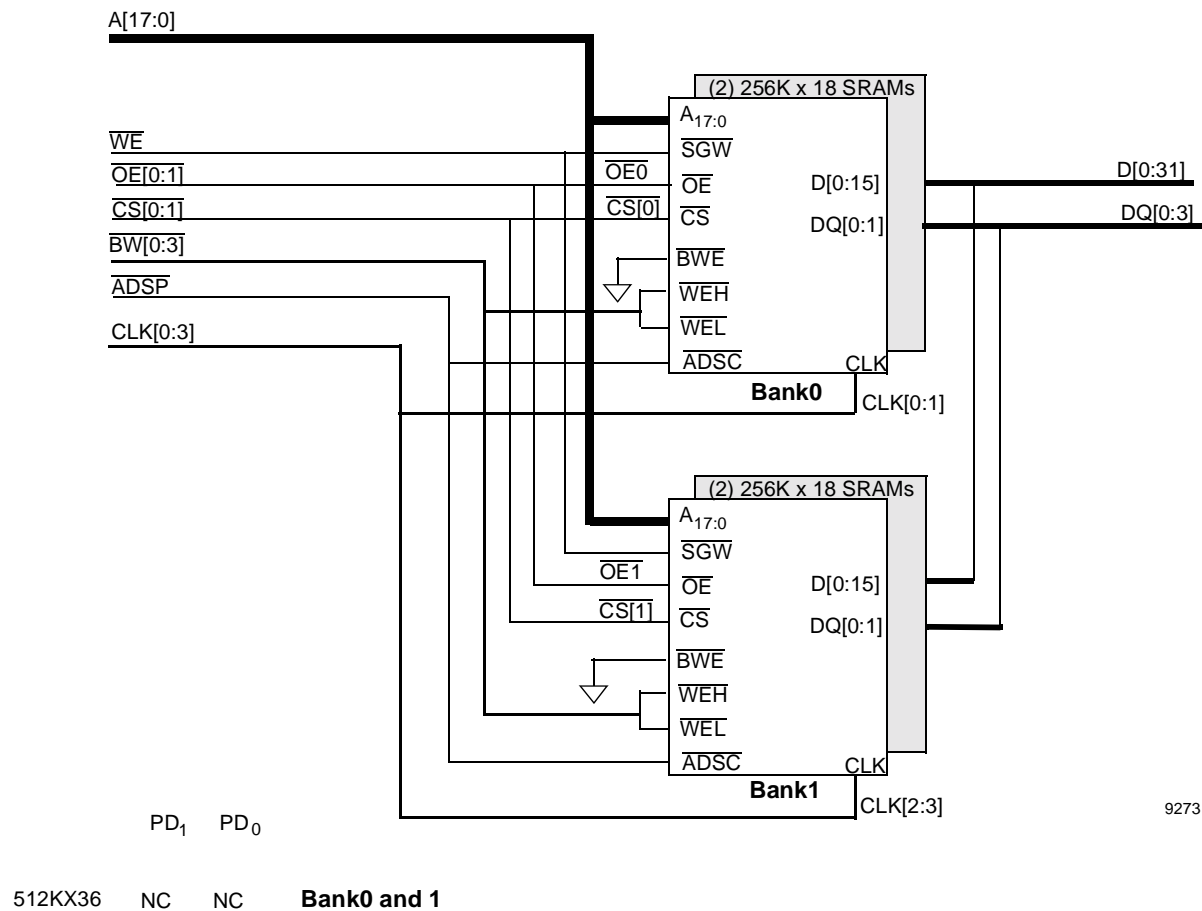


	PD <sub>1</sub>	PD <sub>0</sub>	
128Kx36	NC	GND	<b>Bank0</b>
256Kx36	GND	GND	<b>Bank0 and Bank1</b>

9271B/72A



## Logic Block Diagram - CYM9273





**PinConfiguration**
**Dual Read-Out SIMM (DIMM)**
**Top View**

GND	1	2	GND
A <sub>0</sub>	3	4	A <sub>1</sub>
A <sub>2</sub>	5	6	A <sub>3</sub>
A <sub>4</sub>	7	8	A <sub>5</sub>
V <sub>CC3</sub>	9	10	V <sub>CC3</sub>
NC	11	12	NC
NC	13	14	NC
GND	15	16	GND
A <sub>6</sub>	17	18	A <sub>7</sub>
A <sub>8</sub>	19	20	A <sub>9</sub>
A <sub>10</sub>	21	22	A <sub>11</sub>
NC	23	24	NC
V <sub>CC3</sub>	25	26	V <sub>CC3</sub>
A <sub>12</sub>	27	28	A <sub>13</sub>
A <sub>14</sub>	29	30	A <sub>15</sub>
A <sub>16</sub>	31	32	A <sub>17</sub>
GND	33	34	GND
PD <sub>0</sub>	35	36	PD <sub>1</sub>
GND	37	38	GND
BW[0]	39	40	BW[1]
CS[0]	41	42	OE[0]
GND	43	44	GND
CLK1	45	46	CLK0
GND	47	48	GND
D <sub>0</sub>	49	50	D <sub>1</sub>
V <sub>CC3</sub>	51	52	V <sub>CC3</sub>
D <sub>2</sub>	53	54	D <sub>3</sub>
D <sub>4</sub>	55	56	D <sub>5</sub>
D <sub>6</sub>	57	58	D <sub>7</sub>
GND	59	60	GND
V <sub>CC3</sub>	61	62	V <sub>CC3</sub>
D <sub>8</sub>	63	64	D <sub>9</sub>
D <sub>10</sub>	65	66	D <sub>11</sub>
GND	67	68	GND
D <sub>12</sub>	69	70	D <sub>13</sub>
D <sub>14</sub>	71	72	D <sub>15</sub>
DQ <sub>0</sub>	73	74	DQ <sub>1</sub>
NC	75	76	NC
NC	77	78	NC
GND	79	80	GND
WE	81	82	ADSP
NC	83	84	NC
V <sub>CC3</sub>	85	86	V <sub>CC3</sub>
NC	87	88	NC
NC	89	90	NC
NC	91	92	NC
V <sub>CC3</sub>	93	94	V <sub>CC3</sub>
NC	95	96	NC
NC	97	98	NC
NC	99	100	NC
GND	101	102	GND
BW[2]	103	104	BW[3]
CS[1]	105	106	OE[1]
V <sub>CC3</sub>	107	108	V <sub>CC3</sub>
D <sub>16</sub>	109	110	D <sub>17</sub>
D <sub>18</sub>	111	112	D <sub>19</sub>
NC	113	114	NC
NC	115	116	NC
NC	117	118	NC
GND	119	120	GND
CLK3	121	122	CLK2
GND	123	124	GND
D <sub>20</sub>	125	126	D <sub>21</sub>
GND	127	128	GND
D <sub>22</sub>	129	130	D <sub>23</sub>
D <sub>24</sub>	131	132	D <sub>25</sub>
D <sub>26</sub>	133	134	D <sub>27</sub>
D <sub>28</sub>	135	136	D <sub>29</sub>
V <sub>CC3</sub>	137	138	V <sub>CC3</sub>
D <sub>30</sub>	139	140	D <sub>31</sub>
DQ <sub>2</sub>	141	142	DQ <sub>3</sub>
GND	143	144	GND



## Pin Definitions

Signal	Description
V <sub>CC3</sub>	3V Supply
GND	Ground
A[17:0]	Addresses from processor
ADSP	Address strobe from the processor
OE[1:0]	Output Enables for each of the banks
BW[0:3]	Byte writes
WE	Global Write
CS[1:0]	Chip Select for the two banks
PD <sub>0</sub> –PD <sub>1</sub>	Presence Detect output pins
D[31:0]	Data lines from processor
DQ[3:0]	Data Parity lines from processor
CLK[0:3]	Clock lines to the module.
NC	Signal not connected on module
RSVD	Reserved

## Presence Detect Pins

	PD <sub>1</sub>	PD <sub>0</sub>
CYM9270 – 64K x 36	GND	NC
CYM9271B – 128K x 36	NC	GND
CYM9272A – 256K x 36	GND	GND
CYM9273 – 512K x 36	NC	NC



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -55°C to +125°C

Ambient Temperature  
with Power Applied..... -0°C to +70°C

3.3V Supply Voltage to Ground Potential..... -0.5V to +4.5V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5V to +4.6V

DC Input Voltage ..... -0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 5%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min. I <sub>OH</sub> = -4 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min. I <sub>OL</sub> = 8 mA		0.4	V
I <sub>CC</sub> (9270)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		350	mA
I <sub>CC</sub> (9271B)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		500	mA
I <sub>CC</sub> (9272A)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1000	mA
I <sub>CC</sub> (9273)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1200	mA

## Capacitance<sup>[1]</sup>

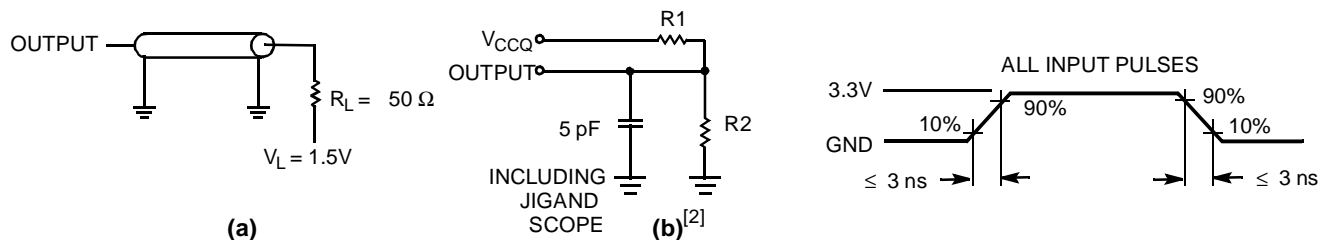
Parameter	Description	Test Conditions	Max.	Max.	Unit
C <sub>A</sub>	Address Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9270	12	pF
			9271B	7	
			9272A	14	
			9273	20	
C <sub>I</sub>	Control Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9270	12	
			9271B	8	
			9272A	16	
			9273	20	
C <sub>O</sub>	Input / Output Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9270	9	
			9271B	5	
			9272A	10	
			9273	16	
C <sub>CLK</sub>	Clock Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9270	6	
			9271B	3	
			9272A	3	
			9273	5	

### Note:

1. Tested initially and after any design or process changes that may affect these parameters.



## AC Test Loads and Waveforms<sup>[3]</sup>



## Switching Characteristics Over the Operating Range

Parameter	Description	CYM9270		CYM9271B		CYM9272A		CYM9273		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CYC}$	Clock Cycle Time	12		12		12		12		ns
$t_{CH}$	Clock HIGH	4		4		4		4		ns
$t_{CL}$	Clock LOW	4		4		4		4		ns
$t_{AS}$	Address Set-Up Before CLK Rise	3		3		3		3		ns
$t_{AH}$	Address Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
$t_{CDV}$	Data Output Valid After CLK Rise		10.3		10.3		10.3		10.3	ns
$t_{DOH}$	Data Output Hold After CLK Rise	3		3		3		3		ns
$t_{WES}$	$\overline{WH}$ , $\overline{WL}$ Set-Up Before CLK Rise	3.1		3.1		3.1		3.1		ns
$t_{WEH}$	$\overline{WH}$ , $\overline{WL}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
$t_{DS}$	Data Input Set-Up Before CLK Rise	3.3		3.3		3.3		3.3		ns
$t_{DH}$	Data Input Hold After CLK Rise	0.5				0.5		0.5		ns
$t_{CSS}$	Chip Select Set-Up	3.1		3.1		3.1		3.1		ns
$t_{CSH}$	Chip Select Hold After CLK Rise	0.5		0.5		0.5		0.5		ns
$t_{EOZ}^{[4]}$	$\overline{OE}$ HIGH to Output High Z		7		7		7		7	ns
$t_{EOV}$	$\overline{OE}$ LOW to Output Valid	7		7		7		7		ns

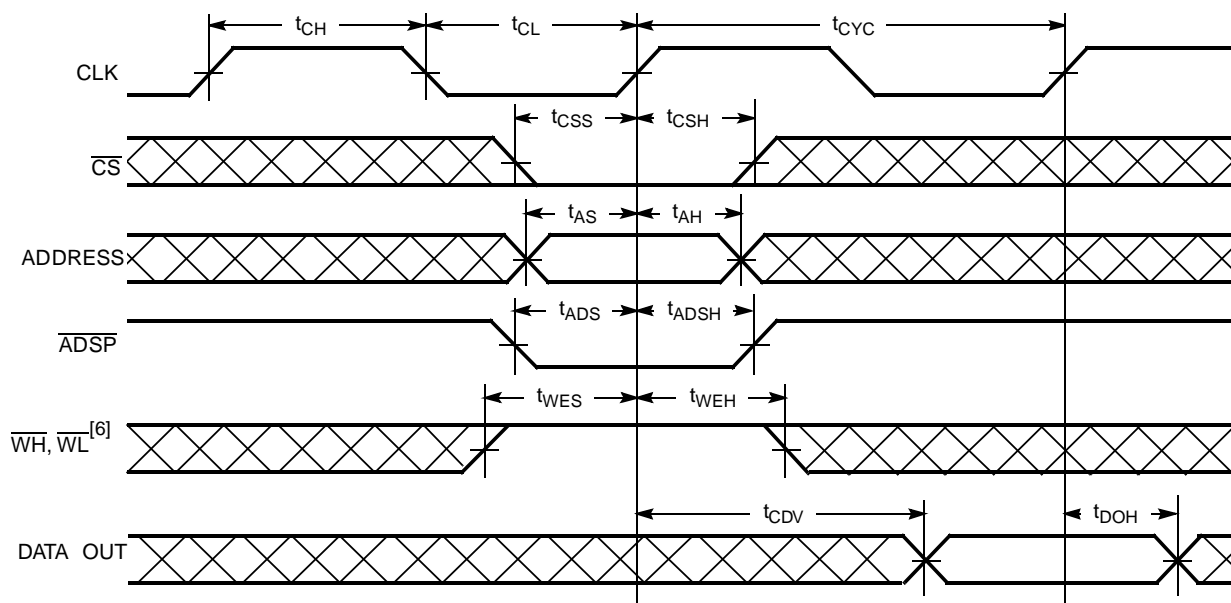
### Notes:

- Resistor values for  $V_{CCQ}=3.3\text{V}$  are  $R1=317\ \Omega$  and  $R2=351\ \Omega$ .
- Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and load capacitance. Shown in (a) and (b) of AC test loads. All measurements are at room temperature.
- $t_{EOZ}$  is specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500\text{ mV}$  from steady-state voltage.

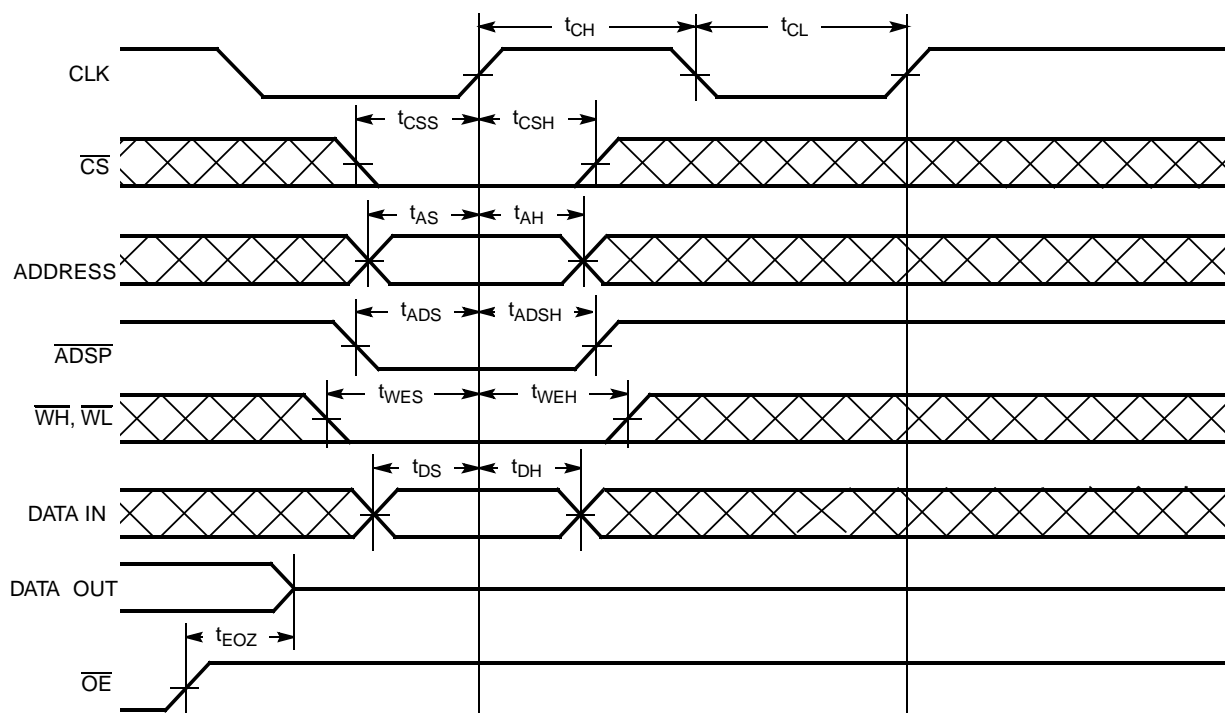


## Switching Waveforms

### Single Read<sup>[5]</sup>



### Single Write Timing



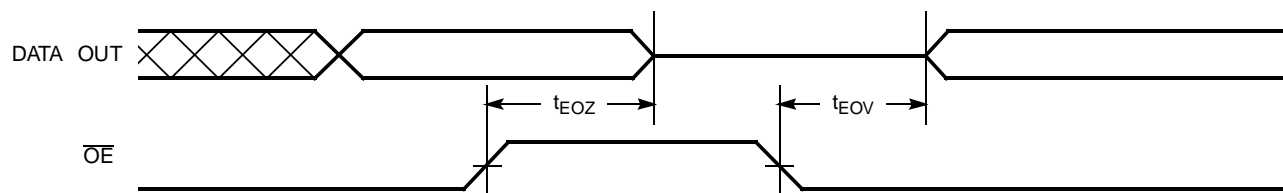
#### Notes:

5. OE is LOW throughout this operation.
6. ADSP has no effect on ADV, WL, and WH if CS is HIGH.

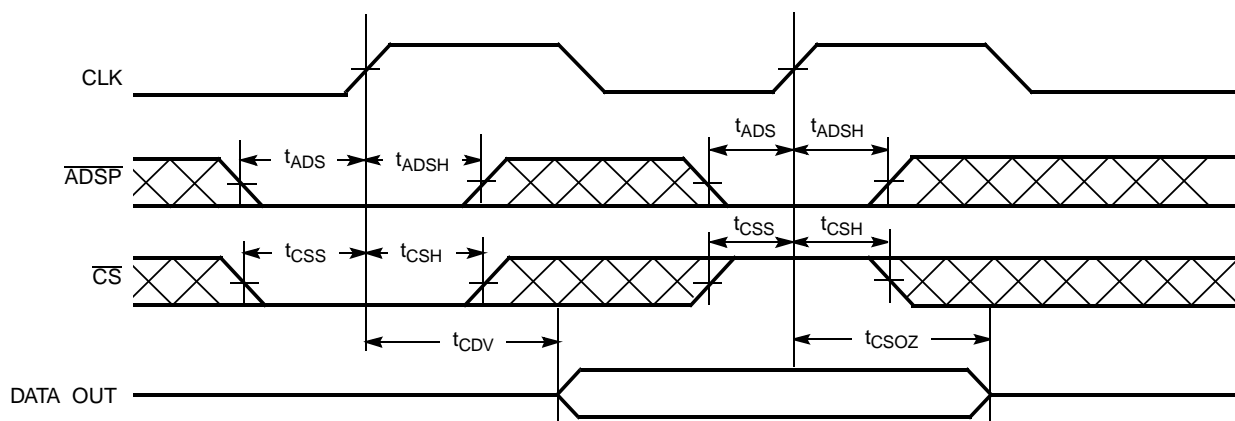


## Switching Waveforms (continued)

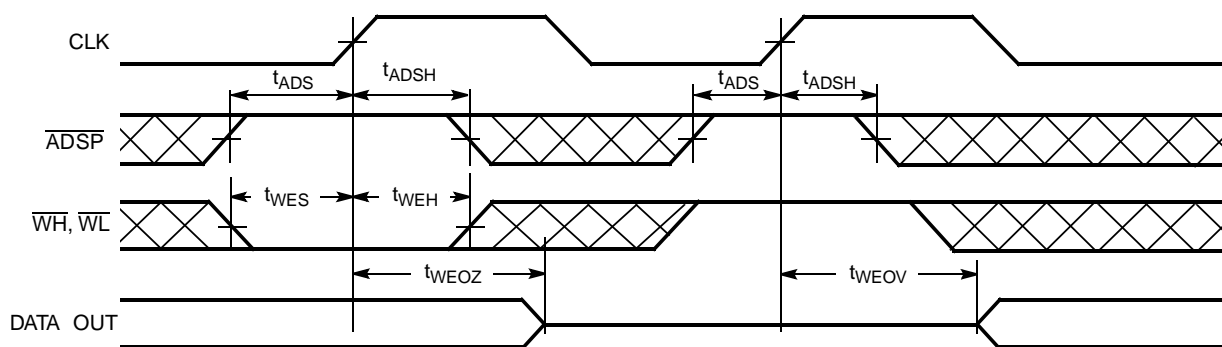
### Output (Controlled by $\overline{OE}$ )



### Output Timing (Controlled by $\overline{CS}$ )



### Output Timing (Controlled by $\overline{WH}/\overline{WL}$ )



## Ordering Information

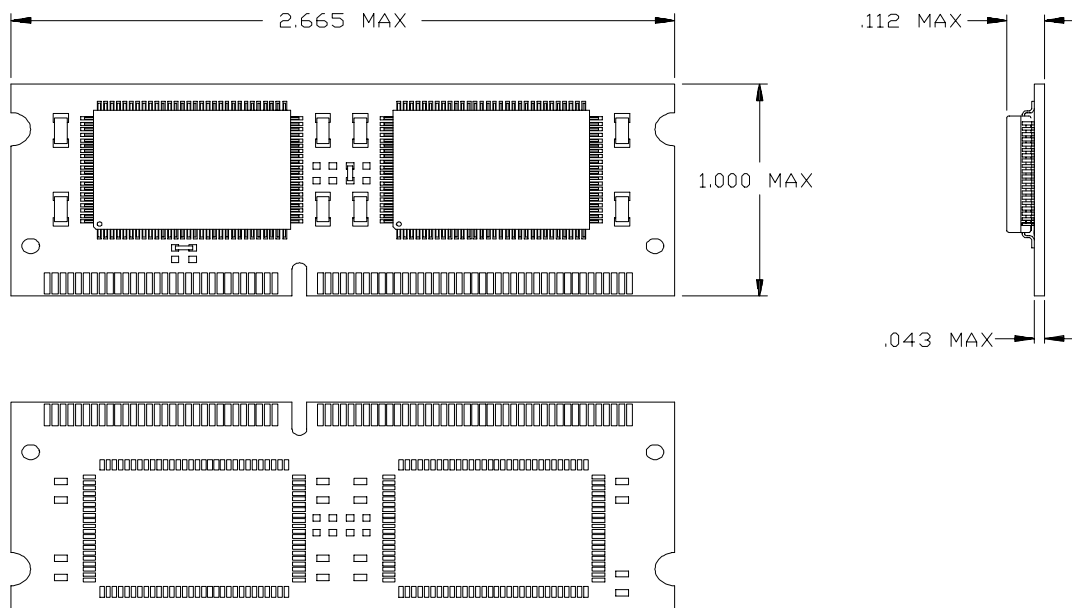
Speed(MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM9270PM-50C	PM45	144-Pin Dual-Readout SIMM	Sync 64K x 36	Commercial
	CYM9271BPM-50C	PM45	144-Pin Dual-Readout SIMM	Sync 128K x 36	
	CYM9272APM-50C	PM46	144-Pin Dual-Readout SIMM	Sync 256K x 36	
	CYM9273PM-50C	PM46	144-Pin Dual-Readout SIMM	Sync 512K x 36	

Document #: 38-M-00083-A



## Package Diagrams

**144-Pin Single-Sided DIMM PM45**



**144-Pin Dual-Sided DIMM PM46**

