CYM1481A

2048K x 8 SRAM Module

Features

- **High-density 16-megabit SRAM modules**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **Low active power**
  - **605 mW (max.), 2M x 8**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Small footprint SIP**
  - **PCB layout area of 0.72 sq. in.**
- **2V data retention (L version)**

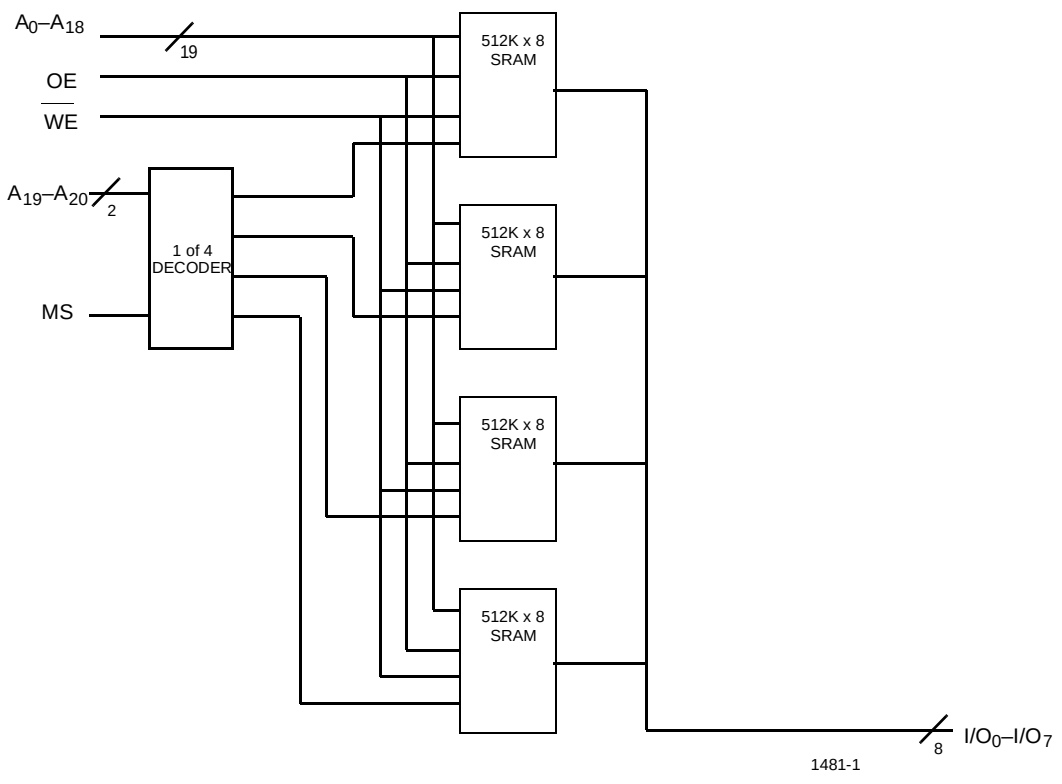
Functional Description

The CYM1481A is a high-performance 16-megabit static RAM module organized as 2048K words by 8 bits. These modules are constructed from four 512K x 8 SRAMs in plastic surface-mount packages on an epoxy laminate board with pins. On-board decoding selects one of the SRAMs from the high-order address lines, keeping the remaining devices in standby mode for minimum power consumption.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs $\overline{MS}$ and $\overline{OE}$ active LOW while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

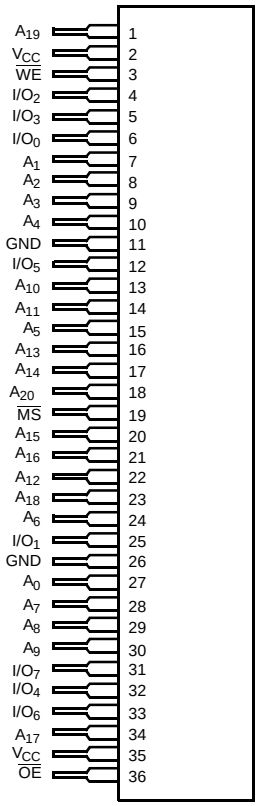
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration

SIP
Top View



Selection Guide

	CYM1481A			
Maximum Access Time (ns)	70	85	100	120
Maximum Operating Current (mA)	110	110	110	110
Maximum Standby Current (mA)	64	64	64	64

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature –55°C to +125°C

Ambient Temperature with Power Applied0°C to +70°C

Supply Voltage to Ground Potential–0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State–0.3V to +7.0V

DC Input Voltage–0.3V to +7.0V

Output Current into Outputs (LOW)20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

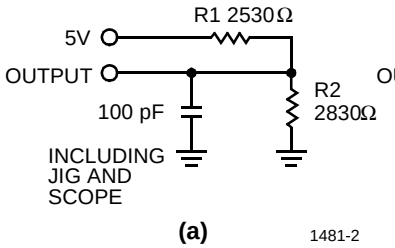
Parameter	Description	Test Conditions		1481A Min.	1481A Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $\overline{MS}$ ≤ V_{IL}, I_{OUT} = 0 mA			110	mA
I_{SB1}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			64	mA
I_{SB2}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V	Standard		32	mA
			L Version –100, –120		500	µA
			L Version –85		1600	µA

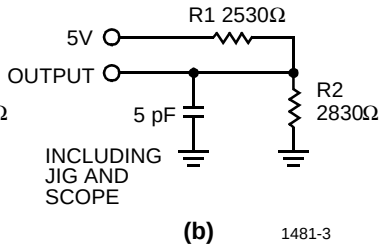
Capacitance[1]

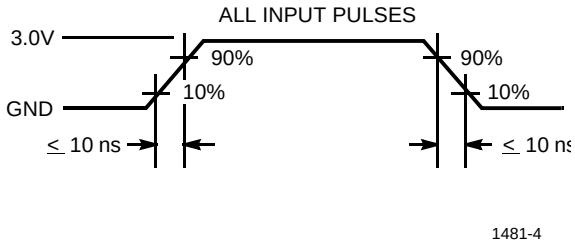
Parameter	Description	Test Conditions	CYM1481AMax.	Unit
C_{INA}	Input Capacitance ($A_{0–16}$, $\overline{OE}$, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	125	pF
C_{INB}	Input Capacitance ($A_{17–20}$, $\overline{MS}$)		25	pF
C_{OUT}	Output Capacitance		165	pF

Note:
1. Tested on a sample basis.

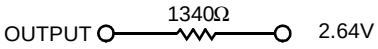
AC Test Loads and Waveforms







Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2]

Parameter	Description	1481A-70		1481A–85		1481A–100		1481A–120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	70		85		100		120		ns
t_{AA}	Address to Data Valid		70		85		100		120	ns
t_{OHA}	Data Hold from Address Change	5		10		10		10		ns
t_{AMS}	$\overline{MS}$ LOW to Data Valid		70		85		100		120	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		40		45		50		60	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		30		30		35		45	ns
t_{LZMS}	$\overline{MS}$ LOW to Low Z[4]	5		10		10		10		ns
t_{HZMS}	$\overline{MS}$ HIGH to High Z[3, 4]		30		30		35		45	ns
WRITE CYCLE[5]										
t_{WC}	Write Cycle Time	70		85		100		120		ns
t_{SMS}	$\overline{MS}$ LOW to Write End	65		75		90		100		ns
t_{AW}	Address Set-Up to Write End	65		75		90		100		ns
t_{HA}	Address Hold from Write End	5		7		7		7		ns
t_{SA}	Address Set-Up to Write Start	0		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	65		65		75		85		ns
t_{SD}	Data Set-Up to Write End	30		35		40		45		ns
t_{HD}	Data Hold from Write End	0		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		30		30		35		40	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		ns

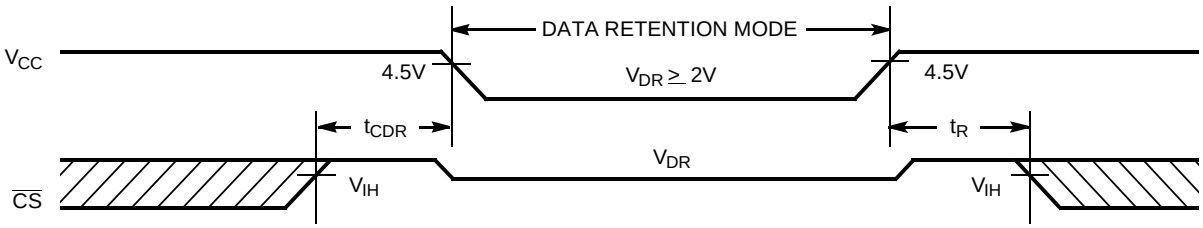
Notes:

2. Test conditions assume signal transition time of 10 μs or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of 1 TTL load, and 100-pF load capacitance.
3. t_{HZOE}, t_{HZMS}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
4. At any given temperature and voltage condition, t_{HZMS} is less than t_{LZMS} for any given device. These parameters are guaranteed and not 100% tested.
5. The internal write time of the memory is defined by the overlap of $\overline{MS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	1481A-70		1481A–85		1481A–100 148A1–120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2		2		2		V
I_{CCDR}	Data Retention Current	V_{DR} = 3.0V, $\overline{MS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		800		800		250	µA
t_{CDR}[6]	Chip Deselect to Data Retention Time		0		0		0		ns
t_R	Operation Recovery Time		5		5		5		ns

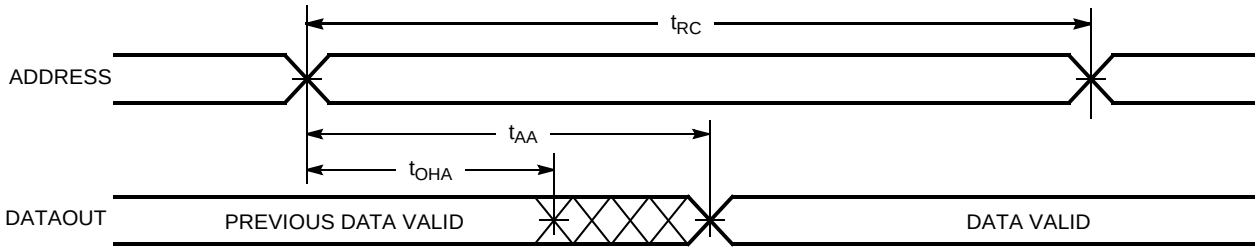
Data Retention Waveform



1481-6

Switching Waveforms

Read Cycle No. 1[7, 8]

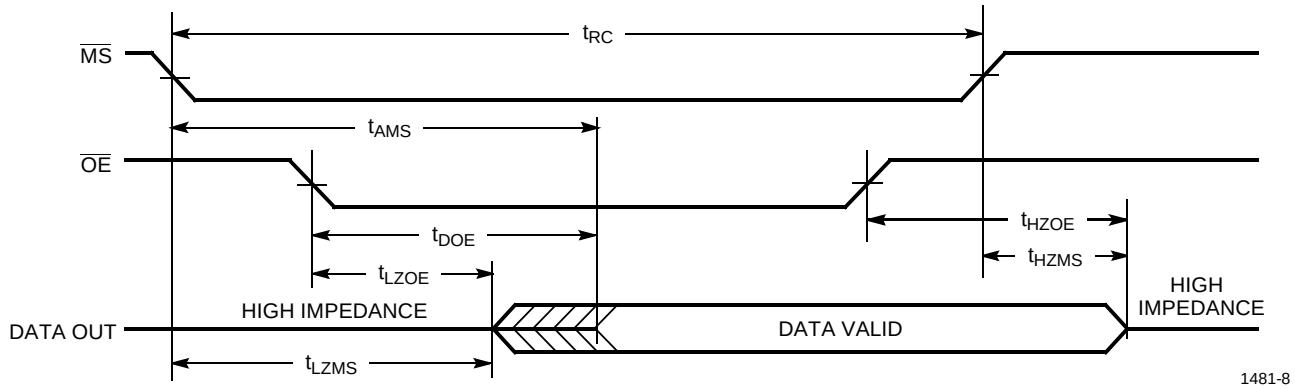


1481-7

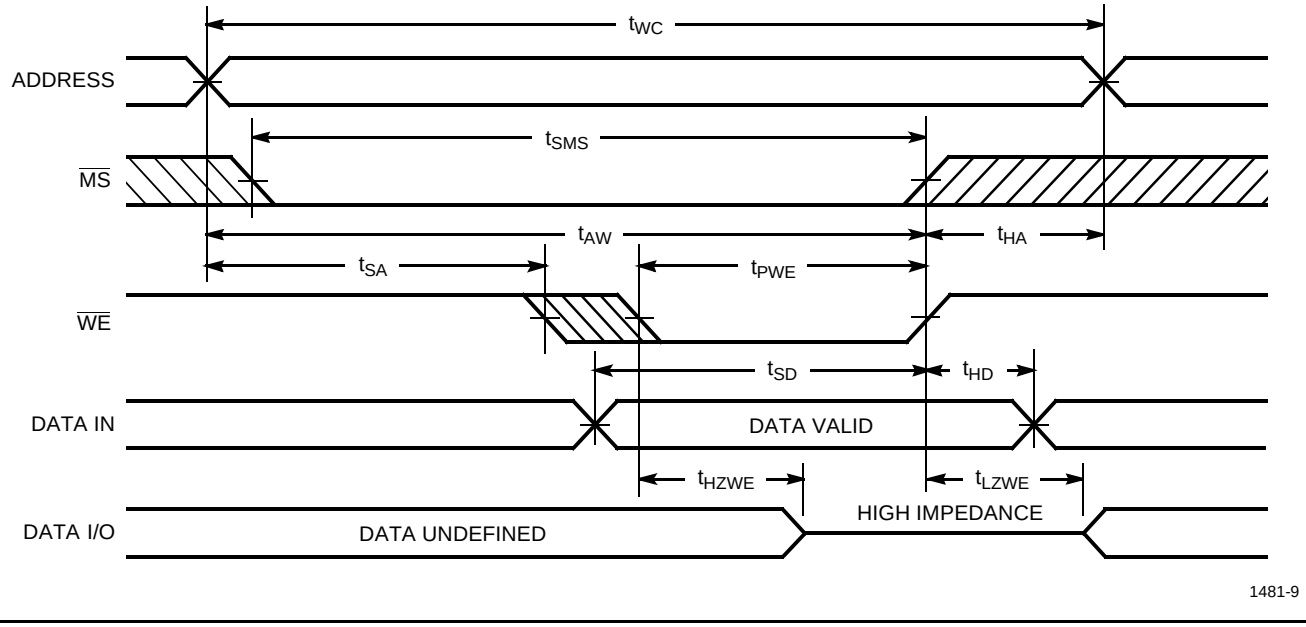
Notes:
6. Guaranteed, not tested.
7. Device is continuously selected. $\overline{OE}$, $\overline{MS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{MS}$ transition LOW.

Switching Waveforms (continued)

Read Cycle No. 2[8, 9]



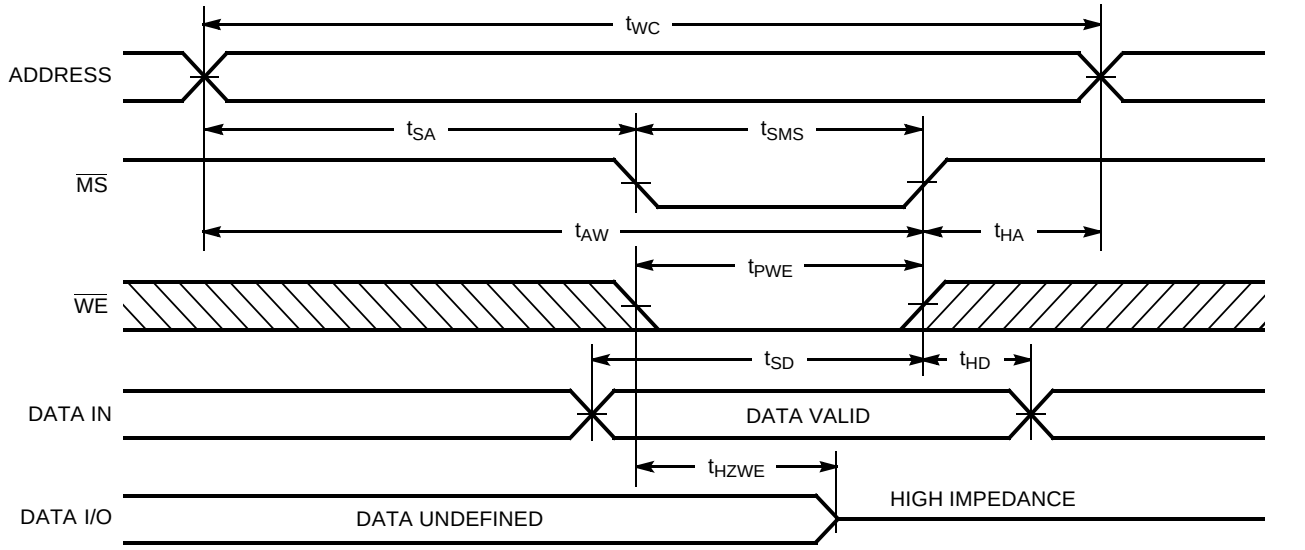
Write Cycle No. 1[5, 10]



Notes:
9. $\overline{WE}$ is HIGH for read cycle.
10. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Switching Waveforms (continued)

Write Cycle No. 2[5, 10, 11]



Note:
11. If $\overline{MS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{MS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
70	CYM1481APS-70C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS-70C			
85	CYM1481APS–85C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS–85C			
100	CYM1481APS–100C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS–100C			
120	CYM1481APS–120C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS–120C			

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Package Diagram

36-Pin SIP Module PS10